UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION,
Petitioner,

v.

COLLABO INNOVATIONS, INC.,
Patent Owner.

Case IPR2016-00940
Patent 8,030,724 B2


CHAGNON, Administrative Patent Judge.

DECISION
Institution of Inter Partes Review
37 C.F.R. § 42.108

I. INTRODUCTION


1 Petitioner identifies Sony Corporation of America and Sony Electronics Inc. as additional real-parties-in-interest. Pet. 1.

We have authority to determine whether to institute \textit{inter partes} review. \textit{See} 35 U.S.C. § 314(b); 37 C.F.R. § 42.4(a). Upon consideration of the Petition and the Preliminary Response, and for the reasons explained below, we determine that the information presented shows a reasonable likelihood that Petitioner would prevail on at least one asserted ground with respect to all of the challenged claims. \textit{See} 35 U.S.C. § 314(a).

Accordingly, we institute trial as to claims 1–4 of the ’724 patent.

\textbf{A. Related Proceedings}

The ’724 patent has been asserted in \textit{Collabo Innovations, Inc. v. Sony Corp.}, No. 1:15-cv-01094 (D. Del.). Pet. 1; Paper 5, 1.

\textbf{B. The Applied References and Evidence}

Petitioner relies on the following evidence. Pet. 2.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Date</th>
<th>Exhibit No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>WO2006/073085 A1 (&quot;Asano&quot;)</td>
<td>July 13, 2006</td>
<td>Ex. 1003(^3)</td>
</tr>
</tbody>
</table>

\(^2\) Patent Owner identifies Wi-LAN Technologies Inc. and Wi-LAN Inc. as additional real-parties-in-interest. Paper 5, 1.

\(^3\) Citations throughout are to the certified translation of Asano (Ex. 1006).

\(^4\) Citations throughout are to the certified translation of Shibayama (Ex. 1005).

\(^5\) Citations throughout are to the certified translation of Yanagida (Ex. 1008).
Petitioner further relies on alleged Admitted Prior Art ("APA"),\(^6\) as well as the Declaration of R. Michael Guidash (Ex. 1002, "Guidash Declaration").

**C. The Asserted Grounds**

Petitioner sets forth its challenges to claims 1–4 as follows. Pet. 2, 15–60.

<table>
<thead>
<tr>
<th>Reference(s)</th>
<th>Basis</th>
<th>Claim(s) Challenged</th>
</tr>
</thead>
<tbody>
<tr>
<td>APA</td>
<td>§ 102</td>
<td>1</td>
</tr>
<tr>
<td>APA and Shibayama</td>
<td>§ 103</td>
<td>2–4</td>
</tr>
<tr>
<td>Asano</td>
<td>§ 103</td>
<td>1, 2</td>
</tr>
<tr>
<td>Asano and Shibayama</td>
<td>§ 103</td>
<td>3, 4</td>
</tr>
<tr>
<td>Yanagida</td>
<td>§ 103</td>
<td>1, 2</td>
</tr>
<tr>
<td>Yanagida and Holm</td>
<td>§ 103</td>
<td>3, 4</td>
</tr>
</tbody>
</table>

**D. The ’724 Patent**

The ’724 patent relates to solid-state imaging devices, and methods for fabricating such devices. Ex. 1001, at [54]. According to the ’724 patent, the invention “provide[s] a solid-state imaging device having a structure that can suppress an increase in leakage current at the PN junction and an increase in dark current.” *Id.* at 2:60–64.

---

\(^6\) Petitioner asserts that the “Background of the Invention” section at Ex. 1001, 1:22–2:55, Figs. 12, 13A, 13B is Admitted Prior Art. Pet. 15–16.
Figures 1A and 1B of the '724 patent, annotated by the panel, are reproduced below.

**FIG. 1A**

**FIG. 1B**

Figures 1A and 1B are a plan view and a cross-sectional view, respectively, of a solid-state imaging device according to one embodiment of the invention of the '724 patent. *Id.* at 4:24–28. As seen in Figures 1A and 1B,
P-type semiconductor layer 2 (highlighted in yellow) is formed in semiconductor substrate 1 (highlighted in blue), which is formed of N-type silicon. *Id.* at 5:24–28. N⁺-type semiconductor layer 3 (highlighted in green) is formed in a surface portion of P-type semiconductor layer 2. *Id.* at 5:28–30. Insulating film 4 is formed on a surface of semiconductor substrate 1. *Id.* at 5:30–32.

Through hole 6 is formed in insulating film 4 and semiconductor substrate 1. *Id.* at 6:8–9. Insulating film 7 (highlighted in purple, above) is formed on a sidewall portion of through hole 6, as well as on a rear surface of semiconductor substrate 1. *Id.* at 6:11–13. Through electrode 8 (highlighted in pink, above) is formed, filling the inside of insulating film 7. *Id.* at 6:13–14. Pad portion 5 is formed on a front side of semiconductor substrate 1 and is connected to N⁺-type semiconductor layer 3 and through electrode 8 through openings in insulating film 4. *Id.* at 6:19–22. Rear surface electrode 9, insulating resin layer 10, and protruding electrode 11 are formed on a rear side of semiconductor substrate 1. *Id.* at 6:25–34.
According to the invention of the '724 patent, “a region in which the P-type semiconductor layer 2 is formed is reduced as compared to the conventional art” (id. at 6:43–45), which is shown in Figures 13A and 13B, annotated by the panel, and reproduced below.

FIG. 13A

FIG. 13B

Figures 13A and 13B are a plan view and a cross-sectional view, respectively, of a conventional solid-state imaging device, according to the '724 patent. Id. at 5:3–7. Similar features are highlighted in similar colors, as compared to the annotated versions of Figures 1A and 1B,
reproduced above. As can be seen in a comparison of Figures 1A and 1B to Figures 13A and 13B, “through hole 6 [of the device of Figures 1A and 1B] does not penetrate through a PN junction region,” whereas through hole 116 in the device of Figures 13A and 13B does penetrate through a PN junction region (see points b, circled in red, above). \textit{Id.} at 6:45–47; 2:30–34. In the embodiment shown in Figures 1A and 1B, through hole 6 “penetrates through a region having a single conductivity type, and the through electrode 8 is formed in the through hole 6.” \textit{Id.} at 6:47–49. According to the ’724 patent, by this arrangement, “it is possible to reduce and suppress a leakage current at a PN junction caused by etching damage or the like occurring when a through hole penetrates through the PN junction region, and a dark current that becomes more significant during an operation at high temperature.” \textit{Id.} at 6:50–54. These benefits “result[] in a solid-state imaging device having a high-sensitivity and a high [signal-to-noise (S/N)] ratio.” \textit{Id.} at 6:54–57.

Of the challenged claims, claim 1 is independent. Claims 2–4 depend, directly or indirectly, from claim 1. Claim 1 of the ’724 patent, reproduced below, is illustrative of the challenged claims:

1. A solid-state imaging device, comprising:

   a first conductivity type semiconductor substrate having the imaging region and the peripheral circuit region on a main surface thereof;

   an imaging region formed on a main surface of the semiconductor substrate and having a plurality of light receiving portions arranged two-dimensionally and for generating signal electric charges by photoelectric conversion;
a peripheral circuit region formed on a main surface of the semiconductor substrate and formed in an outer peripheral portion of the imaging region;

a second conductivity type first semiconductor layer formed in the first conductivity type semiconductor substrate at a side of the main surface of the semiconductor substrate;

a first conductivity type second semiconductor layer formed in the first semiconductor layer;

a through electrode formed in a through hole penetrating through the semiconductor substrate in a thickness direction of the semiconductor substrate;

a pad portion formed on the main surface of the semiconductor substrate and connected to the through electrode; and

a side insulating film formed at a side surface of the through electrode.

Ex. 1001, 15:35–16:22.

II. ANALYSIS

A. Claim Construction

In an inter partes review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. See 37 C.F.R. § 42.100(b); Cuozzo Speed Techs. LLC v. Lee, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard). Under the broadest reasonable construction standard, claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. See In re Translogic Tech., Inc., 504 F.3d 1249, 1257 (Fed. Cir. 2007). The claims, however, “should always be read in light of the specification and teachings in the
underlying patent,’” and “[e]ven under the broadest reasonable interpretation, the Board’s construction ‘cannot be divorced from the specification and the record evidence.’” Microsoft Corp. v. Proxyconn, Inc., 789 F.3d 1292, 1298 (Fed. Cir. 2015) (citations omitted). Further, any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. See In re Paulsen, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner proposes constructions for three claim phrases:

(1) “peripheral circuit region formed on a main surface of the semiconductor substrate and formed in an outer peripheral portion of the imaging region”;

(2) “second conductivity type first semiconductor layer formed in the first conductivity type semiconductor substrate at a side of the main surface”; and

(3) “semiconductor layer.”

Pet. 9–15. In its Preliminary Response, Patent Owner disagrees with Petitioner’s proposed constructions. Prelim. Resp. 8–14. For purposes of this Decision, we address the construction of “peripheral circuit region . . . formed in an outer peripheral portion of the imaging region”; no other terms require express construction at this stage of the proceeding. See, e.g., Wellman, Inc. v. Eastman Chem. Co., 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”) (quoting Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999)).

Claim 1 recites “a peripheral circuit region . . . formed in an outer peripheral portion of the imaging region.” Petitioner asserts that “the
relationship of the ‘imaging region’ to the ‘peripheral circuit region’ warrants interpretation.” Pet. 10. According to Petitioner, the “outer peripheral portion” need not be in the imaging region, but is merely associated with the imaging region. Id. at 11. Specifically, Petitioner proposes the phrase peripheral circuit region . . . formed in an outer peripheral portion of the imaging region should mean a peripheral circuit region . . . formed near the outer portions of the imaging region (whether inside or outside of that region). Id. at 12–13. Patent Owner argues that the “spatial arrangement of the peripheral circuit region in relation to the imaging region is easily ascertained from the claim language and does not require explicit construction.” Prelim. Resp. 9. Patent Owner also argues that Petitioner is attempting to “improperly expand the meaning of the claim limitation.” Id.

Figure 12 of the ’724 patent is instructive, and is reproduced below.

Figure 12 is a plan view showing a schematic structure of a conventional solid-state imaging device, according to the ’724 patent. Ex. 1001, 1:39–40. The ’724 patent describes internal circuit region 101 “provided at a middle portion of” semiconductor substrate 100, and peripheral circuit region 102
“provided at a peripheral portion” of semiconductor substrate 100. Id. at 1:41–46. The ’724 patent further describes internal circuit region 101 has “having a light receiving portion and a drive circuit portion” and describes peripheral circuit region 102 as “having a pad portion and a protective circuit portion.” Id. In describing the preferred embodiments, the ’724 patent refers to Figure 12 to show the location of the peripheral circuit region and an internal circuit region, including light receiving portions. Id. at 5:36–65.

Patent Owner disputes that the phrase “formed in an outer peripheral portion of the imaging region” can include circuits formed “outside the imaging region.”7 Prelim. Resp. 9. Based on the description in the ’724 patent and the evidence now before us, we determine that a peripheral circuit region formed in an outer peripheral portion of the imaging region includes, at least, a peripheral circuit region formed at or adjacent the outer edges of the imaging region.8 We need not further construe this term for purposes of this Decision.

B. Grounds Based, At Least in Part, on Asano

Petitioner asserts that claims 1 and 2 are unpatentable under 35 U.S.C. § 103 as obvious in view of Asano. Pet. 2, 34–46. Petitioner further asserts

7 We note that other limitations in the claim require the peripheral circuit region to be formed on the semiconductor substrate with the imaging region, thus addressing Patent Owner’s concern that an interpretation allowing the peripheral circuit region to be outside of the imaging region could encompass any circuit outside the imaging region. See Prelim. Resp. 11.
8 This is consistent with the plain meaning of “periphery.” See Periphery Definition, MERRIAM-WEBSTER.COM, http://www.merriam-webster.com/dictionary/periphery (last accessed Oct. 18, 2016) (3a : the outward bounds of something as distinguished from its internal regions or center; 3b : an area lying beyond the strict limits of a thing).
that claims 3 and 4 are unpatentable under 35 U.S.C. § 103 as obvious in view of Asano in combination with Shibayama. *Id.* at 2, 46–49. In its Preliminary Response, Patent Owner argues that Asano does not disclose several features of independent claim 1. Prelim. Resp. 19–29. We have reviewed the parties’ contentions and supporting evidence in the current record, and, for the reasons explained below, determine that the information presented shows a reasonable likelihood that Petitioner would prevail on these asserted grounds.

1. **Summary of Asano**

Asano relates to solid-state image pickup devices and methods for manufacturing the same. Ex. 1006 ¶ 1. Figure 1 of Asano is reproduced below.

Figure 1 is a structural sectional view showing a basic construction of the image pickup device of Asano. *Id.* ¶ 19. The image pickup device shown in Figure 1 includes “a large number of photoreceiving sections 2, and microlenses 3 formed individually on the photoreceiving sections, disposed on the front face of the wafer 1.” *Id.* ¶ 20. “Penetrating electrodes 4 are provided at numerous locations in the peripheral section of the wafer 1, through which power is supplied to, and electrical signals are transmitted to
and from the photoreceiving sections 2.” *Id.* Electrodes 4 are connected to electrode pad 4a on one end and rear face electrode 5 on the other end. *Id.*

Figure 3 of Asano is reproduced below.

![Figure 3 of Asano](image)

Figure 3 is a sectional view showing formation of penetrating electrodes 4, according to Asano. *Id.* ¶ 42. “[T]renches 16 are formed from the front face of the wafer 1 beforehand, localized oxide film 17 is formed, . . . [and] the trenches are filled with an electrode material to form the wiring and then connected to the electrode pad.” *Id.* As described in Asano, by forming through electrodes using this method “the occurrences of dry etching damage and crystal defects can be considerably reduced.” *Id.* ¶ 43.

2. **Summary of Shibayama**

Shibayama relates to a semiconductor device and process for producing the same. Ex. 1005, Abstract. Figure 17 of Shibayama is reproduced below.
Figure 17 is a sectional view of the photodiode array of Shibayama.  
*Id.* ¶ 54. As seen in Figure 17, the device of Shibayama includes through holes 105c with through-wiring 115 (i.e., a through electrode) disposed therein. *Id.* ¶¶ 61, 63. Through-wiring 115 is surrounded by oxidized film 113. *Id.* ¶¶ 61–63. During formation of through holes 105c, holes 141 are etched into substrate 105. *Id.* ¶¶ 83–84, Fig. 20(c). Shibayama describes that forming holes 141 can result in damage at the wall faces, resulting in unnecessary carriers, which can in turn cause dark current and/or noise. *Id.* ¶ 98.

The faces of the through holes are doped to create high concentration N-type regions 125 surrounding the through hole. *Id.* ¶ 85, Fig. 21(a). Shibayama notes that “the n-type high impurity concentration regions 125 formed along the wall faces defining the through holes can trap the unnecessarily generated carriers thereby preventing them from affecting the photodiodes.” *Id.* ¶ 76. The walls of holes 141 are then covered with oxidized film 113, and polysilicon (which serves as through-wiring 115) is deposited. *Id.* ¶¶ 85–87, Fig. 21(b).
3. Analysis

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. See KSR Int’l Co. v. Teleflex Inc., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. Graham v. John Deere Co., 383 U.S. 1, 17–18 (1966).

In that regard, an obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” KSR, 550 U.S. at 418; accord In re Translogic Tech., 504 F.3d at 1259. The level of ordinary skill in the art may be reflected by the prior art of record. See Okajima v. Bourdeau, 261 F.3d 1350, 1355 (Fed. Cir. 2001); In re GPAC Inc., 57 F.3d 1573, 1579 (Fed. Cir. 1995); In re Oelrich, 579 F.2d 86, 91 (CCPA 1978).

Obviousness in View of Asano — Claims 1 and 2

Petitioner’s Arguments and Evidence

Petitioner asserts that claims 1 and 2 are unpatentable under 35 U.S.C. § 103 as obvious in view of Asano. Pet. 2, 34–46. Claim 1 recites a “solid-state imaging device.” Asano describes a solid-state image pickup device and methods for manufacturing the same. Ex. 1006, Title; see Pet. 35 (citing Ex. 1006, Title, ¶ 8). Petitioner relies on wafer 1 of Asano, an “n-type
wafer,” as teaching the claimed first conductivity type semiconductor substrate. Pet. 36 (citing Ex. 1006 ¶ 45; Ex. 1002 ¶¶ 206–207).

Petitioner asserts that photoreceiving regions 2, each with an optical element (microlenses 3) formed thereon, and disposed on the front face of wafer 1, teach the claimed “imaging region” formed on “a main surface” of the substrate. Id. at 36–37 (citing Ex. 1006, Abstract, ¶¶ 19–20, Fig 1; Ex. 1002 ¶¶ 208–209). Regarding the claimed “imaging region . . . having a plurality of light receiving portions [being] arranged two-dimensionally,” Petitioner notes that Asano does not expressly state that photoreceiving regions 2 and microlenses 3 (which Petitioner maps to the claimed “imaging region”) are arranged two-dimensionally. Id. at 35, 39. Petitioner, however, asserts that this arrangement would have been obvious in view of the teachings of Asano. Id. at 38–39. In particular, Petitioner argues that one of skill in the art would have understood imaging devices, such as the one taught in Asano, to include two-dimensional arrays of photoreceiving sections in practice. Id. at 39–40 (citing Ex. 1006, Abstract, ¶ 65; Ex. 1002 ¶¶ 219–222, 224).

Regarding the claimed “imaging region” being “for generating signal electric charges by photoelectric conversion,” Petitioner points to Asano’s teaching that power is supplied to, and electrical signals are transmitted to and from, photoreceiving sections 2 via electrodes 4. Id. at 40 (citing Ex. 1006 ¶ 20). Petitioner also points to Mr. Guidash’s testimony that image pickup devices sense images using photoreceiving sections to generate such signal electric charges by photoelectric conversion, as claimed. Id. (citing Ex. 1002 ¶¶ 29, 32, 223).
Petitioner further relies on “electrode pads 4a and ‘semiconductor device responsible for performing imaging function, such as . . . , a protection diode’” as teaching the claimed “peripheral circuit region” formed on “a main surface” of the substrate. *Id.* at 37 (citing Ex. 1006 ¶¶ 19, 25; Ex. 1002 ¶ 210), 38 (citing Ex. 1006 ¶ 56, Fig. 1; Ex. 1002 ¶ 215).

According to Petitioner, “the peripheral circuit region [of Asano], including electrode pads 4a . . . and the protection diode immediately below the electrode pads, is formed near an outer region . . . of the imaging region,” thus, teaching that the peripheral circuit region” is “formed in an outer peripheral portion of the imaging region,” as claimed. *Id.* at 40 (citing Ex. 1006, Fig. 1; Ex. 1002 ¶ 225).

Petitioner points to Asano’s “p-type well formed at the front face section of the n-type wafer” as teaching the claimed “second conductivity type first semiconductor layer formed in the first conductivity type semiconductor substrate.” Pet. 40–41 (citing Ex. 1006 ¶ 45; Ex. 1002 ¶¶ 227–228). Petitioner’s annotated version of Figure 1 (*id.* at 41) is reproduced below.

Figure 1 is a sectional view of the image pickup device of Asano. Ex. 1006 ¶ 19. As seen in annotated Figure 1, the p-type well (highlighted in green) is “formed . . . at a side of the main surface of the semiconductor substrate” (highlighted in yellow). Pet. 41.
Petitioner notes that Asano does not expressly state that the photodiodes include n-type layers formed in the p-type well. *Id.* at 35. Petitioner asserts, however, that one skilled in the art would understand that the sensor of Asano must include an n-type layer in the p-type well, thus forming a p-n junction, in order for the sensor to function properly. *Id.* at 41–42 (citing Ex. 1002 ¶¶ 231–232). Petitioner relies on this n-type layer as teaching the claimed “first conductivity type second semiconductor layer formed in the first semiconductor layer.” *Id.* Petitioner’s annotated version of Figure 1 (*id.* at 42) is reproduced below.

![Image of Figure 1](image.png)

Figure 1 is a sectional view of the image pickup device of Asano. Ex. 1006 ¶ 19. In the annotated Figure 1, the n-type layer Petitioner relies on as teaching the claimed “first conductivity type second semiconductor layer” is highlighted in red, with the p-type well (which Petitioner maps to the claimed “first semiconductor layer”) highlighted in green, and wafer 1 (which Petitioner maps to the claimed “substrate”) highlighted in yellow. Pet. 42
Two additional annotated versions of Figure 1, provided by Petitioner (Pet. 42, 45) are reproduced below.

Figure 1 is a sectional view of the image pickup device of Asano. Ex. 1006 ¶ 19. The annotated versions of Figure 1 show electrodes 4 (highlighted in yellow), electrode pads 4a (highlighted in pink), and localized oxide film 17 (highlighted in blue), upon which Petitioner relies as teaching the claimed through electrode, pad portion, and side insulating film, respectively. Pet. 42 (citing Ex. 1006 ¶ 20; Ex. 1002 ¶ 234), 43 (citing Ex. 1006 ¶ 20; Ex. 1002 ¶ 237), 44 (citing Ex. 1006 ¶ 42; Ex. 1002 ¶ 240).

As can be seen in the figures above, and as described in Asano, electrodes 4 are “formed in a through hole penetrating through the semiconductor substrate in a thickness direction of the semiconductor substrate,” as claimed. Pet. 42–43 (citing Ex. 1006 ¶¶ 38–39, 41, Figs. 2a, 2b; Ex. 1002 ¶¶ 235–236). As also can be seen in the figures above, electrode pads 4a are “formed on the main surface of the semiconductor substrate.” Id. at 43 (citing Ex. 1006 ¶ 20; Ex. 1002 ¶ 237). Asano also teaches that electrodes 4 are “connected to” electrode pads 4a. Ex. 2006 ¶ 20; see Pet. 43. The figures above also show localized oxide film 17 being “formed at a side surface of the through electrode,” as claimed. Pet. 45 (citing Ex. 1002 ¶¶ 242–243); see Ex. 1006 ¶ 42, Fig. 3; Ex. 1002 ¶¶ 239–241).
Regarding claim 2, which recites that “the through hole penetrates through only a first conductivity type area of the semiconductor substrate,” (Ex. 1001, 16:24–26), Petitioner relies on Figure 8 of Asano, which is similar to Figure 1, and “shows an embodiment where the through holes containing electrodes 4” “penetrate only through the N-type substrate 1,” as teaching this claim feature. Pet. 45–46 (citing Ex. 1006 ¶¶ 20, 26, Fig. 8; Ex. 1002 ¶¶ 245–247).

Patent Owner’s Arguments

In its Preliminary Response, Patent Owner argues that several limitations of independent claim 1 are missing from Asano. See Prelim. Resp. 19–29. Specifically, Patent Owner asserts that Asano does not teach or suggest the claimed “peripheral circuit region,” “second conductivity type first semiconductor layer,” or “first conductivity type second semiconductor layer.” Id. We address each of Patent Owner’s arguments in turn.

Peripheral Circuit Region

Patent Owner argues that Asano does not teach or suggest the claimed “peripheral circuit region.” Id. at 19–22. According to Patent Owner, Asano does not describe any circuits in the purported peripheral circuit region of Figure 1. Id. at 19–20. Patent Owner further asserts that Petitioner’s reliance on disclosure regarding an interline charge coupled device (“CCD”) in Asano to teach a protection diode “immediately below or at the periphery of the electrode pad” (Ex. 1006 ¶ 45), “incorrectly imports into Asano’s Figure 1 a feature from an embodiment specifically distinguished by Asano from the embodiment of Figure 1.” Prelim. Resp. 20. According to Patent Owner, in the case of a CCD, “penetrating electrodes cannot be disposed at the electrode pad location,” and, thus, the
teachings of Asano regarding the CCD embodiment are incompatible with the teachings of Figure 1 of Asano. *Id.* at 20–21 (citing Ex. 1006 ¶ 45).

Asano, however, also teaches that, in the case of a CCD, “[t]he region for the protection diode immediately below or at the periphery of the pad electrode can alternatively be structured as an annular shape or plural divided regions, and the penetrating electrodes be formed in the wafer region on the inside of the annular region or the plural divided regions where the region for the protection diode is absent.” Ex. 1006 ¶ 46 (emphasis added). According to Asano, “[t]his allows for the penetrating electrodes to be formed immediately below the electrode pad thereby having the penetrating electrodes come directly into contact with the electrode pad.” *Id.* (emphasis added).

Based on the evidence now before us, we agree with Petitioner’s contention that the discussion about the CCD in paragraphs 45 and 46 of Asano may apply to the device shown in Figure 1 thereof. Nothing in Asano leads us to conclude that the “basic construction of the image pickup device according to the invention” (Ex. 1006 ¶ 19) discussed with respect to Figure 1 is not applicable to all of the teachings of Asano. We are not persuaded by Patent Owner’s arguments that these teachings are incompatible.

Based on the evidence now before us, we are persuaded that the evidence supports a finding that Asano teaches the claimed “peripheral circuit region.”

**Second Conductivity Type First Semiconductor Layer**

Patent Owner also argues that Asano does not teach or suggest the claimed “second conductivity type first semiconductor layer.” Prelim.
Resp. 22–26. Patent Owner’s argument is largely premised on its assertion that the discussion of the interline CCD embodiment in Asano is incompatible with the embodiment of Figure 1 (see id.), which we do not find persuasive for the reasons discussed above.

Patent Owner also argues that the structure of Figure 1 of Asano “has no p-n junction,” but instead “describes an image sensor based on the MOS capacitor (Metal Oxide Semiconductor).” Id. at 25. On the record now before us, we are persuaded by Petitioner’s assertion (Pet. 41–42), supported by Mr. Guidash’s testimony (Ex. 1002 ¶¶ 231–232), that one of skill in the art would understand that the sensor of Asano includes photodiodes with p-n junction, as discussed above. Patent Owner provides an explanation of MOS capacitors and argues that a “MOS capacitor CCD has no p-n junction” (Prelim. Resp. 25–26), but we discern no portion of Asano itself that contradicts Mr. Guidash’s testimony that Asano includes photodiodes with p-n junctions. At this stage of the proceeding, we credit the testimony of Mr. Guidash in this regard.

Based on the evidence now before us, we are persuaded that the evidence supports a finding that Asano teaches the claimed “second conductivity type first semiconductor layer.”

First Conductivity Type Second Semiconductor Layer

Patent Owner also argues that Asano does not teach or suggest the claimed “first conductivity type second semiconductor layer.” Prelim. Resp. 27–29. Patent Owner again argues that Figure 1 of Asano is “more likely” a MOS capacitor, and that “MOS capacitors do not have p-n junctions.” Id. at 28. As discussed above, based on the evidence now before us, this argument is not persuasive.
Patent Owner also argues that Petitioner has not shown the n-type layer (upon which Petitioner relies as teaching the claimed second semiconductor layer) is “necessarily present.” *Id.* at 29. Petitioner, however, has not argued that the n-type layer is inherent in Asano, but rather, argues that that it would have been obvious to include an n-type layer in the p-type well of Asano in order to form a p-n junction. Pet. 42 (citing Ex. 1002 ¶¶ 231–232).

Based on the evidence now before us, we credit the testimony of Mr. Guidash in this regard, and are persuaded that the evidence supports a finding that Asano teaches the claimed “first conductivity type second semiconductor layer.”

**Conclusion**

We have considered Petitioner’s arguments and evidence in light of Patent Owner’s arguments presented in its Preliminary Response. Based on the record now before us, we determine that the information presented shows a reasonable likelihood that Petitioner would prevail in showing that claims 1 and 2 would have been obvious in view of Asano.

**Obviousness in View of Asano and Shibayama — Claims 3 and 4**


Claim 3 depends from claim 1, and recites “a first conductivity type third semiconductor layer formed in the semiconductor substrate around the through electrode.” Ex. 1001, 16:27–31. Claim 4 depends from claim 3,
and recites “the third semiconductor layer is formed from the main surface of the semiconductor substrate to another surface of the semiconductor substrate opposite to the main surface of the semiconductor substrate.” Id. at 16:32–36. Petitioner relies on Shibayama as teaching these claim features. Pet. 46–49.

According to Petitioner, both Asano and Shibayama recognize that damage may result from forming through holes. Pet. 47 (citing Ex. 1006 ¶ 43; Ex. 1002 ¶¶ 75, 253); see Ex. 1005 ¶¶ 23, 76. Asano further recognizes that such damage can reduce sensor performance, and that imaging sensors are “extremely sensitive to damage and defects.” Ex. 1006 ¶ 43; see Pet. 47. Petitioner notes that “[t]o alleviate such damage, Shibayama proposes forming N-type regions 125 and/or the N⁺-type layers 25 along the wall faces of the through holes.” Pet. 47 (citing Ex. 1002 ¶ 75); see Ex. 1005 ¶¶ 23, 50–51, 76.

Petitioner asserts that “[i]t would also have been obvious to form a semiconductor layer, such as the N-type high impurity concentration regions 125 or N⁺-type layers 25 of Shibayama, around the wall surfaces of the through holes disclosed in Asano.” Pet. 46–47. According to Petitioner, “[t]his would have reduced performance degradation caused by issues such as leakage or dark currents.” Id. at 47 (citing Ex. 1002 ¶ 255). It also would “trap undesirable carriers.” Id. (citing Ex. 1002 ¶¶ 255–256).

Petitioner argues that Asano, as modified, would include the claimed “first conductivity type third semiconductor layer formed in the semiconductor substrate around the through electrode,” as recited in claim 3. Pet. 48. Petitioner further argues that “it would have also been obvious to form the layers from the main surface of the substrate to an opposite surface
as disclosed by Shibayama,” and as required by claim 4. *Id.* at 48–49 (citing Ex. 1002 ¶¶ 259, 261).

Based on the evidence now before us, we are persuaded that Petitioner’s proposed modification is the “combination of a known imaging device (Asano Fig. 1) with a known solution (forming an N-type semiconductor layer or region around through electrodes) to address an issue (reduce the impact of common issues such as leakage current and dark current) well-understood by those with ordinary skill in the art.” *Pet.* 48. We further are persuaded that the modification was well within the ordinary skill in the art to implement and would have yielded no unpredictable results. *KSR*, 550 U.S. at 416; see *Pet.* 48 (citing Ex. 1005 ¶¶ 43, 85; Ex. 1006 ¶ 48; Ex. 1002 ¶ 257; Ex. 1001, 14:35–37), 49 (citing Ex. 1005 ¶ 23; Ex. 1002 ¶¶ 261–262).

Accordingly, we determine that the information presented shows a reasonable likelihood that Petitioner would prevail in showing that claims 3 and 4 would have been obvious in view of Asano and Shibayama.

*C. Grounds Based, At Least in Part, on Yanagida*

Petitioner asserts that claims 1 and 2 are unpatentable under 35 U.S.C. § 103 as obvious in view of Yanagida. *Pet.* 2, 50–57. Petitioner further asserts that claims 3 and 4 are unpatentable under 35 U.S.C. § 103 as obvious in view of Yanagida in combination with Holm. *Id.* at 2, 57–60. In its Preliminary Response, Patent Owner argues that Yanagida does not disclose several features of independent claim 1. *Prelim. Resp.* 29–36. We have reviewed the parties’ contentions and supporting evidence in the current record, and, for the reasons explained below, determine that the
information presented does not show a reasonable likelihood that Petitioner would prevail on these asserted grounds.

1. **Summary of Yanagida**

Yanagida relates to a solid-state image pickup device. Ex. 1008, Abstract. Figure 2 of Yanagida is reproduced below.

![Figure 2](image.png)

Figure 2 is a sectional view of an image sensor according to an embodiment of Yanagida. *Id.* ¶ 23. The device of Yanagida includes image pickup region 41, optical black region 42, and pad region 43. *Id.* ¶ 24. Photoelectric conversion elements 7, including n-type charge accumulation region 8 and p-type positive charge accumulation region 9, are formed in the semiconductor substrate 4 (a single crystal silicon layer), in image pickup region 41. *Id.* ¶ 25. Wiring layer 13 is formed in insulating layer 15, which is formed on one face of single crystal silicon layer 4. *Id.* ¶ 29. Wiring 26 and electrode layer 20 also are formed in insulating layer 15 “on the same plane as for the wiring 131,” which is part of wiring layer 13. *Id.* ¶ 33. “[C]onductive material layer 25 is formed . . . from the back face side to the
front face side in the semiconductor well region 6 reaching the wiring 26 formed in the insulating layer 15 on the front face side of the semiconductor well region 6.” *Id.* ¶ 36.

2. *Analysis*

Petitioner’s annotated versions of Figures 1 and 2 of Yanagida (Pet. 51–52) are reproduced below.
Figures 1 and 2 are a schematic plan view and a sectional view, respectively, of an image sensor according to an embodiment of Yanagida. Ex. 1008 ¶ 23. Petitioner’s annotations illustrate the proposed mapping of Yanagida to recited features of claim 1, shown in the following chart.

<table>
<thead>
<tr>
<th>Claim Element</th>
<th>Petitioner’s Mapping to Yanagida</th>
</tr>
</thead>
<tbody>
<tr>
<td>first conductivity type semiconductor substrate</td>
<td>single crystal silicon layer 4 (boxed in red, Fig. 2)</td>
</tr>
<tr>
<td>main surface [of the substrate]</td>
<td>front face side of layer 4 (denoted by dashed red line, Fig. 2)</td>
</tr>
<tr>
<td>imaging region</td>
<td>image pickup region 41 (highlighted in yellow, Fig. 1) with photoelectric conversion elements 7 (boxed in green, Fig. 2)</td>
</tr>
<tr>
<td>peripheral circuit region</td>
<td>pad region 43 (highlighted in blue, Fig. 1)</td>
</tr>
<tr>
<td>second conductivity type first semiconductor layer</td>
<td>charge accumulation region 8 (highlighted in blue, Fig. 2), comprising an N-type semiconductor region</td>
</tr>
<tr>
<td>first conductivity type second semiconductor layer</td>
<td>positive charge accumulation region 9, comprising a high concentration P-type semiconductor region (highlighted in purple, Fig. 2)</td>
</tr>
<tr>
<td>through electrode</td>
<td>conductive material layer 25 (highlighted in brown, Fig. 2)</td>
</tr>
<tr>
<td>pad portion</td>
<td>electrode layer 20 and wiring 26 (both highlighted in green, Fig. 2)</td>
</tr>
<tr>
<td>side insulating film</td>
<td>insulation (highlighted in blue, Fig. 2) between conductive material layer 25 and semiconductor well region 6</td>
</tr>
</tbody>
</table>
Notwithstanding whether we agree with Petitioner’s mapping of the other elements,9 we are not persuaded electrode layer 20 and wiring 26, upon which Petitioner relies for teaching the claimed pad portion, are formed on the alleged main surface of the semiconductor substrate, as required by claim 1. Instead, electrode layer 20 and wiring 26 are formed “in the insulating layer 15,” and, thus, are separated from the surface of layer 4 upon which Petitioner relies for teaching the claimed main surface.

Ex. 1008 ¶¶ 33, 59; see also id. ¶ 62 (describing etching off layer 4 and insulating layer 15 for forming opening 21 to reach electrode 20).

Accordingly, we are not persuaded that Petitioner has demonstrated a reasonable likelihood of success in showing that claims 1 and 2 would have been obvious in view of Yanagida, or that claims 3 and 4 would have been obvious in view of Yanagida and Holm.

9 Patent Owner argues that several features are missing from Yanagida, including the claimed “first conductivity type semiconductor substrate” (Prelim. Resp. 29–32), the substrate “having the imaging region and the peripheral circuit region on a main surface thereof” (id. at 32–35), “a peripheral circuit region formed on a main surface of the semiconductor substrate” (id. at 35), and “a pad portion formed on the main surface of the semiconductor substrate” (id. at 36). Patent Owner also takes issue with Petitioner’s construction of “a main surface,” calling it “an overly broad and manipulated interpretation” (id. at 32–33). Because our determination with respect to the claimed “pad portion” is dispositive to the grounds based on Yanagida, we need not address Patent Owner’s other arguments for purposes of this Decision.
D. Grounds Based, At Least In Part, on Admitted Prior Art

Petitioner asserts that claim 1 is unpatentable under 35 U.S.C. § 102 as being anticipated by APA alone. Pet. 2, 15–20. 35 U.S.C. § 311(b) provides that “[a] petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications” (emphasis added). Further, 37 C.F.R. § 42.104(b)(4) provides that the petition “must specify where each element of the claim is found in the prior art patents or printed publications relied upon” (emphasis added). This ground, which does not identify any patents or printed publications, fails to comply with Section 311(b) or Rule 42.104(b)(4). Accordingly, we decline to institute an inter partes review of claim 1 as anticipated by APA.

Petitioner further asserts that dependent claims 2–4 are unpatentable under 35 U.S.C. § 103 as obvious in view of APA in combination with Shibayama. Pet. 2, 21–34. Because this ground incorporates its arguments with respect to independent claim 1, on which we do not institute review, we

---

10 Patent Owner argues that the portions of the Specification asserted by Petition to be “admitted prior art,” are not actually prior art. Prelim. Resp. 14–18. Because we do not institute on this ground, we need not resolve this issue for purposes of this Decision.

11 Petitioner cites Intri-Plex Techs., Inc. v. Saint-Gobain Performance Plastics Rencol Ltd., Case IPR2014-00309, slip op. at 21 n.8 (PTAB Mar. 23, 2014) (Paper 83) to support its assertion that “[a]dmitted prior art is available for use in an inter partes review.” Pet. 15. We note, the cited previous Board decision is not precedential and is not binding on this panel. Further, in Intri-Plex, the asserted ground also included a U.S. Patent and the panel relied on the APA as “probative evidence under the Graham factor directed to the level of skill in the art rather than the Graham factor directed to scope and content of the prior art.” Intri-Plex, slip op. at 21 n.8.
exercise our discretion and decline also to institute an *inter partes* review with respect to claims 2–4. *See* 37 C.F.R. § 42.108(a).

III. CONCLUSION

For the foregoing reasons, we institute an *inter partes* review of claims 1–4. At this preliminary stage in the proceeding, we have not made a final determination with respect to the patentability of any challenged claim or the construction of any claim term.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1–4 of the U.S. Patent No. 8,030,724 B2 on the following grounds:

Claims 1 and 2 under 35 U.S.C. § 103(a) as obvious in view of Asano; and

Claims 3 and 4 under 35 U.S.C. § 103(a) as obvious in view of Asano and Shibayama;

FURTHER ORDERED that no other ground of unpatentability is authorized for this *inter partes* review; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.
IPR2016-00940
Patent 8,030,724 B2

PETITIONER:
Matthew A. Smith
Zhuanjia Gu
TURNER BOYD LLP
smith@turnerboyd.com
gu@turnerboyd.com

PATENT OWNER:
Terry Saad
Nicholas Kliewer
BRAGALONE CONROY PC
tsaad@bcpc-law.com
nkliwer@bcpc-law.com