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Paper No. 43
Entered: June 5, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

INNOVATIVE MEMORY SYSTEMS, INC.,
Patent Owner.

Case IPR2016-00323
Patent 7,495,953 B2

Before KARL D. EASTHOM, JAMES B. ARPIN, and KEVIN W. CHERRY, *Administrative Patent Judges*.

CHERRY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a); 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Micron Technology, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting institution of *inter partes* review of claims 1, 2, 8, and 9 of U.S. Patent No. 7,495,953 B2 (Ex. 1001, "the '953 patent"). Innovative Memory Systems, Inc. ("Patent Owner") filed a Preliminary Response (Paper 9, "Prelim. Resp."). Pursuant to 35 U.S.C. § 314, we instituted this trial ("Decision to Institute") as to each of the challenged claims of the '953 patent. Paper 11 ("Dec.").

After the Decision to Institute, Patent Owner filed a Patent Owner Response (Paper 26, "PO Resp.") and Petitioner filed a Reply to the Patent Owner Response (Paper 30, "Pet. Reply"). An oral hearing was held March 23, 2017, in this matter. A transcript of the oral hearing has been entered into the record. Paper 42 ("Tr.").

Petitioner relies on the testimony of Dr. Vivek Subramanian (Ex. 1003 ("Subramanian Declaration") & Ex. 1010 ("Subramanian Reply Declaration")) in support of its contentions. Patent Owner relies on the testimony of Vijay K. Madisetti, Ph.D. (Ex. 2001 ("Madisetti Declaration") in support of its contentions.

Patent Owner filed a Motion to Exclude certain evidence. Paper 35 ("Mot. Exclude"). Petitioner filed an opposition. Paper 38 ("Opp."). Patent Owner filed a reply. Paper 39 ("PO Reply").

Patent Owner also filed a Motion for Observations on Cross Examination of Vivek Subramanian, Ph.D. Paper 36 ("Obs."). Petitioner filed a response. Paper 37 ("Obs. Resp."). We have reviewed and

considered Patent Owner's observations and Petitioner's response in arriving at our Final Written Decision in this case.

We have jurisdiction under 35 U.S.C. § 6(b). This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims. Based on the record before us, Petitioner has demonstrated, by a preponderance of the evidence, that claims 1, 2, 8, and 9 of the '953 patent are unpatentable.

B. Related Proceedings

According to the parties, the '953 patent is involved in, at least, the following lawsuit: *Innovative Memory Sys., Inc. v. Micron Tech., Inc.*, 14-cv-1480 (D. Del.). Pet. 2.

Petitioner filed a number of other petitions challenging the patentability of certain subsets of claims in the following patents owned by Patent Owner: (1) U.S. Patent No. 6,169,503 B1 (Case IPR2016-00320); (2) U.S. Patent No. 7,045,849 B2 (Case IPR2016-00322); (3) U.S. Patent No. 7,886,212 B2 (Case IPR2016-00324) (Institution Denied); (4) U.S. Patent No. 7,000,063 B2 (Case IPR2016-00325) (Institution Denied); (5) U.S. Patent No. 6,324,537 B1 (Case IPR2016-00326) (Terminated, Adverse Judgment Requested by Patent Owner); (6) U.S. Patent No. 7,085,159 B2 (Case IPR2016-00327) (Terminated, Adverse Judgment Requested by Patent Owner); and (7) U.S. Patent No. 6,901,498 B2 (Case IPR2016-00330). *See* Pet. 2–3.

C. The References

Petitioner relies upon the following references:

Chen	US 5,867,429	Feb. 2, 1999	Ex. 1005
Harari	US 5,297,148	Mar. 22, 1994	Ex. 1006

D. The Asserted Ground of Unpatentability

We instituted this proceeding based on the following ground of unpatentability: Claims 1, 2, 8, and 9 as unpatentable as obvious under 35 U.S.C. § 103(a) over Chen and Harari.

E. The '953 Patent

The '953 patent is titled "System for Configuring Compensation" and issued February 24, 2009. Ex. 1001, [12], [45]. The '953 patent generally relates to a system for "reducing the effect of coupling between adjacent floating gates" of a non-volatile storage. Ex. 1001, 3:6–7. The system has a managing circuit configured to compensate for floating gate coupling during either programming or reading of the non-volatile storage elements. *Id.* at 3:13–24. The '953 patent explains that EEPROM and flash memory, two common types of non-volatile memory, "utilize a floating gate that is positioned above and insulated from a channel region in a semiconductor substrate" to store data. *Id*. at 1:41–43. "The floating gate is positioned between the source and drain regions" of a memory cell, and a "control gate is provided over and insulated from the floating gate." *Id.* at 1:43–45. One or more bits of data may be stored in a flash memory cell by programming or erasing the memory cell to set the threshold voltage of the memory cell to a programmed state. *Id.* at 1:65–2:9. The threshold voltage of the memory cell "is controlled by the amount of charge that is retained on the floating gate." *Id.* at 1:45–47.

The '953 patent explains that, at the time of the invention, it was known in the prior art that "[s]hifts in the apparent charge stored on a floating gate can occur because of the coupling of an electric field based on the charge stored in adjacent floating gates." *Id.* at 2:10–15. Floating-gate

coupling may occur between sets of adjacent memory cells. *Id.* at 2:26–28, 2:41–43. After the memory cells are programmed,

> the charge level read from the first memory cell appears to be different than programmed because of the effect of the charge on the adjacent memory cells being coupled to the first memory cell. The coupling from adjacent memory cells can shift the apparent charge level being read a sufficient amount to lead to an erroneous reading of the data stored.

Id. at 2:34–40.

The ’953 patent teaches compensating for floating gate coupling during reading by adding “offset” voltages to the read reference voltages that are used to read the memory cells. *Id.* at 23:22–37. The offset values are intended to compensate for increased apparent threshold voltages that result from floating gate coupling. *Id.* The ’953 patent also teaches compensating for floating gate coupling during programming by adjusting the threshold voltage at the time of programming the cell, i.e., providing a threshold voltage less than the target threshold voltage. *Id.* at 24:5–40.

F. Illustrative Claim

Claim 1 is the only independent claim of the ’953 patent challenged in this Petition. Each of claims 2, 8, and 9 directly depends from claim 1. Claim 1 is illustrative of the subject matter in this proceeding and is reproduced below.

> 1. A non-volatile storage system, comprising:
>
> a plurality of non-volatile storage elements; and
>
> a managing circuit in communication with said non-volatile storage elements, said managing circuit configures said non-volatile storage system to either compensate for floating gate coupling during reading or compensate for floating gate coupling during programming, based on said configuring said managing system causes compensation for coupling during reading of said

> non-volatile storage elements if said non-volatile storage system is configured to compensate for floating gate coupling during reading and causes compensation for coupling during programming of said non-volatile storage elements if said non-volatile storage system is configured to compensate for floating gate coupling during programming.

Id. at 30:2–21, 50–57.

II. CLAIM CONSTRUCTION

In an *inter partes* review, the Board gives claim terms in an unexpired patent their broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable interpretation standard, and absent any special definition, claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). "Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification and prosecution history." *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1062 (Fed. Cir. 2016).

As a first step in our analysis, we determine the meaning of the claims. Only terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

In the Decision to Institute, we preliminarily construed one claim term found in all of the challenged claims. The claim term and our preliminary construction are reproduced in the table below:

Claim Term	Claim Construction in the Decision to Institute
"managing circuit"	"one or more components, other than a memory cell array, capable of configuring a non-volatile storage system to compensate for floating gate coupling during programming or reading" (Dec. 7)

Neither party objects to this construction. *See* PO Resp. 12–13 (adopting construction). Having reviewed all of the evidence at trial, we maintain this construction. In the Decision to Institute, we noted that the parties appeared to dispute the terms "compensation during programming" and "configures." *See* Dec. 10 n.1 (discussing "configures"), 12–14 (discussing "programming"). We discuss these terms in detail below.

A. "configures"

All of the challenged claims require the "managing circuit configures." Ex. 1001, 30:2–21, 30:50:57. In the preliminary proceeding, neither party requested that we construe the term "configures."

In the Patent Owner Response, Patent Owner now proposes that we construe the term "configures," in accordance with its plain and ordinary meaning, to mean "[t]o set up or initialize the functionality of a device in a particular manner so that that functionality thereafter becomes available/unavailable for use when it is setup to allow/disallow it." PO Resp. 29 (citing Ex. 2001 ¶ 104). According to Dr. Madisetti, a device can be "configured" either at the time of manufacturing based on a choice made at the time of manufacture *or* it can be "'configurable' such that after it is

manufactured, the functionality that is available for use may be changed." *Id.* at 29–30. Patent Owner contends that configurability after manufacturing is

> typically done using circuitry in the device that reads an adjustable parameter, such as a stored flag or the state of a switch, which specifies a particular functionality or manner of operation, and then changes the functionality of the device that is available for use thereafter based on the read adjustable parameter.

Id. at 30.

In its Reply, Petitioner contends that the proper construction of "configure" is "to initialize a device so that it operates in a particular way." Pet. Reply 15–16. Petitioner submits that this construction, based on a definition in the *IEEE Dictionary*, represents the broadest reasonable construction of the term. Pet. Reply 19. Petitioner argues that Patent Owner improperly limits the definition with the additional requirements. *Id.* For example, Petitioner asserts that Patent Owner's requirements that the configuration of the device makes "functionality . . . available/unavailable for use" and that to be "setup to allow/disallow it" in the field is improper. *Id.* at 19–20.

We agree with Petitioner that Patent Owner improperly seeks to narrow the construction of this term. There is no contention by either party that the Specification of the '953 patent defines or limits the plain and ordinary meaning of "configures." In addition, our own review of the Specification has failed to locate any definition of the term or disclaimer of the term's scope. The only support that Patent Owner cites for its definition is Dr. Madisetti's testimony. *See* PO Resp. 29 (citing Ex. 2001 ¶ 104). But the only support cited by Dr. Madisetti is the *IEEE Dictionary*. *See* Ex. 2001 ¶ 104 (citing Ex. 2004, 11). The *IEEE Dictionary* definition

offered by Patent Owner defines the term as "[t]o initialize a device so that it operates in a particular way." Ex. 2004, 11. Petitioner accepts this definition as the plain and ordinary meaning. Pet. Reply 19. However, this definition does not contain support for Patent Owner's additional requirement "that functionality thereafter becomes available/unavailable for use when it is setup to allow/disallow it." Without additional support from the intrinsic evidence, we decline to read in additional limitations into the plain and ordinary meaning for this term as evidenced by the dictionary definition. On the contrary, we find that this dictionary definition is consistent with the use of that term in Specification, which use "configure" in the plain and ordinary sense of the term. *See, e.g.*, Ex. 1001, 28:12–29:55 (discussing various embodiments where there are different options for "configuring" the memory). Thus, we determine that the broadest reasonable interpretation of "configures" consistent with the Specification is "[t]o initialize a device so that it operates in a particular way." Ex. 2004, 11 (definition of "configure").

B. "compensation during programming"

The phrase "compensation during programming" is found in independent claim 1, and through dependency in all of the other challenged claims. In our Decision to Institute, we did not expressly construe the phrase "compensation during programming." We did determine, however, that the term—"programming"—"broadly refers to the step of writing and reading (verifying) information on the storage element." Dec. 13. In other words, we determined that "programming," as it was used in the '953 patent, was broad enough to encompass the entire programming process, including any verification reads performed as part of that process. *See id.* at 12–13. Patent

Owner does not challenge this determination that the term "programming" is broad enough to encompass a "programming process." *See* Tr. 20:9–28:14. Instead, Patent Owner now argues that "compensation during programming" must be done during the incremental step pulse programming ("ISPP") process shown in Figures 11 and 23 of the '953 patent. *See id.*; *see also* PO Resp. 36–37 (describing and defining ISPP process). Patent Owner does not contend that there is an explicit definition or disclaimer that limits the term's scope, but instead argues that because ISPP is the only process disclosed in the Specification of the '953 patent, the term must be limited to the ISPP process. *Id.*

Petitioner disagrees that "programming" is so limited. Pet. Reply 4–7. Petitioner argues that Patent Owner is attempting to limit the claims to the preferred embodiment without any showing of a disclaimer or definition in the Specification. *Id.* at 5–6.

We agree with Petitioner that the claims should not be limited to the specific ISPP process. As Petitioner explains and Patent Owner concedes, there is no express definition or disclaimer of "programming" in the Specification. Pet. Reply 4–7; Tr. 24:1–15. Instead, Patent Owner's argument is based on its contention that the Specification only describes ISPP, and, therefore, must be limited to that programming process. *See* Tr. 20:9–28:14. We do not agree. The mere fact that the Specification describes only one programming process embodiment is insufficient to limit the claims to that process. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc) ("[W]e have expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment."); *see also Kara Tech.*

Inc. v. Stamps.com Inc., 582 F.3d 1341, 1348 (Fed. Cir. 2009) ("The patentee is entitled to the full scope of his claims, and we will not limit him to his preferred embodiment or import a limitation from the specification into the claims."); *Liebel–Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) ("[T]his court has expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment."). Indeed, "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Liebel–Flarsheim*, 358 F.3d at 906 (quoting *Teleflex Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002)).

Here, Patent Owner has not identified any such words or expressions of manifest exclusion or restriction. On the contrary, the language of the Specification is clear that the process described is not intended to be limiting. *See* Ex. 1001, 4:29–30 (describing Figure 23 as "a flow chart describing one embodiment of a programming process"), 4:5–6 (describing Figure 11 as "a flow chart describing one embodiment of a process for programming non-volatile memory"), 16:39–40 ("FIG. 11 is a flow chart describing one embodiment of a method for programming non-volatile memory."), 25:31–33 ("FIG. 23 is a flowchart describing one embodiment of a process for programming according to the graphs of FIGS. 21 and 22."). Thus, we decline to limit "compensation during programming" to only the ISPP programming process.

III. ANALYSIS

A. Obviousness of Claims 1, 2, 8, and 9 over Chen and Harari

Petitioner asserts that a combination of the teachings of Chen and Harari would have rendered the subject matter of claims 1, 2, 8, and 9 obvious to one of ordinary skill in the art at the time of the invention. Pet. 36–52. The Petition includes discussion identifying where Chen and Harari allegedly teach or suggest the limitations of each challenged claim. *Id.*

1. Chen (Ex. 1005)

Chen, titled "High Density Non-Volatile Flash Memory Without Adverse Effects of Electric Field Coupling Between Adjacent Floating Gates," discloses a system utilizing EEPROM storage elements and a managing circuit that compensates for floating gate coupling. Ex. 1005, 3:35–43, 7:11–53, 8:6–28, 8:34–37. The main components of Chen are illustrated in Figure 2, which is reproduced below:

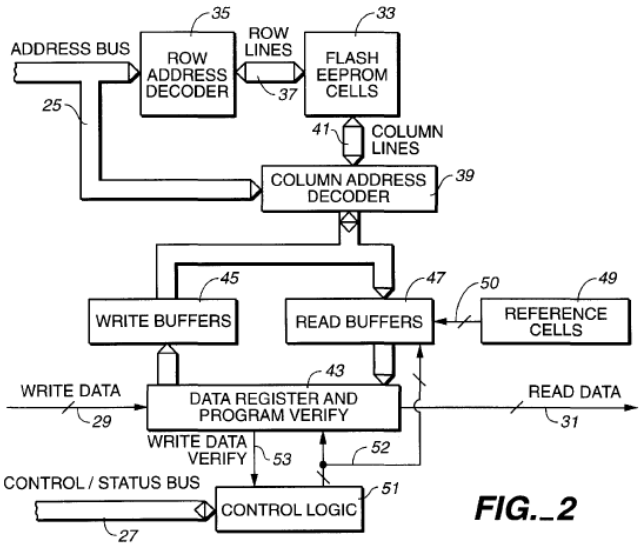

FIG._2

Figure 2 is a block diagram of the salient components of the flash EEPROM memory array. The flash EEPROM memory array includes decoders (35 and 39), a read/write circuit (43, 45, and 47), a controller (27), and control circuitry (51). *Id.* at 3:57–4:22.

When reading a memory cell, a compensation technique is initiated by first reading all of the memory cells that are field coupled with the cell being read. *Id.* at 7:44–45. A number related to either the floating gate voltage or the state of each coupled cell then is multiplied by the coupling ratio between the cells. *Id.* at 7:46–48. The multiplied readings then are combined in order to determine the collective effect of the adjacent cells on each of the cells of the addressed row being read. *Id.* at 8:16–19. The threshold current breakpoint levels then are shifted for each of the addressed cells by an amount that compensates for the voltage couple from adjacent cells. *Id.* at 8:22–26. The current read from the cell then is compared with the adjusted current breakpoint levels in order to accurately read its state. *Id.* at 8:26–28. The same compensating technique is used as part of the programming process when the states of the cells being programmed are individually read in order to verify that they have been programmed to the desired states. *Id.* at 8:34–37.

2. Harari (Ex. 1006)

Harari, titled "Flash EEPROM System," describes a system of Flash EEPROM memory chips with controlling circuits serving as non-volatile memory. Ex. 1006, Abstract. Among other things, Harari discloses a managing circuit using adaptive error correction. *Id.* at 8:43–53. The adaptive error correction can take place during a read operation (*id.* at 8:35–

36) or during a programming operation (*id.* at 8:33–35). *Id. at* 9:16–22, 11:49–60.

3. Level of Ordinary Skill in the Art

Petitioner contends that

> [a] person of ordinary skill in the art with respect to the technology described in the 953 Patent would be a person with a Bachelor of Science degree in electrical engineering, computer engineering, computer science or a closely related field, along with at least 2–3 years of experience in the development and use of memory devices. An individual with an advanced degree in a relevant field would require less experience in the design of memory devices.

Pet. 19 (citing Ex. 1003 § IV). Petitioner's assessment of the level of ordinary skill in the art is supported by Dr. Subramanian's testimony. Ex. 1003 ¶¶ 17–19. Patent Owner does not contest Petitioner's assessment of the level of ordinary skill in the art as of the date of the invention.

Accordingly, for the purposes of this Decision, we adopt Petitioner's proposed level of ordinary skill in the art.

4. Discussion

Claim 1

"A non-volatile storage system, comprising:"

With respect the preamble of claim 1, we find that Petitioner has shown adequately that Chen accounts for this limitation. *See* Pet. 36–37. Specifically, we agree with Petitioner that Chen discloses a non-volatile storage system. Ex. 1005, 2:56–62, Fig. 1.

"a plurality of non-volatile storage elements"

We further agree with Petitioner Chen accounts for this limitation. Pet. 37–40. Specifically, Chen discloses of a plurality of non-volatile

storage elements (21), which are EEPROM cell arrays that include decoders (35 and 39), a read/write circuit (43, 45, and 47), a controller (27), and control circuitry (51). Ex. 1005, Abstract, 1:26–29, 3:35–43, 3:57–4:7, 4:36–44, Figs. 1, 2, 3.

"a managing circuit in communication with said non-volatile storage elements, said managing circuit configures said non-volatile storage system to either compensate for floating gate coupling during reading or compensate for floating gate coupling during programming, based on said configuring said managing system causes compensation for coupling during reading of said non-volatile storage elements if said non-volatile storage system is configured to compensate for floating gate coupling during reading and causes compensation for coupling during programming of said non-volatile storage elements if said non-volatile storage system is configured to compensate for floating gate coupling during programming."

Petitioner submits that the combination of the teachings of Chen and Harari accounts for this limitation. Pet. 41–47. Specifically, Petitioner asserts that Chen discloses that the managing circuit configures the non-volatile storage system to compensate for floating gate coupling during reading. Pet. 41–44 (citing Ex. 1005, 3:57–4:22, 7:11–53, 8:6–28, Figs. 2, 9, 10). Petitioner also contends that Chen teaches that the compensation technique it describes using when reading also may be used to compensate for floating-gate coupling during programming. Pet. 42, 44 (citing Ex. 1005, 8:34–37).

Petitioner argues that, although Chen teaches a circuit capable of compensating on reading or a circuit capable of compensating on programming, Chen fails to account for a managing circuit that would enable or disable compensation. *Id.* at 45. For that aspect of the limitation, Petitioner turns to Harari. *Id*. at 45–47. Harari, Petitioner asserts, teaches a managing circuit that implements adaptive error correction that may apply

an error correction technique during reading and programming. Ex. 1006, 8:27–54. Petitioner alleges that the combination of the teachings of Chen and Harari would have led one of ordinary skill in the art to perform floating-gate coupling compensation *either* during reading *or* programming. Pet. 46–47.

As for the reason for combining the references, Petitioner provides several reasons why a person of ordinary skill would have combined the teachings of Chen and Harari. Pet. 34–35, 46–47. First, Petitioner submits that Chen expressly incorporates Harari by reference into its disclosure. *Id.* at 34. Second, Petitioner argues that the two references are in the same field and use the same system to solve the same problem. *Id.* Finally, Petitioner asserts that the combination would be applying a known technique to yield a predictable result. *Id.* In addition, Petitioner submits that Chen discloses that its compensation technique will have a negative impact on flash EEPROM performance during reading or programming. *Id.* at 46. Petitioner argues that Harari discloses a managing circuit to control a flash EEPROM that minimizes negative impacts on performance without compromising reliability by providing an error correction scheme that is selectively enabled. *Id.* at 46–47. Thus, Petitioner asserts that a person of ordinary skill would understand that the combination of these techniques would compensate for errors arising from floating gate coupling while minimizing negative performance impacts otherwise caused by Chen's compensation technique. *Id.* at 47.

Patent Owner challenges Petitioner's arguments on three main points. First, Patent Owner argues that the combination fails to account for a "managing circuit" that "configures" as recited by claim 1. PO Resp. 28–35.

Patent Owner and Dr. Madisetti contend that Harari does not disclose a managing circuit that configures the operation of the memory. *Id.* at 30. Instead, Patent Owner asserts that "Harari discloses a system that is hardwired to ***always*** function in a particular manner that may not be initialized or adjusted." *Id*. Patent Owner argues that "Harari's memory system has a fixed form that may not be adjusted before or after manufacture . . . [and] is thus not a configurable device. And Harari does not have a managing circuit that can configure the device so as to change its functionality." *Id.* (citing Ex. 2001 ¶ 108). Instead, Patent Owner asserts that Harari's system "responds via different paths in a computation/processing flow graph depending on the type of error encountered." *Id.* at 31. In other words, according to Patent Owner, the error correction is "always ON and available for use" and "it is not possible to switch Harari's error correction techniques ON and OFF." *Id.*

To the extent the dispute with respect to this term turns on the disagreement between the parties of the construction of "configures," we resolved that part of the dispute above. Instead of Patent Owner's narrow construction that includes a requirement that functionality become available or unavailable as a result of the configuring, we have adopted Petitioner's construction of "to initialize a device so that it operates in a particular way." *See supra*, § II.A. As explained below, under this construction, we agree with Petitioner that the combination of the teachings of Chen and Harari accounts for this limitation.

The parties largely agree on how Harari operates. *See* Pet. Reply 18–19; *compare* Pet. 45–46 *with* PO Resp. 29–31. Petitioner has shown, and Patent Owner does not dispute, the following: (1) Harari discloses an

adaptive approach to error correction that utilizes a two tier error correction approach (Ex. 1006, 8:27–53); (2) Harari uses traditional ECC at all times to correct for errors where possible and to detect errors that cannot be corrected through traditional ECC techniques (*id.* at 8:35–46); and (3) Harari discloses that the advanced error correction is used if and when a "hard error" is detected (*id.* at 8:46–49). As Dr. Subramanian testifies, Harari makes advanced error correction available in the field using a logical control path to choose whether or not to use advanced error correction based on the type of error detected. *See* Ex. 2003, 63:7–17 (noting the managing circuit is "mak[ing] a decision on whether to use it or not"). In addition, we find that Petitioner has shown that Harari teaches a managing circuit of a non-volatile storage system that sets up the storage system so it operates in a particular way—to use a two-tier adaptive error correction approach. Ex. 1010 ¶ 35 (citing Ex. 1003 ¶¶ 97–104).

In the proposed combination, the combined managing circuit teaching includes Harari's adaptive error correction approach in Chen's floating gate compensation technique. *See* Pet. 45–46. As the Petition explains, the advanced error correction scheme is enabled dynamically during *either* reading *or* programming to minimize impacts to the performance of the flash EEPROM without compromising reliability. *Id.* at 46. As Dr. Subramanian testifies, when the managing circuit teaching of Chen is modified in light of Harari, the storage device of Chen is initialized to operate using a similar adaptive error correction approach. Ex. 1010 ¶¶ 35, 36. Under this approach, the modified managing circuit teaching of Chen would use error correction techniques to detect floating-gate coupling errors in Chen's storage system, and then selectively enable floating-gate coupling

compensation *either* during reading *or* programming, but only when an error is detected. *Id.* Thus, the managing circuit would configure the memory system to either perform compensation during reading or during programming depending on the type of error encountered. *Id.* This type of setup is consistent with the configuring described in the Specification, where the managing circuit is configured at manufacture to operate a particular way. *See* Ex. 1001, 28:30–38.

As Dr. Subramanian persuasively testifies the combined system would obtain the benefit of enhanced reliability of the compensation techniques of Chen, while reducing the performance impact associated with those techniques. Ex. 1010 ¶ 36. As Dr. Subramanian explains, this combined managing circuit initializes the storage device, so that it operates in a particular way. *Id.* Dr. Subramanian testifies that, depending on the type of error detected, Harari makes a particular type of error correction available and makes the other type of error correction unavailable. *Id.* ¶ 40. As a result, the managing circuit of Harari initializes the functionality of the memory device, so that the advanced error correction functionality thereafter becomes available or unavailable for use. *Id.* We find Dr. Subramanian's testimony to be consistent with the references' teachings and consistent with the construction we have adopted. Thus, we give Dr. Subramanian's testimony substantial weight. Dr. Madisetti's testimony, on the other hand, relies on the inappropriately narrow construction we rejected above. Thus, we determine that Dr. Madisetti's testimony is entitled to less weight. In light of this determination and weighing the testimony and evidence presented by the parties, we find that Petitioner has shown that the

combination of the teachings of Chen and Harari accounts for the "managing circuit" that "configures."

Second, Patent Owner asserts that the combination of the teachings of Chen and Harari fails to account for compensation for floating gate coupling "during programming." *Id.* at 35–44. There is no dispute between the parties, and we find, that Chen teaches compensation for floating gate coupling during reading. *See* Pet. 42–44; PO Resp. 18–22 (discussing Chen's description of floating gate coupling during reading); Ex. 1005, 7:10–8:28; Ex. 1003, A-9–A-12. Petitioner points to the following disclosure of Chen as also teaching compensation "during programming": "The same compensating technique is used as part of the programming process when the states of the cells being programmed are individually read in order to verify that they have been programmed to the desired states." Ex. 1005, 8:34–37 (cited at Pet. 44) (emphasis omitted). In our Decision to Institute, we determined that "programming," as it is used in the challenged claims is broad enough to encompass the entire "programming process." Dec. 12–14. In its Patent Owner Response, Patent Owner no longer attempts to draw a distinction between "programming" and "programming process," but instead argues that Chen discloses using compensation for floating gate coupling in a programming process other than ISPP. *See* PO Resp. 36–43. However, as Patent Owner admitted in response to a question from Judge Arpin at the oral hearing, this argument turns on the adoption of Patent Owner's construction of "programming" that limits it to the ISPP process:

> JUDGE ARPIN: Counselor, going back to your discussion about the claim construction, if we disagree with you that programming is limited to ISPP, this argument doesn't work, isn't that correct?

> MR. FLYNN: If you would construe programming in the context of the claim, and in light of -- as disclosed by the claim in light of the specification, if you would still construe programming to be after ISPP, then that argument does not work, Your Honor, you are correct, because Chen discloses read compensation after ISPP. He describes it as part of the programming process.
>
> We can disagree whether one of ordinary skill in the art would actually consider at that point still to be part of programming or programming process, but at least he uses that language.
> *So you are absolutely correct, that if you construe the claim term programming, in light of the specification in the '953, to extend beyond ISPP, then this argument does not work.*

Tr. 36:19–37:15 (emphasis added). As we discussed above, we have determined that the broadest reasonable interpretation of "programming" is not limited to just the ISPP process. *See supra*, § II.B. Thus, without deciding whether Chen's compensation occurs during the ISPP process or after it, this argument is not persuasive. As Patent Owner acknowledges, Chen specifically refers to the compensation as occurring during its "programming process." *See* Tr. 36:19–37:15; Ex. 1005, 8:34–37. Thus, we find persuasive Petitioner's evidence and Dr. Subramanian's testimony on this point, and find that Petitioner has shown that Chen teaches "compensation during programming," as we have construed it. *See* Ex. 1003, A-12–A-13.

Finally, Patent Owner contends that there is no reason to combine Chen and Harari in the manner proposed by Petitioner. *Id.* at 45–46. We disagree. As Petitioner explains, Chen expressly incorporates by reference Harari, and teaches that Chen's error correction techniques may be used in memory systems employing Harari's managing circuit that configures adaptive error correction. *See* Ex. 1005, 3:51–56; Ex. 1003 ¶ 120. Moreover, as Dr. Subramanian explains, a person of ordinary skill would

have been motivated to apply Harari's adaptive error correction techniques to the floating gate coupling compensation method of Chen in light of Chen's teaching that compensation techniques have performance tradeoffs. Ex. 1003 ¶¶ 89, 122; Ex. 1005, 8:38–41. Dr. Subramanian further explained that a person of ordinary skill would have found it obvious to substitute the managing circuit of Harari into Chen to selectively enable the floating-gate coupling error correction of Chen selectively for either read or program operations because it is merely the use of known techniques to yield predictable results. Ex. 1003 ¶ 122.

Patent Owner and Dr. Madisetti argue that the combination would not be obvious because it would not yield predictable results, but their basis for this conclusion merely repeats their other arguments. PO Resp. 45–46. Dr. Madisetti's testimony based this unpredictability on three reasons:

> (1) Chen only teaches floating gate compensation during reading, and does not teach floating gate compensation during programming; (2) Chen mandates that Chen's compensation during reading is always used and cannot be turned ON and OFF; and (3) Harari mandates that ECC error correction of soft errors and cell replacement of hard errors are both always operational and cannot be turned ON and OFF.

Ex. 2001 ¶ 146. We are not persuaded that these reasons establish Dr. Madisetti's contention because they are either founded on questionable reasoning or based on requirements found only in claim constructions we rejected. For example, we have rejected Patent Owner's contention Chen fails to teach floating gate coupling during "programming." *See supra*, at 20–22. As for the second reason, neither Patent Owner nor Dr. Madisetti cites any support in Chen, and we have been unable to independently locate, anywhere in Chen that "mandates" that compensation during reading is

always used and cannot be turned ON and OFF. Moreover, even if Chen did "mandate" that compensation in its system always be used, Petitioner relies on the combination of the teachings of Chen and Harari, not on Chen alone. *See In re Urbanski*, 809 F.3d 1237, 1243–44 (Fed. Cir. 2016) (holding that combined process was not rendered inoperative where person of ordinary skill "would have been motivated to pursue the desirable properties taught by [one prior art reference], even at the expense of foregoing the benefit taught by [the second prior art reference]"). Finally, Patent Owner's requirement that Harari turn "ON" and "OFF" ECC error correction appears to be based on its construction for "configures" and arguments regarding the claim limitation "managing circuit" that "configures." Because we have found that Harari adequately discloses configuring, we do not agree with Patent Owner that whether Harari discloses turning "ON" and "OFF" ECC error correction is significant for the combination. In conclusion, because we determine that the three reasons underlying Dr. Madisetti's contention that the results would not be predictable are questionable, we decline to give substantial weight to Dr. Madisetti's testimony on this point. In contrast, we find that Dr. Subramanian's testimony is well-reasoned and supported by citations to the record and accord it substantial weight. In sum, weighing the evidence together, we find that Petitioner has shown adequately that a person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings of Chen and Harari in the manner proposed by Petitioner for the reasons stated by Dr. Subramanian. *See* Ex. 1003 ¶¶ 119–122.

Claim 2

Claim 2 depends from claim 1 and additionally recites "where: said non-volatile storage system is installed in a host and is in communication with a host." Ex. 1001, 30:18–21. Patent Owner does not separately argue the patentability of claim 2, apart from arguments we considered with respect claim 1. PO Resp. 46. We find that Petitioner has shown sufficiently that Chen accounts for this limitation. Ex. 1005, Fig. 1, 3:27–35, 3:48–50; Ex. 1003, A-20–A-22. As discussed above, we have found that Petitioner has shown sufficiently that Chen and Harari account for the remaining limitations of claim 1, and Petitioner has shown that a person of ordinary skill would have been motivated to combine the teachings of Chen and Harari in the manner suggested by Petitioner. Thus, we find that Petitioner has shown by a preponderance of the evidence that Chen and Harari would have rendered obvious claim 2.

Claim 8

Claim 8 depends from claim 1 and additionally recites "wherein: said non-volatile storage elements are NAND flash memory devices." Ex. 1001, 30:50–53. Patent Owner does not separately argue the patentability of claim 2, apart from arguments we considered with respect claim 1. PO Resp. 46. We find that Petitioner has shown sufficiently that Chen accounts for this limitation. Ex. 1005, Fig. 3, 2:63–65, 4:36–39, 4:65–67; Ex. 1003, A-23. As discussed above, we have found that Petitioner has shown sufficiently that Chen and Harari account for the remaining limitations of claim 1, and Petitioner has shown that a person of ordinary skill would have been motivated to combine the teachings of Chen and Harari in the manner suggested by Petitioner. Thus, we find that Petitioner has shown by a

preponderance of the evidence that Chen and Harari would have rendered obvious claim 8.

Claim 9

Claim 9 depends from claim 1 and additionally recites "wherein: said non-volatile storage elements are multi-state flash memory devices." Ex. 1001, 30:54–57. Patent Owner does not separately argue the patentability of claim 2, apart from arguments we considered with respect claim 1. PO Resp. 46. We find that Petitioner has shown sufficiently that Chen accounts for this limitation. Ex. 1005, Fig. 5, 1:7–12, 1:25–31, 1:37–39; Ex. 1003, A-24–A-25. As discussed above, we have found that Petitioner has shown sufficiently that Chen and Harari account for the remaining limitations of claim 1, and Petitioner has shown that a person of ordinary skill would have been motivated to combine the teachings of Chen and Harari in the manner suggested by Petitioner. Thus, we find that Petitioner has shown by a preponderance of the evidence that Chen and Harari would have rendered obvious claim 9.

B. Patent Owner's Motion to Exclude

We have reviewed Patent Owner's Motion to Exclude (Paper 35), Petitioner's Opposition to the Motion (Paper 38), and Patent Owner's Reply in Support of the Motion (Paper 39). Patent Owner moves to exclude certain paragraphs of the reply testimony of Dr. Subramanian (Ex. 1010 ¶¶ 41–44) and Exhibits 1011 and 1012. Paper 35. We did not rely on either the testimony to which Patent Owner objects or any of the exhibits identified in Patent Owner's motion. Accordingly, for these reasons, we *dismiss* Patent Owner's Motion to Exclude as *moot*.

IV. CONCLUSION

We determine that Petitioner has demonstrated, by a preponderance of the evidence, that claims 1, 2, 8, and 9 of the ’953 patent are unpatentable as obvious under 35 U.S.C. § 103(a) over Chen and Harari.

V. ORDER

Accordingly, it is:

ORDERED that, based on a preponderance of the evidence, claims 1, 2, 8, and 9 of the ’953 patent have been proven unpatentable;

FURTHER ORDERED that Patent Owner’s Motion to Exclude is *dismissed as moot*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of this Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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