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Paper 33
Entered: June 9, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

INNOVATIVE MEMORY SYSTEMS, INC.,
Patent Owner.

Case IPR2016-00322
Patent 7,045,849 B2

Before KARL D. EASTHOM, JAMES B. ARPIN, and KEVIN W. CHERRY, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner"), filed a Petition requesting *inter partes* review of claims 1–6 of U.S. Patent No. 7,045,849 B2 (Ex. 1001, "the '849 patent") under 35 U.S.C. §§ 311–319. Paper 1 ("Petition" or "Pet."). Innovative Memory, Inc. ("Patent Owner"), filed a Preliminary Response. Paper 9 ("Prelim. Resp."). On June 13, 2016, we instituted *inter partes* review of claims 1–6 of the '849 patent. Paper 11 ("Dec. on Inst."), 41–42.

Patent Owner then filed a Response (Paper 24 ("PO Resp.")), and Petitioner filed a Reply to the Patent Owner Response. Paper 25 ("Pet. Reply"). An Oral Hearing was held on March 23, 2017, and the record includes a transcript of the Oral Hearing. Paper 32 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision issues pursuant to 35 U.S.C. § 318(a). We determine that Petitioner has shown by a preponderance of the evidence that claims 1–6 of the '849 patent are unpatentable.

A. Related Proceedings

According to the parties, the '849 patent is involved in, at least, the following lawsuit: *Innovative Memory Sys., Inc. v. Micron Tech., Inc.*, 14-v-1480 (D. Del. 2014). Pet. 2; Paper 7, 1.

Petitioner filed a number of other petitions for *inter partes* review challenging the patentability of certain subsets of claims in the following patents owned by Patent Owner: (1) U.S. Patent No. 6,169,503 B1 (Case IPR2016-00320); (2) U.S. Patent No. 7,495,953 B2 (Case IPR2016-00323); (3) U.S. Patent No. 7,886,212 B2 (Case IPR2016-00324) (institution

denied); (4) U.S. Patent No. 7,000,063 B2 (Case IPR2016-00325) (institution denied); (5) U.S. Patent No. 6,324,537 B1 (Case IPR2016-00326) (terminated, adverse judgment requested by Patent Owner); (6) U.S. Patent No. 7,085,159 B2 (Case IPR2016-00327); and (7) U.S. Patent No. 6,901,498 B2 (Case IPR2016-00330). *See* Pet. 2–3; Paper 7, 1.

B. The '849 Patent

The '849 patent is entitled "Use of Voids Between Elements in Semiconductor Structures for Isolation" and was filed May 21, 2003, and issued May 16, 2006. Ex. 1001, [45] and [54]. The '849 patent generally relates "to the isolation of tightly packed elements in semiconductor structures, and, more specifically, to the electric field isolation of neighboring charge storage elements of non-volatile flash electrically erasable and programmable read-only-memory (flash EEPROM) cell arrays." Ex. 1001, 1:7–12. In particular, the '849 patent describes structures for reducing field coupling between adjacent memory cells by providing a "dielectric between them that contains a void extending a major part of the distance between the elements instead of the usual technique of making the dielectric solid throughout the entire space between charge storage elements." *Id.* at 4:20–24. Such a void reduces the capacitive coupling as compared to the imposition of a solid dielectric between elements, because air has a dielectric constant of about 1.0, which is lower than, for example, the dielectric constant of silicon dioxide (i.e., about 4.0) or silicon nitride (i.e., about 7.5). *Id.* at 4:24–34.

Figure 1 of the '849 patent, including our annotations, is reproduced below:

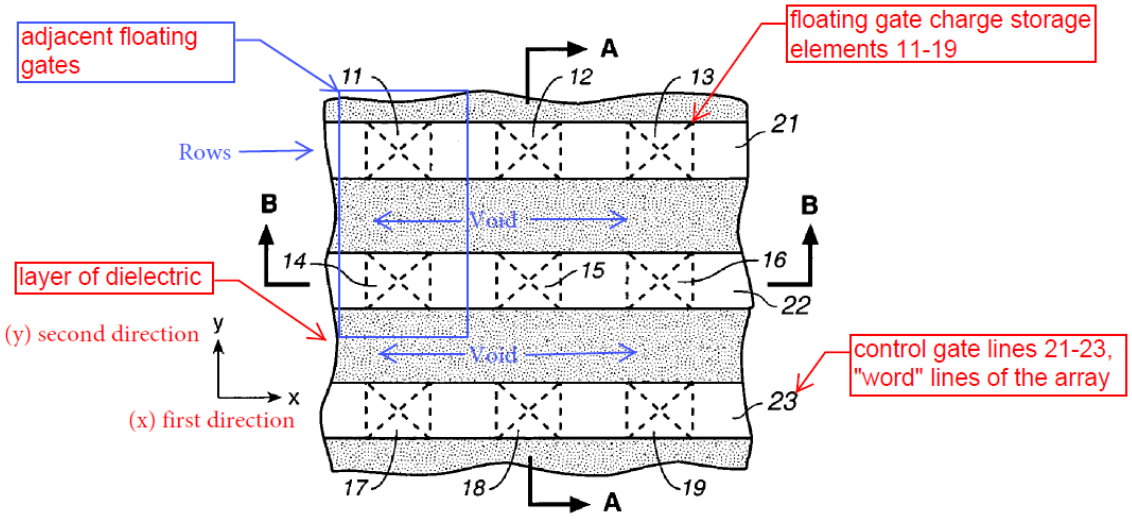


FIG._1

Figure 1 depicts a plan view representation of an array of floating gate memory cells regularly spaced in a first row direction and a second column direction on a semiconductor substrate. Ex. 1001, 5:37–41, 45–48. Control gates lines 21–23 extend across and are connected to memory cells arrayed in a row, and are spaced apart in the column direction, such that they are aligned with floating gates 11–19. *Id.* at 5:41–45. Adjacent floating gates, e.g., floating gates 11 and 14, may be subject to capacitive coupling or parasitic capacitance across the dielectric layer separating them. *Id*. at 4:55–58; *see id*. at 3:65–4:14.

Figure 4 of the ’849 patent, including our annotations, is reproduced below:

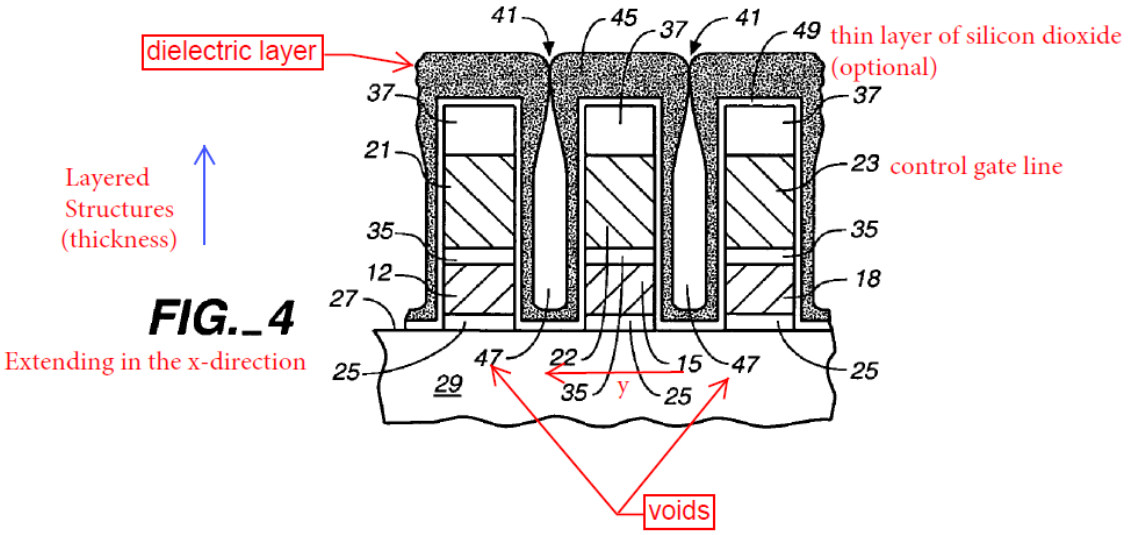


FIG._4

Figure 4 depicts the structure of the individual memory cells. In particular, Figure 4 is a cross-sectional view taken along line A-A of Figure 1. Ex. 1001, 5:19–21. Each memory cell is formed as a "self-aligned stack" of, for example, gate dielectric 25; floating gate charge storage elements 12, 15, or 18; inter-polysilicon layer 35; control gate 21, 22, or 23; dielectric layers 37 and 45; and optional dielectric layer 49. *Id.* at 6:4–39, 7:7–20. Independent claims 1 and 2, reproduced below (*see infra* Section I.C.), referred to "layered structures," which "includ[e] at least the charge storage elements and the control gates." Dielectric material 45 is formed between adjacent stacks while leaving void 47. *Id.* at 7:7–11. Thus, each self-aligned stack is separated by gas-filled void 47, having a dielectric constant of about 1.0. *Id.* at 7:38–41.[1]

> *In one embodiment, this isolation is formed in spaces between floating gates at the bottom of stacks of layers having a height of five, eight or more times the width of the spaces between the stacks.* The other layers in the stacks usually contain at least

[1] Because layer of dielectric material 45 generally is porous, the gases trapped in voids 47 are replaced over time with ambient gases, such as air. Ex. 1001, 7:41–46.

> one dielectric and a conductive control gate line. This 5:1, 8:1 or more cross-sectional aspect ratio of the spaces between the stacks allows a dielectric to be formed that extends downward into the spaces along sidewalls of the stacks but not filling the bottom segments of the spaces between the charge storage elements. Top portions of the spaces are filled with the dielectric, however, thereby leaving large voids sealed in the dielectric between the charge storage elements.

Ex. 1001, 4:35–47 (emphasis added). Independent claims 1 and 2 read on the embodiment wherein the spacing between memory cells is less than one fifth of the thickness or height of the memory cells, i.e., an aspect ratio of greater than 5:1. *Id.* at 9:50–53, 10:7–10; *see id.* at 6:46–48 (defining "aspect ratio" as "height divided by width in cross-section"). Dependent claim 5 reads on the embodiment wherein the spacing between memory cells is less than one eighth of the thickness or height of the memory cells, i.e., an aspect ratio of greater than 8:1. *Id.* at 10:26–29. However, the Specification of the '849 patent explains that

> [t]he aspect ratio is a result of process improvements allowing the shrinking of horizontal dimensions across the substrate causing the widths of the spaces 41 to be reduced without the height of the stacks forming the spaces necessarily being changed. The aspect ratio is also controlled, independent of the process resolution element size, by controlling the heights of the stacks without affecting operation of the resulting array, particularly by controlling the thickness of the top dielectric layer 37 or another dielectric layer that may be added on top of it.

Id. at 6:49–58. Thus, assuming all other values remain unchanged, the value of the aspect ratio increases as the horizontal spacing between adjacent memory cells decreases. *Id.* Moreover, the alleged purpose of these 5:1 and 8:1 aspect ratios is to allow a dielectric to be formed between the memory cells, which contains voids. *Id.* at 4:40–47.

Figure 3B of the '849 patent, including our annotations, is reproduced below:

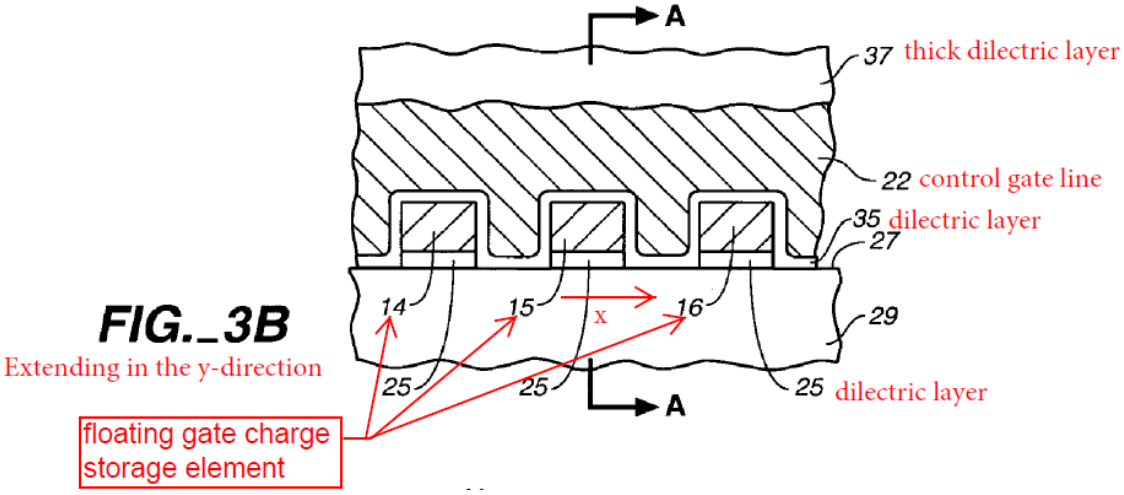


Figure 3B depicts providing shielding between adjacent floating gates 14 and 15 or 15 and 16 in the row or x direction by extending control gate line 22 downward between adjacent floating gates 14 and 15 or 15 and 16.

C. Illustrative Claim

Claims 1 and 2 are the challenged, independent claims of the '849 patent. Each of claims 3–6 directly depends from claim 2. Claims 1 and 2 are illustrative and are reproduced below with disputed limitations emphasized.

1. A non-volatile memory cell array formed on a semiconductor substrate, comprising:

an array of charge storage elements carried by the substrate,

conductive control gate lines elongated in a first direction across the charge storage elements and being separated in a second direction by a distance of separation of the charge storage elements in the second direction, the first and second directions being orthogonal with each other,

wherein layered structures including at least the charge storage elements and the control gates are separated in the second direction by distances that are *less than one-fifth of a thickness of the layered structures*,

dielectric material between the layered structures in the second direction that fill top portions of spaces therebetween while leaving voids between adjacent charge storage elements of the layered structures, and

wherein the charge storage elements are conductive floating gates and the elongated control gate lines extend downward between adjacent floating gates in the first direction.

2. A non-volatile memory cell array formed on a semiconductor substrate, comprising:

an array of charge storage elements carried by the substrate,

conductive control gate lines elongated in a first direction across the charge storage elements and being separated in a second direction by a distance of separation of the charge storage elements in the second direction, the first and second directions being orthogonal with each other,

wherein layered structures including at least the charge storage elements and the control gates are separated in the second direction by distances that are *less than one-fifth of a thickness of the layered structures*,

dielectric material between the layered structures in the second direction that fill top portions of spaces therebetween while leaving voids between adjacent charge storage elements of the layered structures, and

wherein the control gate lines include word lines extending in the first direction along rows of charge storage elements and the charge storage elements form, along columns in the second direction, series strings of a plurality of charge storage transistors.

Ex. 1001, 9:40–10:20 (emphases added).

D. Applied References, Document, and Declaration

Petitioner relies on the following references, document, and declaration in support of its asserted grounds of unpatentability.

Exhibit	References, Document, and Declaration
1002	File History '849 patent
1003	Declaration of Dr. R. Jacob Baker
1005	Patent No. US 6,720,612 B2 to Takeuchi ("Takeuchi"), filed Mar. 15, 2002; publ'd Sep. 19, 2002, issued Apr. 13, 2004
1006	Lee, Jae-Duk *et al.*, *Effects of Floating Gate Interference on NAND Flash Memory Cell Operation*, 23 IEEE ELECTRON DEVICE LETTERS 264–266 (May 2002) ("Lee")
1007	Japanese Unexamined Patent Application Publication No. JP 200-100976 A to Sato, publ'd Apr. 7, 2000 ("Sato")

Pet. vi.

The '849 patent issued from U.S. Patent Application No. 10/443,502, filed May 21, 2003. Ex. 1001 at [22]. Patent Owner does not contend that any of the applied references has an effective date later than May 21, 2003.

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

References	**Basis**	**Challenged Claims**
Takeuchi and Lee	35 U.S.C. § 103(a)	1–6
Sato and Lee	35 U.S.C. § 103(a)	1–6

II. ANALYSIS

A. Claim Interpretation

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable interpretation standard, claim terms are given their ordinary and

customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

In the Decision on Institution, we construed the terms: "thickness" (Claims 1–6) and "a single layer of dielectric" (Claim 6). Patent Owner did not dispute our construction of the term "thickness" in its Patent Owner Response, and we determine that the broadest reasonable interpretation of the term "thickness," as used in the claim phrase "thickness of the layered structures" (claims 1 and 2), is the "height of a layered structure as measured from the substrate," as proposed by Petitioner. *See* Tr. 15:21–16:5, Paper 13, 3 ("**The patent owner is cautioned that any arguments for patentability not raised in the response will be deemed waived.**"). As discussed below, Patent Owner contests our preliminary construction of the term "a single layer of dielectric."

1. "a single layer of dielectric" (Claim 6)

In the Decision on Institution, we determined that the broadest reasonable interpretation of the term "single layer of dielectric," consistent with the language of claims 2 and 6 and the Specification of the '849 patent, is "one layer of dielectric," which will fulfill the two recited structural relationships of claim 6: (1) fills top portions of the spaces and (2) leaves voids between adjacent stacks. Dec. on Inst. 11. In the Patent Owner Response, Patent Owner contends that our preliminary construction "is contrary to the presumptive interpretation based on the doctrine of claim differentiation, which is supported by the specification of the '849 Patent."

PO Resp. 33. Specifically, Patent Owner contends that claim 2 provides "that 1) the dielectric material fill the top portions of the spaces between the layered structures, and 2) that voids be left between adjacent stacks." *Id*. at 34. Consequently, Patent Owner contends that the term "a single layer of dielectric" means "only a single layer of dielectric," contending as follows:

> It is important to note that [claim 6] requires that the dielectric material between the layered structures be formed of a single layer, not just that it include a single layer. If "single layer of dielectric" is not construed to mean only one layer, then the scope of claim 6 would be identical to the scope of claim 2.

Id. (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005)).

Moreover, Patent Owner contends that the Specification of the '849 patent is consistent with this presumption. *Id*. at 34–35. In particular, Patent Owner contends

> [t]he specification clearly discloses two separate embodiments. Figure 4 depicts one embodiment in which there are multiple layers of dielectric between the top portions of the layered structures, consisting of one layer of dielectric 45 in between two layers of silicon dioxide 49. *See also* [Ex. 1001, 7:7–20]. The specification makes clear, however, that the silicon dioxide 49 is optional, stating that "Prior to depositing the dielectric layer 45, a thin layer 49 of silicon dioxide may optionally be grown over the exposed surfaces of the stacks and spaces between them." *Id*.[]. This part of the specification, therefore, describes a separate embodiment in which the optional silicon dioxide 49 is omitted.

Id. Thus, Patent Owner contends that, consistent with claim 6, if optional layer 49 is omitted, there is *only one* layer of dielectric material filling the space at the top portions of the spaces between the layered structures, and leaving voids between adjacent stacks. *Id*. at 35. Therefore, Patent Owner contends that the multiple layer embodiment discloses the structure recited

in claim 2 and the single layer embodiment discloses the embodiment of claim 6. *Id*. Consequently, Patent Owner concludes "that the broadest reasonable interpretation of 'formed of a single layer' means formed of only one layer." [2] *Id*. at 36.

Petitioner disagrees with Patent Owner's proposed construction of "a single layer of dielectric" and argues that our preliminary construction of this claim term is correct. Pet. Reply 27–28. Initially, Petitioner argues that, "[w]hen, as here, the patentee uses an indefinite article, such as 'a' or 'an,' before a claim element, the element is construed in an open-ended way to mean 'at least one' or 'one or more.'" *Id*. at 27 (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356-57 (Fed. Cir. 2000) (stating that "the claim limitation 'a,' without more, requires at least one" and "under the general rules of claim construction, this court presumes the customary meaning of 'a'—one or more")). Further, Petitioner argues that our preliminary construction of "a single layer of dielectric" is consistent with the additional limitations of claim 6, which distinguish claim 6 from the broader recitations of independent claim 2. *Id*. We agree. *See* Dec. on Inst. 11.

Finally, Petitioner notes that, contrary to Patent Owner's contentions, Patent Owner's declarant, Dr. Ho, "acknowledged that Figure 4, which

[2] Consistent with this construction, Patent Owner contends that "because Takeuchi in view of Lee fails to disclose a single layer of dielectric that fills the top portions of the spaces between the layered structures, the asserted combination does not render claim 6 obvious." PO Resp. 36. Because we do not adopt Patent Owner's construction, we review Petitioner's assertion of obviousness with respect to claim 6 based on the combined teachings of Takeuchi and Lee.

shows both layer 45 and layer 49 between the layered structures, is an embodiment of claim 6." *Id*. at 28 (citing Ex. 1035, 60:19–61:3); *cf*. PO Resp. 34–35; *see* Tr. 14:1–6, 31:22–32:17. Again, we agree with Petitioner that Figure 4 depicts the memory cell array, as recited in claim 6.

For the reasons set forth above, we determine that our preliminary construction of the term "a single layer of dielectric" as "one layer of dielectric" is the broadest reasonable interpretation of this term.

2. Other Claim Terms

No other claim terms require express interpretation. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (explaining that "claim terms need only be construed 'to the extent necessary to resolve the controversy'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

B. Obviousness over Takeuchi and Lee

1. Overview

Petitioner argues that claims 1–6 are unpatentable under 35 U.S.C. § 103(a) as obvious over Takeuchi and Lee. *See supra* Section I.E. In support of its argument, Petitioner provides a detailed mapping of limitations of claims 1–6 to structures described by Takeuchi and Lee. Pet. 26–43. Petitioner also cites its declarant's, Dr. Baker's, declaration for support. *See* Ex. 1003 ¶¶ 89–99. A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398,

406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.[3] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

2. Person of Ordinary Skill in the Art

Petitioner proposes an assessment of the level of ordinary skill in the art. Pet. 18; *see* Ex. 1003 ¶ 21. To the extent necessary, we adopted this level of skill for our Decision on Institution. Dec. on Inst. 12 n.3. Patent Owner does not now propose an alternative assessment. Nevertheless, Patent Owner contends that

> the knowledge required to have been able to form and position voids with the specific aspect ratios taught by the '849 Patent would have involved complex deposition processes entirely different from the deposition processes disclosed in the prior art. *The requisite knowledge of these different complex deposition processes would have been beyond the knowledge and skill of a person of ordinary skill in the art at the time of the '849 invention, and the prior art would not have provided sufficient instruction or guidance that it was necessary to use these other deposition processes to achieve the claimed invention.* Moreover, a person of ordinary skill in the art would not have even realized that deposition processes different than those disclosed in the prior art were necessary to form voids with the higher aspect ratios required by the claims of the '849 Patent.

PO Resp. 2–3 (emphasis added). Thus, Patent Owner contends that the '849 patent contains teachings of methods of manufacturing the claimed, non-

[3] Patent Owner does not present evidence of secondary considerations in the Patent Owner Response. *See* Tr. 4:19–20.

volatile memory cell array that would not have been understood by a person of ordinary skill in the art at the time of the invention. *See* Ex. 2001 ¶ 125. This contention, however, is contrary to Dr. Baker's testimony (*see* Ex. 1003 ¶¶ 48, 70–72, 79–81), as well as Dr. Ho's testimony (*see* Ex. 2001 ¶¶ 31–59; Ex. 1035, 85:11–17, 86:24–87:9), and, accordingly, Patent Owner's contentions regarding the level of skill assessment are not persuasive.[4] *See* Tr. 31:14–21 (Patent Owner's counsel acknowledged that conformal and non-conformal processes were known at the time of the invention claimed in the '849 patent.). Therefore, to the extent necessary, we again adopt Petitioner's assessment.[5]

3. Takeuchi (Ex. 1005)

Takeuchi describes embodiments of a semiconductor device, especially, a Not-AND (NAND)-type semiconductor device. Ex. 1005, Abstract. Specifically, Takeuchi identifies adverse effects in such devices, include undesirable variations in the threshold voltages of transistors, as well

[4] The challenged claims in this trial are apparatus claims, rather than method or product-by-process claims. Consequently, the methods by which the claimed cell arrays may be formed are not relevant to our determination of patentability of the challenged apparatus claims. *See* Tr. 13:2–6, 20:8–14, 31:3–8.

[5] Dr. Baker and Dr. Ho appear to exceed Petitioner's assessment of the level of ordinary skill in the art. *See generally* Ex. 1004; Ex. 2002; *see Duramed Pharmaceuticals, Inc. v. Watson Lab's, Inc.*, 413 F. App'x 289, 296 (Fed. Cir. 2010) (error to reject testimony of one who "was not a person of ordinary skill, but extraordinary skill," because "a person of extraordinary skill may opine on the knowledge of this hypothetical person") (citing *Moore v. Wesbar Corp.*, 701 F.2d 1247, 1253 (7th Cir. 1983)) ("not selected for publication").

as lowering of the breakdown voltage of the silicon oxide film, and lowering of the on-current of the transistors. *Id.* at 4:25–5:15. Takeuchi notes the following:

> In the semiconductor devices, a parasitic capacitance is created between the floating gate electrodes of adjacent gates. The adjacent memory cell transistors are involved in interference due to the parasitic capacitance. To reduce the interference, it is desirable that the parasitic capacitance be as small as possible. As recent advancement of miniaturization of semiconductor elements, the distance between the adjacent gates is small and thus the influence of the parasitic capacitance is remarkable.

Id. at 17:65–18:6. Takeuchi teaches that its embodiments achieve less parasitic capacitance than conventional semiconductor devices. *Id.* at 18:7–38.[6]

Figure 1 of Takeuchi, including our annotations, is reproduced below.

[6] Patent Owner contends that "Takeuchi does not teach the intentional use of voids to reduce the effect of capacitive coupling." PO Resp. 8. In view of the cited teachings, this contention is not accurate. Ex. 1005, 16:43–59; *see* Dec. on Inst. 13 n.5.

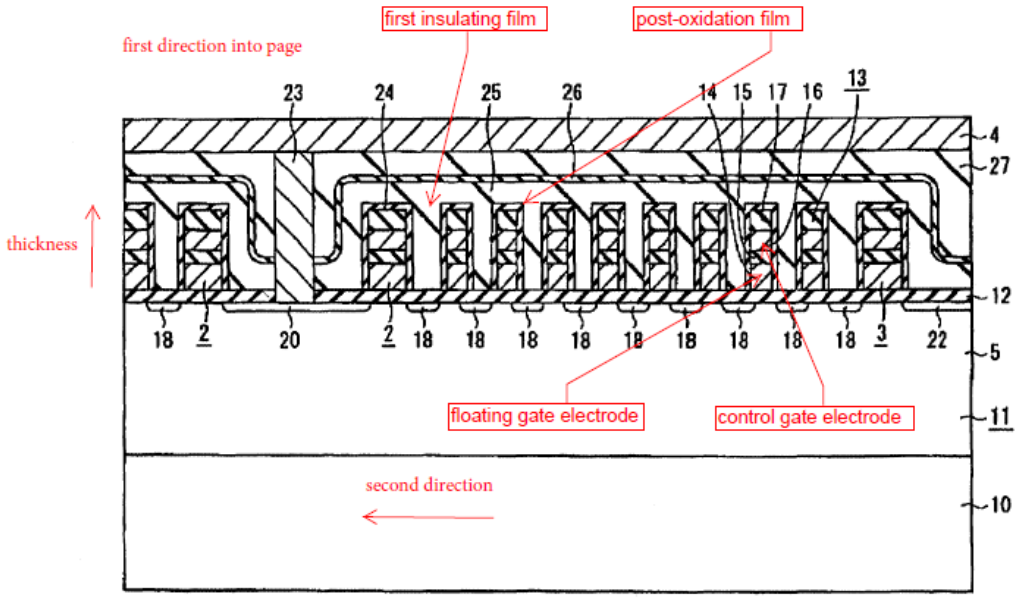


FIG. 1

Figure 1 depicts a first embodiment of Takeuchi's semiconductor device, including a plurality of word lines (*see* Ex. 1005, Fig. 3 (depicting word lines 1)) and a plurality of bit lines 4 that are formed perpendicular to the word lines in a column direction (*id.* at 7:65–8:1–5). The semiconductor device further includes an array of memory cells positioned between bit lines 4 and word lines 1. Each memory cell includes memory cell gate electrode 13 formed on element region 5, and "[t]he control gate electrode 16 of one memory cell gate 13 in a row is common to the control gate electrode of another memory cell gate 13 in the row and forms the word line 1." *Id.* at 8:22–34. Each gate electrode 13 comprises a stack of materials that includes floating gate electrode 14 and control gate electrode 16. *Id.* The distance between memory cell gate electrodes 13 is about 0.2 μm, and the height of each memory cell gate electrode 13 is about 0.6 μm. *Id.* at 9:46–48. These dimensions result in control gates that are separated by one third of the

thickness or height of the layered structures, i.e., an aspect ratio of 3:1. *See* Ex. 1001, 6:46–48.

The surface of each memory cell gate electrode 13 is covered with dielectric post-oxidation film 24. Ex. 1005, 9:19–20. First insulating film 25 is formed on post-oxidation film 24 in a manner so as "to embed" between memory cell gate electrodes 13. *Id.* at 9:24–26. As Takeuchi explains, "the phrase 'to embed' means not only to completely embed, *but also to embed but include a cavity or cavities,* since the functions and effects are not changed even if it includes a cavity such as void inside thereof." *Id.* at 9:42–45 (emphasis added). In the embodiment depicted in Figure 1, second insulating film 26 is formed on first insulating film 25, and interlayer insulating film 27 is formed on second insulating film 26. *Id.* at 9:59–10:2. Bit lines 4 are formed on interlayer insulating film 27. *Id.* at 10:10. Thus, there is at least a single layer, and there may be multiple layers of dielectric material in the spaces between adjacent, memory cell gate electrodes 13.

Figure 16 of Takeuchi, including our annotations, is reproduced below.

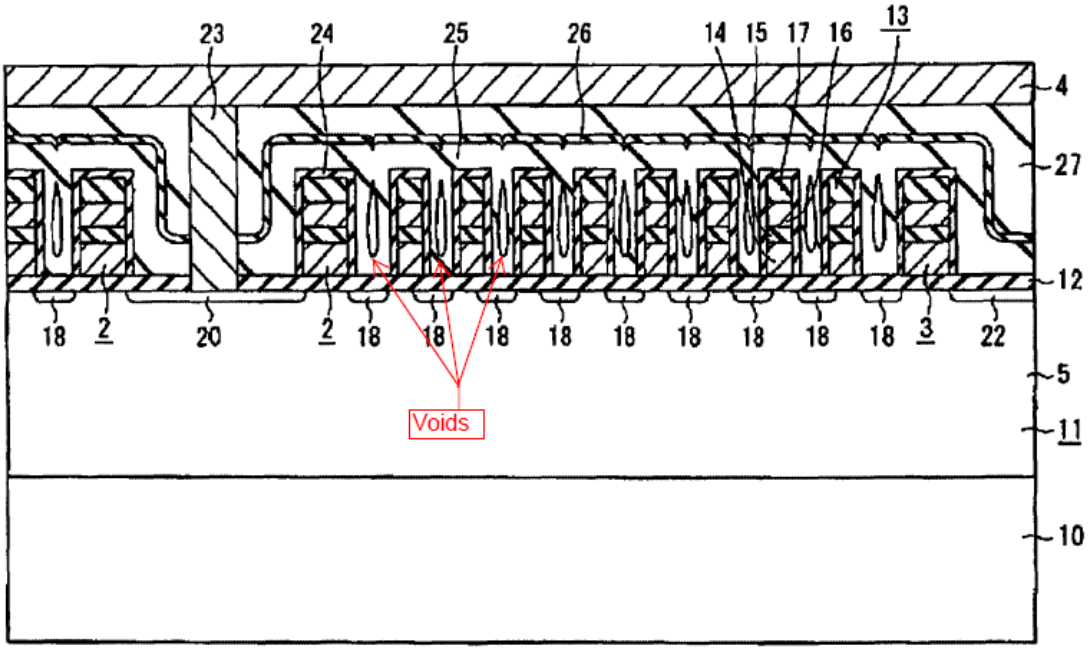


FIG. 16

Figure 16 depicts a cross-sectional view of another embodiment of Takeuchi. *Id.* at 6:37–39. This embodiment is similar to the embodiment depicted in Figure 1, except that each of the "distance portions" between memory cell gate electrodes 13 contains a void. *Id.* at 16:60–17:4. Takeuchi explains that this embodiment obtains similar advantages to those described with respect to other embodiments. *Id.* at 17:2–3.

4. Lee (Ex. 1006)

Lee is entitled "Effects of Floating-Gate Interference on NAND Flash Memory Cell Operation" and relates generally to operational concerns due to increased density of NAND flash memory devices and the resulting decreased gate-to-gate spacing in such devices. Ex. 1006, 2. In particular, Lee describes the problem of parasitic capacitance in high density memory devices. *Id.*

> NAND flash memory has given promise of high-density cell integration, thus it gets much attention as a mass storage device [1]-[5]. Currently, the cell integration density of the NAND flash memory is increasing very rapidly due to its simple structure suitable for high-resolution lithography [6]. The integration density of NAND flash memory is further enhanced by a factor of two by adopting multilevel cell operation [7].
>
> *However, as the cell integration density is increased, NAND flash memory cell suffers from increased parasitic capacitance between the cells, and we have noticed that it generates serious problems in multilevel cell operation.* This letter introduces the concept of floating-gate interference for the first time, shows experimental results of the floating-gate interference using 0.12-μm [6] design-rule cell and predicts the interference in future cells based on simulation results.

Id. According to Lee, NAND flash cell arrays were fabricated based on a 0.12 μm design rule (i.e., the distance of the space between the layered structures is 0.12 μm), and floating-gate interference measurements were performed on the fabricated arrays. *Id.* at 3–4.

Lee also describes simulation results for gate-to-gate spacings in NAND flash memories of less than 0.12 μm. *Id.* at 4, Fig. 4. The results suggest that floating-gate interference coupling ratios increase as gate-to-gate spacing decreased, and that increases below spacings of about 0.04 μm "can hardly be tolerated." *Id.* at 4. Consequently, Lee teaches that "it is required that we should develop a new cell structure, *such as vacuum isolation of the gate-to-gate spacing* or very thin floating-gate structure." *Id.* (emphasis added); *cf.* Ex. 1001, 4:7–14 (describing similar solutions to parasitic capacitance in the "Background" of the '849 patent).[7]

[7] The dielectric constant of air is slightly greater than 1, and the dielectric constant of a vacuum is 1. ALAN VAN HEUVELEN, PHYSICS, A GENERAL INTRODUCTION 450 (1982) (Table 22.1) (Ex. 3001); *see* Ex. 1001, 4:24–28

5. Analysis

a. Claims 1 and 2

As noted above, Petitioner argues that the combined teachings of Takeuchi and Lee would have rendered obvious the subject matter of claims 1 and 2 of the '849 patent. Pet. 26–40. Moreover, Dr. Baker provides a detailed mapping of the limitations of claims 1 and 2 onto the combined teachings of Takeuchi and Lee. Ex. 1003, A1–A41. With the exception of the final limitation of each of independent claims 1 and 2, claims 1 and 2 share the same limitations. *See supra* Section I.C.; *see also* Pet. 9–10 ("Challenged independent claims 1 and 2 are identical other than their final limitations."). In particular, with respect to the common limitations, Petitioner argues that Takeuchi teaches a non-volatile memory cell array formed on a semiconductor substrate. Pet. 29–30, 37 (citing, e.g., Ex. 1005, 4:35–42, 8:22–25); *see* Ex.1001, 9:40–41 (claim 1), 9:62–63 (claim 2).

In addition, Petitioner argues that Takeuchi teaches that its cell array may comprise "an array of charge storage elements carried by the substrate," and "conductive control gate lines elongated in a first direction across the charge storage elements and being separated in a second direction by a distance of separation of the charge storage elements in the second direction, the first and second directions being orthogonal with each other." Pet. 30–32, 38–40 (citing, e.g., Ex. 1005, 8:22–34, 7:65–8:2); Ex. 1003, A5–17; *see* Ex. 1001, 9:43–49 (claim 1), 9:64–10:6 (claim 2). Patent Owner does not

("The void will usually contain the gas present in the processing chamber when the dielectric is formed. Such a gas has a dielectric constant of 1.0 or only a small amount above 1.0, depending upon its exact composition."); Ex. 1035, 52:20–23; Tr. 26:11–19.

contend that these limitations are not taught be Takeuchi. *See* PO Resp. 2–3. We are persuaded Takeuchi teaches these limitations.

Petitioner further argues that Takeuchi teaches "dielectric material [disposed] between the layered structures in the second direction that fill top portions of spaces therebetween while leaving voids between adjacent charge storage elements of the layered structures." Ex. 1001, 9:54–57 (claim 1), 10:11–14 (claim 2). In particular, Takeuchi teaches first insulating film 25 of a dielectric material formed "to embed" between gate electrodes 13 of the memory cell transistors. Pet. 36–37 (citing, *e.g.*, Ex. 1005, 9:24–30); *see also* Pet. 44–45 (citing Ex. 1005, 9:42–45 (defining the phrase "to embed" to include forming a cavity or cavities in layer 25)).[8] Moreover, Takeuchi teaches that the dielectric layer may fill "top portions of the spaces" between the layered structures, and the voids may extend to or above the top of the layered structures. Pet. 45 (citing Ex. 1005, Fig. 16); *see* Ex. 1003 ¶ 70, A26–A29. Petitioner argues persuasively that Takeuchi teaches these limitations.

Although Patent Owner contends that "Takeuchi does not teach the intentional use of voids to reduce the effect of capacitive coupling" (PO Resp. 8), we note that the language of claims 1 and 2 only requires that the dielectric material is disposed between the layered structures "while *leaving* voids between adjacent charge storage elements of the layered structures" (Ex. 1001, 9:54–57 (claim 1), 10:11–14 (claim 2) (emphasis added); *but see* Ex. 1005, 16:57–59. Thus, as discussed further below, the challenged

[8] Although not relied upon by Petitioner to supply this limitation, Lee expressly teaches the use of "vacuum isolation" of the gate-to-gate spacing between the memory cells. Ex. 1006, 4; *see* PO Resp. 12.

apparatus claims do not recite how the voids are formed, but only that they are present. We also are persuaded that Takeuchi teaches this limitation.

Petitioner argues that Takeuchi and Lee teach or suggest that "layered structures including at least the charge storage elements and the control gates are separated in the second direction by distances that are less than one-fifth of a thickness of the layered structures." Pet. 32–36, 40–44; *see* Ex.1001, 9:50–53 (claim 1), 10:7–10 (claim 2). In particular, Takeuchi teaches that memory cell gate electrodes 13 may be formed as stacks of layers including charge storage elements and control gates. Pet. 33, 41 (citing Ex. 1005, 8:22–34 (disclosing memory cell gate electrodes 13 including floating gate electrodes 14 and control gate electrodes 16)). Moreover, Takeuchi teaches that

> when the gate electrode is formed in a significant height comparing to the distance between the gate electrodes, *a large cavity is easily generated in the first insulating film between the gate electrodes*, however, in the present embodiment, the cavity in the first insulating film thus generated can be embedded with the first insulating film.

Id. at 16:21–27 (emphasis added). Although Petitioner acknowledges that "Takeuchi does not expressly disclose . . . an embodiment wherein the gate-to-gate spacing (i.e. the spacing between memory cell gate electrodes 13) is less than one fifth of the height of the memory cell gate electrodes as required by this limitation" (*id.* at 34, 42), Petitioner argues that a person of ordinary skill in the art would have found that spacing obvious based on the combined teachings of Takeuchi and Lee (*id.*). *See also* Tr. 41:7–16, 47:5–21 (same material argument).

Initially, Petitioner notes that Takeuchi discloses an embodiment in which the thickness of the layered structures is "about 0.6 μm," and the

gate-to-gate spacing or separation distance in the second direction is "about 0.2 μm." *Id.* (citing Ex. 1005, 9:46–48). Consequently, Takeuchi expressly teaches layered structures including floating gates and control gates separated in the second direction by distances that are less than one-third (0.2 μm/0.6 μm) of a thickness of the layered structures, i.e., an aspect ratio of 3:1. Further, Lee teaches that gate-to-gate spacings between memory cell electrodes may be 0.12 μm or less. *Id.* (citing Ex. 1006, 2, 4). Thus, in view of Lee's spacing, Petitioner argues that Takeuchi and Lee teach or suggest layered structures including floating gates and control gates separated in the second direction by distances that are less than one-fifth (0.12 μm/0.6 μm) of a thickness of the layered structures, i.e., an aspect ratio of 5:1. *Id.* at 34–35, 42–43. We are persuaded that Takeuchi and Lee teach this limitation.

As noted above, the final limitations recited in independent claims 1 and 2 differ. In particular, claim 1 recites that "the charge storage elements are conductive floating gates and the elongated control gate lines extend downward between adjacent floating gates in the first direction." Ex. 1001, 9:58–61. Petitioner argues that Takeuchi and Lee teach this limitation. Pet. 37–38. In particular, Takeuchi teaches elongated control gate lines that extend across the conductive floating gates. *Id.* at 45 (citing Ex. 1005, Figs. 1 and 3); *see* Ex. 1003, A13–A17. Dr. Baker acknowledges that "Takeuchi does not disclose . . . a cross-sectional view of the memory cell array in the word line direction." Ex. 1003, A30. Nevertheless, Dr. Baker testifies that like Takeuchi, "Lee discloses a typical NAND array," and "Lee also provides in Fig. 1 a view in the word line direction of the NAND array, wherein the control gates extend downward between adjacent floating gates." *Id.* To the extent that Takeuchi may not teach control gates

extending downward between adjacent floating gates, as recited in claim 1, because the teachings of Takeuchi and Lee are directed to the reduction of parasitic capacitance, Dr. Baker testifies that a person of ordinary skill in the art would have had reason "to extend the control gates lines between adjacent floating gates in Takeuchi to reduce the parasitic capacitance between floating gates in a given row of memory cells." Pet. 38; *see* Ex. 1003 ¶¶ 42, 49. We are persuaded that Takeuchi and Lee teach this limitation.

Claim 2 recites that "the control gate lines include word lines extending in the first direction along rows of charge storage elements and the charge storage elements form, along columns in the second direction, series strings of a plurality of charge storage transistors." Ex. 1001, 10:15–17. Petitioner argues that Takeuchi teaches this limitation. Pet. 39–40. In particular, Takeuchi teaches that "[t]he control gate electrode 16 of one memory cell gate 13 in a row is common to the control gate electrode of another memory cell gate 13 in the row and forms the word line 1." *Id*. at 39 (quoting Ex. 1005, 8:31–34). Further, Petitioner argues that Takeuchi teaches that "[e]ach memory cell transistor is connected in the second column direction to form 'series strings of a plurality of charge storage transistors' between a source and drain side selecting gate." *Id*. (citing Ex. 1005, 8:35–39); *see* Ex. 1003, A36–A40; *see also* Ex. 1005, 9:5–6 ("The memory cell transistors are connected to each other in series."). Consequently, Dr. Baker testifies that, "because Takeuchi describes a standard NAND configuration wherein word lines extend across rows of floating gates, and the floating gates form memory cell transistors that are

connected in series in the column direction," Takeuchi teaches this limitation of claim 2. Ex. 1003, A40. We agree.

Petitioner argues that a person of ordinary skill in the art would have had several reasons to combine the teachings of Takeuchi and Lee to achieve the apparatus recited in challenged claims 1 and 2. Pet. 26–29; *see* Ex. 1003 ¶¶ 92–99. First, Dr. Baker testifies that, because "Takeuchi and Lee are directed to non-volatile memory arrays in a NAND configuration wherein the memory cells are arranged in a conventional stacked formation," a person of ordinary skill in the art would have understood that the teachings in both Takeuchi and Lee are interrelated and compatible with one another, and that it would have been obvious to try combining the related teachings of Takeuchi with those of Lee. Ex. 1003 ¶ 93. Second, Dr. Baker testifies that a person of ordinary skill in the art would have understood that "there were significant market pressures to maximize memory cell density on a given amount of silicon." *Id*. ¶ 94; *see KSR*, 550 U.S. at. 417 ("When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one."). Dr. Baker further testifies that, because Takeuchi and Lee teach that gate-to-gate spacings can be reduced and that it is desirable to do so in order to increase the memory cell density (*see* Ex. 1005, 10:17–19, 11:1–10; Ex. 1006, 2), a person of ordinary skill in the art would have had reason to look to the known techniques taught by Lee to reduce the gate spacing of Takeuchi (*id*. ¶ 94). Third, Dr. Baker testifies that, because Takeuchi and Lee share a common goal of reduced gate-to-gate spacing and because Takeuchi teaches improved results in the presence of voids (*see* Ex. 1005, 16:43–59) and Lee teaches the use of vacuum isolation (*see* Ex. 1006,

4), a person of ordinary skill in the art would have had reason to combine known techniques to achieve predictable results. Ex. 1003 ¶ 95. Fourth, Dr. Baker testifies that persons of ordinary skill in the art would have understood that "voids between adjacent memory cells were more easily formed, and could be formed larger, when the aspect ratio between the height of the memory cell and the width between the memory [cells] is high." *Id*. ¶ 96 (citing Ex. 1005, 16:21–27); *see* Ex. 1018, 3:46–54, 4:58–67; Tr. 7:6–21. Thus, Dr. Baker testifies that a person of ordinary skill in the art would have had reason to increase the aspect ratio of the memory cells, such as those taught by Takeuchi in view of Lee, to more easily provide for larger voids to achieve better isolation of the floating gate electrodes. *Id*. ¶ 96; *see In re Ethicon*, 844 F.3d 1344, 1351 (Fed. Cir. 2017) ("The normal desire of artisans to improve upon what is already generally known can provide the motivation to optimize variables . . . for use in a known device."). Fifth, Dr. Baker testifies that because Takeuchi and Lee seek to reduce the effects of parasitic capacitance on adjacent memory cells (*see* Ex. 1005, 5:5–11; Ex. 1006, 2) and because Takeuchi and Lee teach similar solutions, namely using dielectric materials with lower dielectric constants (i.e., air or a vacuum), a person of ordinary skill in the art would have had reason to look to similar solutions to similar problems. Ex. 1003 ¶ 97. We find Dr. Baker's testimony credible.

We find that Petitioner argues persuasively that the combined teachings of Takeuchi and Lee teach or suggest all of the limitations of independent claims 1 and 2 and that a person of ordinary skill in the art would have had reason to combine their teachings to achieve the apparatus recited in these claims.

b. Patent Owner's Contentions

Patent Owner contends that Petitioner fails to demonstrate that the combined teachings of Takeuchi and Lee render claims 1–6 unpatentable for two reasons. PO Resp. 2–4.

i. Nonconformal deposition processes

First, Patent Owner contends that Petitioner fails to demonstrate that a person of ordinary skill in the art would have had a reasonable expectation of success in making or implementing the claimed invention by combining the teachings of Takeuchi and Lee. *Id*. at 16–23. In particular, Patent Owner contends (1) that the combined teachings of Takeuchi and Lee fail to teach or disclose the necessary deposition processes for intentional formation of voids in "a consistent and reproducible manner" (*id*. at 16–19) and (2) that "the knowledge of, and need for, the non-conformal deposition processes taught by the '849 patent would have been outside the scope of knowledge and skill of a person of ordinary skill in the art at the time of the invention" (*id*. at 19–23). For the reasons set forth below, we disagree.

Initially, Patent Owner contends that

> for a person of ordinary skill in the art to have been able to make or implement the claimed invention, that skilled artisan would have had to have been aware that the conformal LPCVD and APCVD deposition processes disclosed in the asserted prior art would not have been suitable for intentionally creating voids at the specific locations and with the specific aspect ratios recited in the '849 Patent, *and that instead, entirely different and even more complex non-conformal processes such as PECVD or PVD with sputtering would be necessary*.

Id. at 16 (emphasis added). Dr. Ho testifies as to the differences between conformal and nonconformal processes. Ex. 2001 ¶ 103. Dr. Ho's Figure 7 is reproduced below.

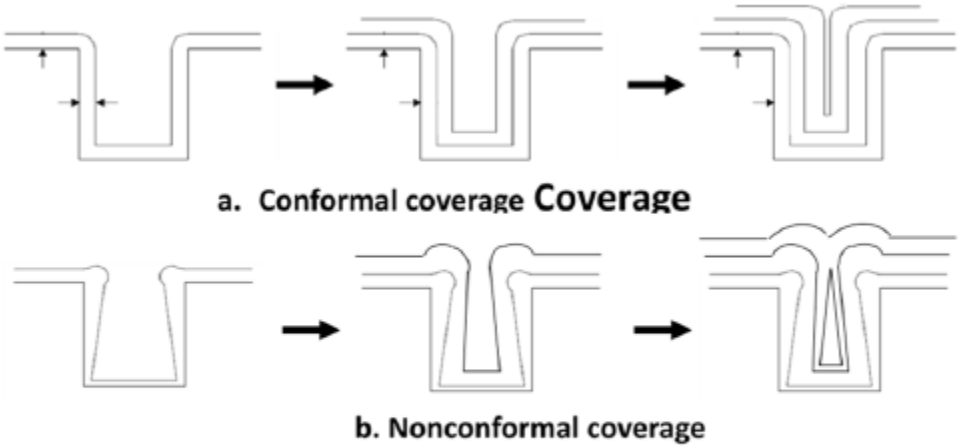


Figure 7. CVD deposition sequences showing conformal versus non-conformal film deposition.

Id. Figure 7 depicts a conformal process in which layers of uniform thickness are deposited in a space between two structures, resulting in the space becoming increasingly narrow, but in which no void is formed. *See id*. ¶¶ 102 ("Takeuchi and the APCVD process disclosed by Sato are conformal processes used to deposit the insulating film material in a *uniform* manner." (Emphasis added.)), 104 ("[T]he conformal deposition *with its uniform film layer* may lead to a structure with a narrow seam in the middle of the trench. It will not consistently result in a closed void structure as disclosed by the '849 patent." (Emphasis added.)). Dr. Ho's Figure 7 also depicts a nonconformal process in which layers of non-uniform thickness are deposited in a space between two structures, resulting in the space becoming increasingly narrow, but in which a void is formed. *See id*. ¶ 102 ("The PECVD process and PVD with sputtering taught by the '849 are non-

conformal and directional processes that deposit the film in a *non-uniform* manner." (Emphasis added.)).

Patent Owner contends that neither Takeuchi nor Lee teaches or suggests a nonconformal deposition process. PO Resp. 18–19. Consequently, Patent Owner concludes that neither Takeuchi nor Lee teaches or suggests the type of deposition processes for the intentional formation of voids that are "necessary" to achieve that apparatus claimed in the '849 patent. *Id*. at 16 ("instead, entirely different and even more complex non-conformal processes such as PECVD or PVD with sputtering would be *necessary*" (emphasis added)). Hence, Patent Owner contends that a person of ordinary skill in the art would not be able to achieve the apparatus recited in the challenged claims, based on the applied art.

Patent Owner's contentions are not persuasive for numerous reasons. First, as Patent Owner acknowledges, neither the '849 patent nor Takeuchi is limited to "conformal" or "nonconformal" processes. Tr. 30:10–13 (Takeuchi is not limited to conformal processes), 31:3–8 ("The methods [of the '849 patent] don't say conformal or non-conformal process."). Second, Patent Owner acknowledges that Takeuchi teaches the creation of voids. *Id*. at 30:1–9. Dr. Ho further testified that "[y]ou cannot look at the final structure of the film and say that whether this is conformal or not conformal, per se." Ex. 1035, 85:13–17. Thus, Takeuchi's Figure 16 does not reveal whether the depicted voids were created by a conformal or nonconformal process. Ex. 1005, Fig. 16; *cf*. Ex. 1007, Fig. 9(b) (depicting void 20). Third, not only does the '849 patent fail to mention conformal or nonconformal processes, the Specification of the '849 patent broadly describes the types of process that may be used to form the voids. In

particular, the ’849 patent states that “[m]any different combinations of starting gasses, pressures, temperatures and times may be used to form the layer 45 of silicon dioxide to include the voids 47, and are usually dependent upon the particular deposition equipment being used,” but does not require any specific process. Ex. 1001, 7:21–37; *see* Tr. 31:3–6. Further, the processes discussed by the parties were known at the time of the invention. *See* Ex. 1035, 23:20–22; Tr. 31:14–21. Fourth, Patent Owner applies an improper standard when it contends that the combined teachings of Takeuchi and Lee fail to teach or disclose the necessary deposition processes for intentional formation of voids in a “consistent and reproducible manner.” PO Resp. 16. As Petitioner correctly explains, there is no requirement that the voids are made in such a manner. Pet. Reply 4–5.

Perhaps most importantly, Patent Owner’s contentions regarding conformal and nonconformal processes are based on a flawed presumption, namely, that the dielectric must be deposited on the side walls of the spaces between adjacent layered structures. Claims 1 and 2 merely recite that “dielectric material between the layered structures *in the second direction that fill top portions of spaces therebetween* while leaving voids between adjacent charge storage elements of the layered structures.” Ex. 1001, 9:54–57 (claim 1), 10:11–14 (claim 2). Thus, the claims recite that the top of the space may be sealed to create a void below, that is, “between adjacent charge storage elements of the layered structures.” Tr. 16:6–21, 21:3–16, 23:21–24:14; *see* Pet. Reply 15–16. The Specification of the ’849 patent makes this clear when it states

> *[i]n one embodiment, this isolation is formed in spaces between floating gates at the bottom of stacks of layers having a height of five, eight or more times the width of the spaces between*

> *the stacks.* The other layers in the stacks usually contain at least one dielectric and a conductive control gate line. This 5:1, 8:1 or more cross-sectional aspect ratio of the spaces between the stacks allows a dielectric to be formed that extends downward into the spaces along sidewalls of the stacks but not filling the bottom segments of the spaces between the charge storage elements. *Top portions of the spaces are filled with the dielectric, however, thereby leaving large voids sealed in the dielectric between the charge storage elements.*

Ex. 1001, 4:35–47 (emphases added). Thus, we are not persuaded that the challenged claims of the '849 patent require conformal or nonconformal deposition processes or that Takeuchi and Lee fail to teach the formation of the recited voids, regardless of the possible processes used. Consequently, because we do not find that the '849 patent requires the use of nonconformal processes, we also find unpersuasive Patent Owner's contention that the knowledge of and the need for the nonconformal deposition processes allegedly taught by the '849 patent would have been outside the scope of knowledge and skill of a person of ordinary skill in the art at the time of the invention or that a person of ordinary skill in the art would not have had a reasonable expectation of success in achieving the claimed apparatus based on the combined teachings of Takeuchi and Lee. PO Resp. 19–23; *see* Pet. Reply 5–12.

ii. Filling Top Portions of the Spaces

Second, Patent Owner contends that Petitioner fails to demonstrate that the combined teachings of Takeuchi and Lee teach dielectric material that fills top portions of spaces between layered structures. PO Resp. 24–29. In particular, Patent Owner contends that

> Takeuchi's specification supports the conclusion that the voids in Figure 16 also extend to the upper limit of the spaces between

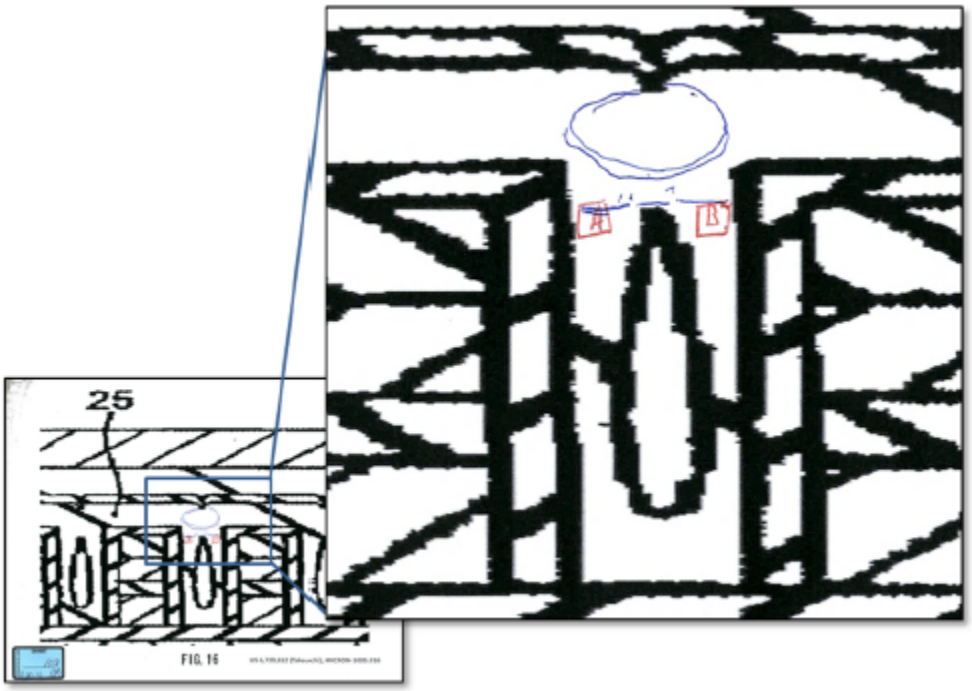
> the control gate electrodes. Specifically, Takeuchi states that "all of the distance portions between the memory cell gates contain voids. *In other words, no distance portions between the memory cell gates is completely embedded by the first insulating film.*"

Id. at 27 (quoting Ex. 1005, 16:64–17:1 (emphasis added)). Thus, Patent Owner concludes that "the top portions of the spaces between the adjacent layered structures in Takeuchi are not filled with dielectric as is required by claims 1 through 6 of the '849 Patent." *Id*. at 27–28. Further, Patent Owner reminds us that, to the extent Takeuchi's Figure 16 may appear to show the void terminating below the top portions of the spaces, we may not rely properly on such drawing depictions as definitive. *Id*. at 28. Again we disagree with Patent Owner's conclusion.

Initially, we note that the language of claims 1 and 2 does not require that the voids end below the top portions or that the top portions are filled *entirely*, such that they include no portion of a void. Pet. Reply 15–16. Instead, claims 1 and 2 merely recite that (1) dielectric material is "between the layered structures in the second direction" and (2) "*top portions of spaces therebetween* [are filled] while leaving voids between adjacent charge storage elements of the layered structures." Ex. 1001, 9:54–57 (claim 1), 10:11–14 (claim 2). Thus, as long as "top portions" of the spaces between the layered structures are filled, this further limitation of claims 1 and 2 is satisfied.

As Petitioner argues, Figure 4 of the '849 patent, which is reproduced above, appears to show voids 47 extending above the top of the layered structures. Pet. Reply 17. Moreover, Dr. Ho testified that Figure 4 of the '849 patent depicts the apparatus as recited in claims 1 and 2, as well as in claim 6. *Id*. (citing Ex. 1035, 60:4–61:3); *see* Ex. 1035, 63:23–64:1. Thus,

even if Patent Owner is correct that the voids in Takeuchi's Figure 16 extend above the tops of the adjacent layered structures, such a structure is not contrary to the recitations of claims 1 and 2, as that language would be understood in view of the Specification of the '849 patent. Pet. Reply 18–19. Further, during his deposition, Dr. Ho testified that the "top portions" taught by Takeuchi are above the voids depicted in Takeuchi's Figure 16. *Id*. at 20. The annotated Figure 16, showing Petitioner's annotations in red and Dr. Ho's annotations in blue, is reproduced below.



Ex. 1031, Fig. 16; *see* Ex. 1035, 61:8–63:15; *cf.* Pet. Reply 20 (reproducing Ex. 1030, Fig. 4 (as annotated)). Specifically, Dr. Ho annotated Takeuchi's Figure 16 during the deposition to clearly indicate that the "top portions" are above the voids, separating them by a dashed blue line.

As Patent Owner notes, in general, it may not be proper in some cases to rely on drawings for "precise proportions or particular sizes of objects

when the specification is silent on the matter." *Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000); *see* PO Resp. 28. Nevertheless, the clear teachings of the drawings cannot be ignored, which here inform us that the voids may, but need not, extend above the level of the layered structures. *See In re Marz*, 455 F.2d 1069, 1072 (CCPA 1972) ("'Patent drawings are not working drawings . . . .' However, we did not mean that things patent drawings show clearly are to be *disregarded*."). Takeuchi's and the '849 patent's drawings are not definitive on the size of the voids, but Dr. Ho's testimony is persuasive evidence of what a person of ordinary skill in the art would discern from these drawings. *See* Ex. 1030; Ex. 1031. In particular, the depictions in the drawings and Dr. Ho's testimony explain that the "top portions of spaces" may or may not be below the tops of the layered structures. Pet. Reply 22. Accordingly, we are persuaded that Takeuchi's teachings regarding the height of the voids are broad enough to encompass the recited limitations of independent claims 1 and 2.

Accordingly, after considering the arguments and evidence presented by each party, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the combined teachings of Takeuchi and Lee would have rendered obvious claims 1 and 2 of the '849 patent.

c. Claims 3 and 4

Claims 3 and 4 depend directly from claim 2. *See supra* Section I.C. Claim 3 recites that "the dielectric material includes at least one of silicon dioxide and silicon nitride," and claim 4 recites that "the charge storage elements are conductive floating gates." Ex. 1001, 10:20–24. Petitioner argues that the combined teachings of Takeuchi and Lee would have

rendered obvious the subject matter of claims 3 and 4 of the '849 patent. Pet. 40–41. Moreover, Dr. Baker provides a detailed mapping of the additional limitations of claims 3 and 4 onto Takeuchi. Ex. 1003, A42–45. In particular, with respect to claim 3, Petitioner argues that Takeuchi teaches that the dielectric material may include "silicon oxide film, an oxinitride film, or an oxidized silicon nitride film." Pet. 40 (citing Ex. 1005, 9:19–30, 18:7–19). Further, with respect to claim 4, Petitioner argues that Takeuchi teaches that "'each memory cell gate electrode 13' in the NAND memory array of claim 2 comprises a conductive 'floating gate electrode 14 which becomes a charge accumulation layer.'" *Id*. at 40–41 (citing Ex. 1005, 8:26–29). We find Petitioner's arguments and evidence, including Dr. Baker's unrebutted testimony regarding the mapping of claims 3 and 4 on the teachings of Takeuchi, persuasive.

Patent Owner does not contend that dependent claims 3 and 4 are separately patentable, but, instead, relies on its contentions with respect to their base claim, claim 2. *See* PO Resp. 2–3. Because Patent Owner does not present arguments directed specifically to the recitations of claims 3 and 4, Patent Owner waives such arguments. *See* Paper 13, 3. In view of the analysis set forth above with respect to independent claim 2 (*see supra* Section II.B.5.a. and b.), Petitioner argues persuasively that the combined teachings of Takeuchi and Lee would have rendered claims 3 and 4 obvious. Pet. 40–41; *see* Ex. 1003, A42–A45. Thus, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the combined teachings of Takeuchi and Lee would have rendered obvious claims 3 and 4 of the '849 patent.

d. Claim 5

Claim 5 depends directly from claim 2. *See supra* Section I.C. Claim 5 recites that "the layered structures are separated in the second direction by distances that are less than one-eighth of a thickness of the layered structures." Ex. 1001, 10:25–28. Petitioner argues that the combined teachings of Takeuchi and Lee render obvious the subject matter of claim 5. Pet. 41–42. Moreover, Dr. Baker provides a detailed mapping of the limitations of claim 5 onto Takeuchi and Lee. Ex. 1003, A46–A47. In particular, with respect to claim 5, Petitioner argues that Takeuchi teaches "an embodiment wherein the height of the memory cells (the thickness of the layered structures) is 'about 0.6 μm' and the gate-to-gate spacing (the distance of separation in the second direction) is 'about 0.2 μm.'" Pet. 34 (citing Ex. 1005, 9:46–48). Further, Takeuchi teaches that the gate-to-gate spacing may be less than 0.2 μm. *Id*. (citing Ex. 1005, 10:17–19). Petitioner also notes that Lee teaches that the gate-to-gate spacing between adjacent memory cells may be less than about 0.12 μm. *See* Ex. 1006, 2, Fig. 4. Thus, Petitioner argues that Takeuchi and Lee teach or suggest layered structures including floating gates and control gates separated in the second direction by distances that are less than one-fifth (0.12 μm/0.6 μm) of a thickness of the layered structures, i.e., an aspect ratio of 5:1. Pet. 34–35. Petitioner argues that the combined teachings of Takeuchi and Lee teach or suggest further reducing the aspect ratio (*see* Ex. 1005, 16:21–27, 3:37–38; Ex. 1006, Fig. 4) and, thus, the additional limitations of claim 5. Pet. 32–36 (Section 9.1.4), 41–42. We find Petitioner's arguments and evidence, including Dr. Baker's testimony regarding the mapping of claim 5 on the teachings of Takeuchi and Lee, persuasive. Further, Petitioner relies on the

reasons to combine the teachings of Takeuchi and Lee, as set forth above with respect to claims 1 and 2. *Id*. at 41.

Patent Owner does not contend that dependent claim 5 is separately patentable, but, instead, relies on its contentions with respect to its base claim, claim 2. *See* PO Resp. 2–3. Because Patent Owner does not present arguments directed specifically to the recitations of claim 5, Patent Owner waives such arguments. *See* Paper 13, 3. In view of the analysis set forth above with respect to independent claim 2 (*see supra* Section II.B.5.a. and b.), Petitioner argues persuasively that the combined teachings of Takeuchi and Lee would have rendered claim 5 obvious. Pet. 41–42; *see* Ex. 1003, A46–A47. Thus, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the combined teachings of Takeuchi and Lee would have rendered obvious claim 5 of the '849 patent.

e. Claim 6

Claim 6 depends directly from claim 2. *See supra* Section I.C. Claim 6 recites that "the dielectric material between the layered structures in the second direction are formed of *a single layer of dielectric* that fills top portions of spaces therebetween while leaving voids underneath the sealed top portions in between adjacent charge storage elements of the layered structures." Ex. 1001, 10:30–35 (emphasis added). As noted above, Patent Owner contends that the term "a single layer of dielectric" should be construed to mean "*only* one layer of dielectric." PO Resp. 33. For the reasons set forth above, we decline to adopt Patent Owner's construction. *See supra* Section II.A.1. Instead, we construe this term to mean "one layer of dielectric."

Petitioner argues that the combined teachings of Takeuchi and Lee render obvious the subject matter of claim 6 of the '849 patent. Pet. 42–43. Moreover, Dr. Baker provides a detailed mapping of the limitations of claim 6 onto Takeuchi and Lee. Ex. 1003, A48–A50. In particular, referring to Takeuchi's Figure 16, Petitioner argues that Takeuchi's first insulating film 25 teaches the single layer of dielectric that fills top portions between adjacent memory cell gate electrodes 13 and that post-oxidation film 24 is part of the layered structure and that second insulating film 26 is not formed in top portions between adjacent memory cell gate electrodes 13. Pet. 43. Thus, neither film 24 nor film 26 is another "single layer of dielectric that fills top portions of spaces." *See* Pet. Reply 25–26.

Patent Owner contends that, unlike Figure 4 of the '849 patent, which teaches "multiple layers of dielectric between the top portions of the layered structures, consisting of one layer of dielectric 45 in between two layers of silicon dioxide 49" (Ex. 1001, 7:7–20), Takeuchi's first insulating film 25 does "not include only a single layer of dielectric." PO Resp. 33–34. In particular, Patent Owner contends that, unlike Takeuchi's films 24 and 26, layer of silicon dioxide 49 is optional. *Id*. Nevertheless, Dr. Ho testified that Figure 4 of the '849 patent, which depicts multiple layers, embodies the limitations of both claim 2 and claim 6. Ex. 1035, 60:12–61:3; *see* Tr. 13:10–15:10.[9] We agree. Consequently, we are persuaded that Petitioner

[9] Patent Owner's counsel attempts to lessen the effect of Dr. Ho's testimony on this point. Tr. 32:4–17. Patent Owner did not attempt to contact us during the deposition to discuss Petitioner's counsel's questioning, and we find no evidence in the transcript of the deposition to indicate that Dr. Ho's testimony represents anything other than his affirmative responses to the questions of Petitioner's counsel. *See* Ex. 1035, 60:12–61:3.

has shown by a preponderance of the evidence that the combined teachings of Takeuchi and Lee would have rendered obvious claim 6 of the '849 patent.

f. Summary

Accordingly, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in showing that the combination of the teachings of Takeuchi and Lee would have rendered obvious claims 1–6 of the '849 patent.

C. Obviousness over Sato and Lee

1. Overview

Petitioner argues that claims 1–6 are unpatentable under 35 U.S.C. § 103(a) as obvious over Sato and Lee. *See supra* Section I.E. To support its contention, Petitioner provides a detailed mapping of limitations of claims 1–6 to structures described by Sato and Lee. Pet. 43–60. Petitioner also cites Dr. Baker's Declaration for support. *See* Ex. 1003 ¶¶ 100–110.

We begin our analysis of these grounds of unpatentability with a review of the applied art.[10]

2. Sato (Ex. 1007)

Sato describes a semiconductor memory array device made up of EEPROM cells that have a floating-gate structure. Ex. 1007 ¶ 39. As with Takeuchi and Lee, discussed above, Sato recognizes the problem of capacitive coupling and noted that the introduction of a cavity between

[10] A review of Lee and an assessment of the level of skill of a person of ordinary skill in the art are provided above. *See supra* Section II.B.2. and 4.

adjacent floating gates reduced the consequences of capacitive coupling. *Id.* ¶¶ 41, 58; *see id.* ¶¶ 4, 9, 14. Sato's Figure 9(b) of Sato, including our annotations, is reproduced below.

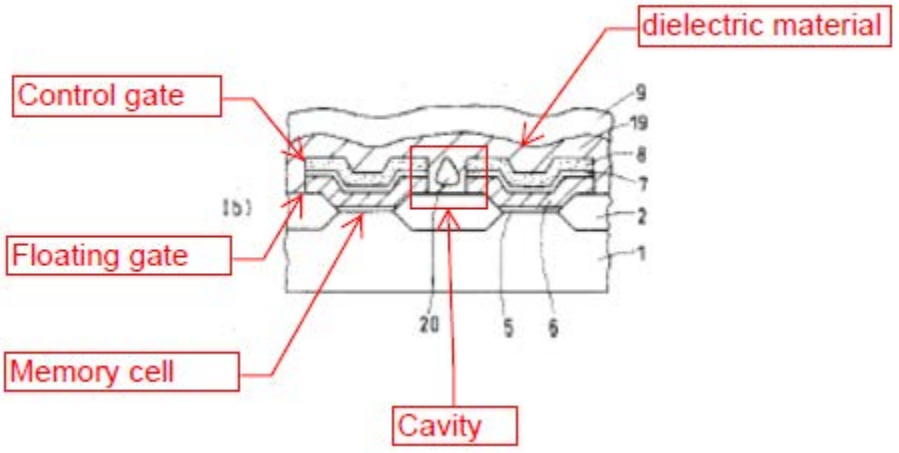


Fig. 9(b)

Figure 9(b) depicts the manufacturing process for a semiconductor memory. *Id.* ("Brief Description of the Drawings"). The semiconductor memory includes polysilicon film 8, "etched so as to leave a part capable of serving as a control gate electrode, . . . control gate electrode 8 consisting of a polysilicon film is thereby formed"; and, "with the control gate electrode 8 as a mask, the interlayer insulating film 7 and the polysilicon film 6 are etched to form a floating gate electrode 6 consisting of a polysilicon film." *Id.* ¶ 43.

> [U]sing an ordinary pressure vapor phase growth method using silane gas and oxygen, a silicon oxide insulating film 19 is deposited over the whole surface. *At this time, as the deposition is carried out at ordinary pressure, the silicon oxide insulating film 19 does not entirely fill the trench part, i.e. between the control gate electrodes 8 and between the floating gate electrodes 6, and overhangs it, whereby a cavity 20 is formed.*

> Then, on that, by a known vapor phase growth method the whole surface is covered with a silicon oxide insulating film 9.

Id. (emphasis added). Sato goes on to explain that "although it is preferable for the interior of the cavity 20 to be in a vacuum state, there are similar effects even if it contains a gas such as air." *Id.* ¶ 45.

In Figure 9(b), the memory array device includes a plurality of layers provided on substrate 1. In such an array, each memory cell may include the following: a 0.01 μm thick, gate insulating film 5; a 0.35 μm thick, floating-gate electrode 6; a 0.3 μm thick, insulation film 7; a 0.4 μm thick, control gate 8; and a 0.5 μm thick, isolation insulating film 2. *Id.* ¶ 42. As noted above, silicon oxide insulating layer 19 is provided over the memory cells, and cavity 20 is provided in silicon oxide insulating layer 19 in the spaces or trench between adjacent memory cells. *Id.* ¶ 43.

Although, referring to Figures 23 and 24, Sato describes reduced read out margins when gap 10 between floating gate electrodes 6 and gap 11 between control gate electrodes 8 are less than 0.3 μm, Sato does not teach limiting dimensions of the space between the layered structures in its memory cell array or specific aspect ratios. *Id.* ¶¶ 9–11, Figs. 23 and 24.

3. Analysis

a. Claims 1 and 2

Petitioner argues that the combined teachings of Sato and Lee render obvious the limitations of independent claims 1 and 2 of the '849 patent. Pet. 46–57. Moreover, Dr. Baker provides a detailed mapping of the limitations of claims 1 and 2 onto the combined teachings of Sato and Lee. Ex. 1003, B1–B38. As noted above, with the exception of the final

limitation of each of claims 1 and 2, claims 1 and 2 share the same limitations. *See supra* Section I.C.; *see also* Pet. 9–10.

Petitioner argues that Sato teaches a non-volatile memory cell array formed on a semiconductor substrate. Pet. 47 (citing, e.g., Ex. 1007 ¶¶ 1, 42); Ex. 1003, B1–4; *see* Ex.1001, 9:40–41 (claim 1), 9:62–63 (claim 2). Further, Petitioner argues that Sato teaches that its cell array may comprise "an array of charge storage elements carried by the substrate," and "conductive control gate lines elongated in a first direction across the charge storage elements and being separated in a second direction by a distance of separation of the charge storage elements in the second direction, the first and second directions being orthogonal with each other." Pet. 47–50 (citing, e.g., Ex. 1007 ¶¶ 41–43); Ex. 1003, B4–B16; *see* Ex. 1001, 9:43–49 (claim 1), 9:64–10:6 (claim 2). Patent Owner does not contend that these limitations are not taught by Sato. *See* PO Resp. 2–3. We are persuaded that Sato teaches these limitations.

In addition, Petitioner argues that Sato teaches "dielectric material [disposed] between the layered structures in the second direction that fill top portions of spaces therebetween while leaving voids between adjacent charge storage elements of the layered structures." Ex. 1001, 9:54–57 (claim 1), 10:11–14 (claim 2). In particular, Sato teaches silicon oxide insulating film 19 of a dielectric material filling the space between the layered structures and forming cavity 20 therebetween. Pet. 53–54 (citing, e.g., Ex. 1007 ¶¶ 43–45); *see* Ex. 1003, B26–B29. Moreover, Sato teaches that the dielectric layer may fill "top portions of the spaces" between the layered structures, and the voids may extend to or above the top of the

layered structures. Pet. 62 (citing Ex. 1007, Fig. 9(b)); *see* Ex. 1003 ¶ 79, B29. Petitioner argues persuasively that Sato teaches this limitation.

Petitioner argues that Sato and Lee teach or suggest that "layered structures including at least the charge storage elements and the control gates are separated in the second direction by distances that are less than one-fifth of a thickness of the layered structures." Pet. 50–53; *see* Ex. 1001, 9:50–53 (claim 1), 10:7–10 (claim 2). In particular, Sato teaches that memory cell structures may be formed as stacks of layers including charge storage elements and control gates. Pet. 50–51 (citing Ex. 1007 ¶¶ 3, 41, 42 (disclosing memory cell structures including floating gate electrodes 6 and control gate electrodes 8)). Although Petitioner acknowledges that "Sato does not expressly disclose is an embodiment wherein the gate-to-gate spacing in the second column direction (the spacing 10 and 11) is less than one fifth of the height of the conventional stack structures as required by this limitation (*id.* at 51–52)," Petitioner argues that a person of ordinary skill in the art would have found that spacing obvious based on the combined teachings of Sato and Lee (*id.*).

Initially, Petitioner notes that "Sato discloses exemplary height dimensions for the components of the memory cell structures which, *when summed*, have a total height from the substrate of between 790 and 1290 nm." *Id*. at 51–52 (emphasis added; citing Ex. 1007 ¶ 42; Ex. 1003, B21–B22). Consequently, Sato allegedly teaches a layered structure thickness of 0.79–1.29 μm. Further, as noted above, Lee teaches that gate-to-gate spacings between memory cell electrodes may be 0.12 μm or less. *Id.* (citing Ex. 1006, 2, 4); *see* Ex. 1007 ¶ 8 ("In recent years, with the increasing integration of semiconductor integrated circuits, there have been

increasing demands for the miniaturized station even of the semiconductor memory array devices comprised of the EEPROM cells configuring floating gate structures."); Ex. 1003 ¶ 108 ("These market pressures would have motivated a person of ordinary skill in the art to combine the memory cells in Sato with the reduced gate to gate spacing disclosed in Lee."). Thus, in view of Lee's teachings regarding spacings and Sato's recognition of the demand for miniaturization, Petitioner argues that Sato and Lee teach layered structures including floating gates and control gates separated in the second direction by distances that are less than one-fifth (0.12 μm/0.79 μm to 0.12 μm/1.29 μm) of a thickness of the layered structures, i.e., aspect ratios of 6.58:1 to 10.75:1. Pet. 52.

Petitioner argues that a person of ordinary skill in the art would have had sufficient reason to combine the teachings of Sato and Lee to achieve this recited relationship, because both Sato and Lee teach that the gate-to-gate spacings may be reduced, and it is desirable to do so in order to increase the memory cell density. *See* Ex. 1007 ¶ 8; Ex. 1006, 2. Further, it was known in the art to vary the spacing and the height of cells to achieve desired aspect ratios. Pet. 51–53; *see* Ex. 1018, 4:57–59;[11] *see also KSR*, 550 U.S. at 417 ("For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill."). We are persuaded that Sato and Lee teach this limitation.

[11] *See supra* Section II.B.5.

As noted above, the final limitations recited in independent claims 1 and 2 differ. In particular, claim 1 recites that "the charge storage elements are conductive floating gates and the elongated control gate lines extend downward between adjacent floating gates in the first direction." Ex. 1001, 9:58–61. Petitioner argues that Sato teaches this limitation. Pet. 55. In particular, referring to Sato's Figure 9(b), Sato teaches that the "charge storage elements" are floating gate electrodes 6, which have control gate electrodes 8 that extend across a plurality of floating gate electrodes 6 in a row. *Id*. (citing Ex. 1007 ¶¶ 42, 43). Further, because Sato's floating gate electrodes 6 include a polysilicon film, they are conductive. *See* Ex. 1007 ¶ 43. In addition, control gate electrodes 8 extend across and downward between adjacent floating gates in the first row direction. *See id*. ¶ 43 (describing formation of control gate electrodes). Consequently, we are persuaded that Sato teaches this limitation.

Claim 2 recites that "the control gate lines include word lines extending in the first direction along rows of charge storage elements and the charge storage elements form, along columns in the second direction, series strings of a plurality of charge storage transistors." Ex. 1001, 10:15–17. Petitioner argues that Sato and Lee teach this limitation. Pet. 56–57. As discussed above, Sato teaches elongated control gates that extend across a plurality of floating gate electrodes in the first row direction. *Id*. at 48 (citing Ex. 1007 ¶¶ 42, 43). Petitioner acknowledges that "Sato does not expressly disclose . . . a NAND configuration wherein the floating gates are arranged as a 'series strings of a plurality of charge storage transistors' in the second direction, and that the control gates are 'word lines.'" *Id*. at 56; *see*

Ex. 1003, B35–B36. Nevertheless, Petitioner argues that these missing limitations are taught by Lee.

Referring to Lee's Figure 1, Lee teaches "a NAND array with 16-cell NAND memory transistor strings in the bit line (i.e. column) direction, and the control gates are word lines extending along floating gates in the first row direction." *Id*. at 56 (citing Ex. 1006, 2–3). Dr. Baker testifies that "NAND type arrays in which the memory cells are connected as series strings of a plurality of transistors in the column direction was one of the most common flash memory array configurations in use in the 2002-2003 time frame." Ex. 1003 ¶ 50; *see id*. ¶¶ 35–36. Consequently, Dr. Baker testifies that a person of ordinary skill in the art would have had reason "to arrange the floating-gate type EEPROM cells in Sato as a NAND array such as disclosed in Lee," to achieve this limitation. Ex. 1003 ¶ 109. We are persuaded that Sato and Lee teach this limitation.

Petitioner argues that a person of ordinary skill in the art would have had several reasons to combine the teachings of Sato and Lee to achieve the apparatus recited in challenged claims 1 and 2. Pet. 44–46; *see* Ex. 1003 ¶¶ 103–108. First, Dr. Baker testifies that the combined teachings of Sato and Lee are merely a combination of known elements according to known methods to yield predictable results. Ex. 1003 ¶ 104. In particular, because of the similarities in the structure and function of the memory devices taught by Sato and Lee, Dr. Baker testifies that a person of ordinary skill in the art would have had reason to apply the teachings of one reference to the other. *Id*. Second, Dr. Baker testifies that a person of ordinary skill in the art would have had reason to combine the teachings of Sato and Lee because the teachings of each reference are directed to the common problem of "parasitic

capacitance between floating gates of an EEPROM memory array due to increased cell density." *Id*. ¶ 105 (citing Ex. 1007 ¶ 11; Ex. 1006, 2); *see KSR*, 550 U.S. at. 417 ("When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one."). Third, Dr. Baker testifies that, because Sato and Lee share a common goal of reduced gate-to-gate spacing and because Sato and Lee teach improved results in the presence of voids (*see* Ex. 1007 ¶¶ 43–45, 16:43–59; Ex. 1006, 4), a person of ordinary skill in the art would have had reason to combine known techniques to achieve predictable results. Ex. 1003 ¶ 106. Fourth, Dr. Baker testifies, referring to Figures 9(a) and 9(b), Sato teaches that spacing 10 between adjacent floating gates and spacing 11 between adjacent control gates may be "less than 0.3 μm" or "less than 0.5 μm." *Id*. ¶ 107 (citing Ex. 1007 ¶¶ 8, 11). Sato further teaches that microminiaturization of the spacing between floating gates and control gates may be "taken further than in the related art" while still suppressing the effects of parasitic capacitance. *Id*. (citing Ex. 1007 ¶ 41). Consequently, Dr. Baker testifies that persons of ordinary skill in the art would have had reason to look to known techniques for fabricating memory cell arrays with reduced gate-to-gate spacing, such as those taught by Lee. *Id*.; see Ex. 1006, 1–2; *see also KSR*, 550 U.S. at 420 ("Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed."). Thus, Dr. Baker testifies that a person of ordinary skill in the art would have had reason to increase the aspect ratio of the memory cells, such as those taught by Sato and Lee, to

achieve better isolation of the floating gate electrodes. *Id*. ¶¶ 104–108; *see Ethicon*, 844 F.3d at 1351. We find Dr. Baker's testimony credible.

We find that Petitioner argues persuasively that the combined teachings of Sato and Lee teach or suggest all of the limitations of independent claims 1 and 2 and that a person of ordinary skill in the art would have had reason to combine their teachings to achieve the apparatus recited in these claims.

b. Patent Owner's Contentions

Patent Owner contends that Petitioner fails to demonstrate that the combined teachings of Sato and Lee render claims 1–6 unpatentable for two reasons. PO Resp. 2–4.

i. Nonconformal deposition processes

First, Patent Owner contends that Petitioner fails to demonstrate that a person of ordinary skill in the art would have had a reasonable expectation of success in making or implementing the claimed invention by combining the teachings of Sato and Lee. *Id*. at 16–23. In particular, Patent Owner contends (1) that the combined teachings of Sato and Lee fails to teach or disclose the necessary deposition processes for intentional formation of voids in "a consistent and reproducible manner" (*id*. at 16–19) and (2) that "the knowledge of, and need for, the non-conformal deposition processes taught by the '849 patent would have been outside the scope of knowledge and skill of a person of ordinary skill in the art at the time of the invention" (*id*. at 19–23). For the reasons set forth below, we disagree.

Initially, Patent Owner contends that, in order to have been able to make or implement the claimed invention, a person of ordinary skill in the

art would have had to have been aware of the unsuitability of the conformal LPCVD and APCVD deposition processes taught by the applied art and that an "entirely different and even more complex non-conformal processes such as PECVD or PVD with sputtering would be necessary." *Id*. at 16; *see supra* Section II.B.5.b.i. Dr. Ho testifies as to the differences between conformal and nonconformal processes. Ex. 2001 ¶ 103. Dr. Ho's Figure 7 is reproduced above (*see supra* Section II.B.5.b.i.), along with a description of Figure 7. *Id*.

Patent Owner contends that neither Sato nor Lee teaches or suggests a nonconformal deposition process. PO Resp. 18–19. Consequently, Patent Owner concludes that neither Sato nor Lee teaches or suggests the type of deposition processes for the intentional formation of voids that are "necessary" to achieve that apparatus claimed in the '849 patent. *Id*. at 16 ("instead, entirely different and even more complex non-conformal processes such as PECVD or PVD with sputtering would be *necessary*" (emphasis added)). Hence, Patent Owner contends that a person of ordinary skill in the art would not be able to achieve the apparatus recited in the challenged claims.

Patent Owner's contentions are not persuasive for numerous reasons. First, as Patent Owner acknowledges, neither the '849 patent nor Sato is limited to "conformal" or "nonconformal" processes. Tr. 30:10–13 (Sato is not limited to conformal processes), 31:3–8 ("The methods [of the '849 patent] don't say conformal or non-conformal process."). Second, Patent Owner acknowledges that Sato teaches the creation of voids. *Id*. at 30:1–9. Dr. Ho further testified that "[y]ou cannot look at the final structure of the film and say that whether this is conformal or not conformal, per se."

Ex. 1035, 85:13–17. Thus, Sato's Figure 9(b) does not reveal whether the depicted voids were created by a conformal or nonconformal process. Ex. 1007, Fig. 9(b); *cf.* Ex. 1005, Fig. 16) (depicting voids). Third, not only does the '849 patent fail to mention a conformal or nonconformal process, the Specification of the '849 patent broadly describes the types of processes that may be used to form the voids, but does not require any specific process. Ex. 1001, 7:21–37; *see* Tr. 31:3–6. Further, the processes discussed by the parties were known at the time of the invention. *See* Ex. 1035, 23:20–22; Tr. 31:14–21. Fourth, Patent Owner applies an improper standard when it contends that the combined teachings of Sato and Lee fail to teach or disclose the necessary deposition processes for intentional formation of voids in a "consistent and reproducible manner." PO Resp. 16. As Petitioner explains, there is no requirement that the voids are made in such a manner. Pet. Reply 4–5.

As noted above, and perhaps most importantly, Patent Owner's contentions regarding conformal and nonconformal processes are based on a flawed presumption, namely, that the dielectric must be deposited on the side walls of the spaces between the adjacent layered structures. Claims 1 and 2 merely recite "dielectric material between the layered structures *in the second direction that fill top portions of spaces therebetween* while leaving voids between adjacent charge storage elements of the layered structures." Ex. 1001, 9:54–57 (claim 1), 10:11–14 (claim 2). Thus, the claims merely require that the top of the space is sealed to create a void below, that is, "between adjacent charge storage elements of the layered structures." Tr. 16:6–21, 21:3–16, 23:21–24:14; *see* Pet. Reply 15–16. The Specification of the '849 patent makes this clear when it states that the isolation or void "is

formed in spaces between floating gates *at the bottom of stacks of layers* having a height of five, eight or more times the width of the spaces between the stacks," and that "*[t]op portions of the spaces are filled* with the dielectric, however, thereby leaving large voids sealed in the dielectric between the charge storage elements." Ex. 1001, 4:35–47 (emphases added). Thus, we are not persuaded that the challenged claims of the '849 patent require conformal or nonconformal deposition processes or that Sato and Lee fail to teach the formation of the recited voids, regardless of the possible processes used. Consequently, because we do not find that the '849 patent claims require the use of nonconformal processes, we also find unpersuasive Patent Owner's contention that the knowledge of and the need for the nonconformal deposition processes allegedly taught by the '849 patent would have been outside the scope of knowledge and skill of a person of ordinary skill in the art at the time of the invention or that, consequently, a person of ordinary skill in the art would not have a reasonable expectation of success in achieving the claimed apparatus based on the combined teachings of Sato and Lee. PO Resp. 19–23; *see* Pet. Reply 5–12.

ii. Filling Top Portions of the Spaces

Second, Patent Owner contends that Petitioner fails to demonstrate that the combined teachings of Sato and Lee teach dielectric material that fills top portions of spaces between layered structures. PO Resp. 24–29. In particular, Patent Owner contends that

> Sato does not teach this recited limitation of claim 6. The Board cited to claims 4-6 of Sato, characterizing those claims as providing a cavity "between each of said floating gate electrodes" or "between each of said control gate electrodes." Patent Owner respectfully submits, however, that neither the

> claims of Sato nor its specification limit the specific location of the cavity, as the Board seems to suggest.

Id. at 24 (citations omitted) (quoting Ex. 1007 ¶¶ 17–19, Claims 4–6). In particular, with respect to Sato's claim 4, Patent Owner contends the recitation that

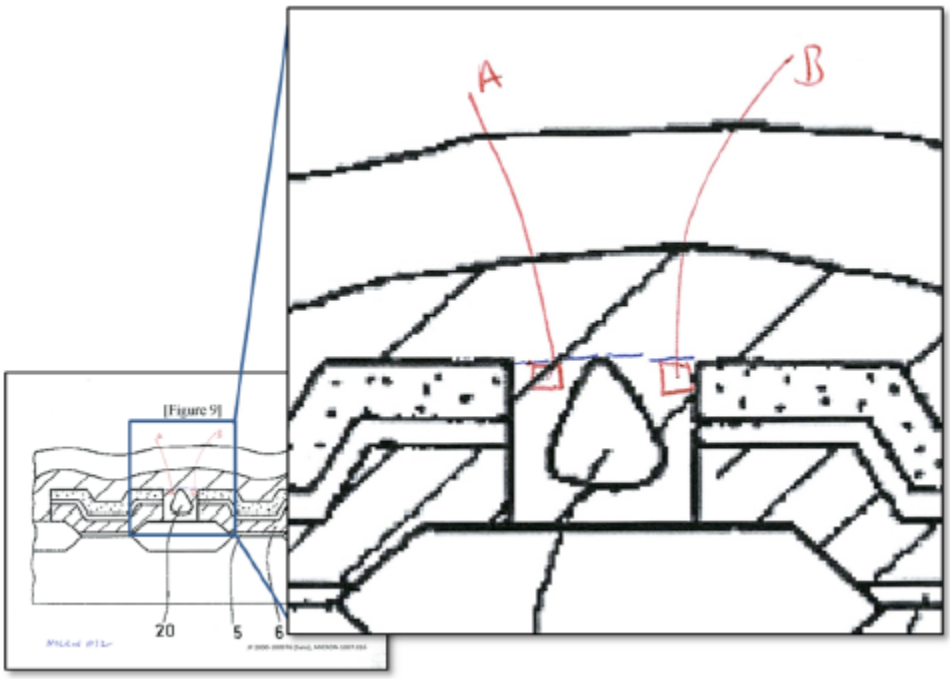
> "a cavity provided between each of said floating gate electrodes," does not mean that the cavity is only between the floating gate electrodes, and that it extends no higher. Rather, as any open-ended claim language, *it means that the cavity is at least between the floating gate electrodes, and that it can extend higher*. In other words, this claim language does not prescribe an upper limit of the cavity such that it extends no higher than the top level of the floating gates.

Id. at 24–25 (emphasis added). Thus, Patent Owner contends that, because the scope of the teaching of Sato's claim 4 is not definitive, Petitioner has failed to meet its burden of showing that the limitations of challenged claims 1 and 2 are taught by Sato and Lee. *Id*. at 25–26. Consequently, Patent Owner concludes that "[o]nly by being able to show that the upper limit of the void is below the upper limit of the spaces between the layered structures can Petitioner show that any part of the top portions of the spaces between the layered structures is filled with dielectric material." *Id*. at 26. We disagree with Patent Owner's conclusion.

Initially, we note that the language of claims 1 and 2 does not require that the voids end below the top portions or that the top portions are filled *entirely*, such that they include no portion of a void. Pet. Reply 15–16. Instead, claims 1 and 2 merely recite that dielectric material is (1) "between the layered structures in the second direction" and (2) "*top portions of spaces therebetween* [are filled] while leaving voids between adjacent charge storage elements of the layered structures." Ex. 1001, 9:54–57

(claim 1), 10:11–14 (claim 2). Thus, as long as "top portions" of the spaces between the layered structures are filled, this limitation of claims 1 and 2 is satisfied.

As Petitioner argues, Figure 4 of the '849 patent, which is reproduced above, appears to show voids 47 extending above the top of the layered structures. Pet. Reply 17. Moreover, Dr. Ho testified that Figure 4 of the '849 patent depicts the apparatus as recited in claims 1 and 2, as well as in claim 6. *Id*. (citing Ex. 1035, 60:4–61:3); *see* Ex. 1035, 63:23–64:1. Thus, even if Patent Owner is correct that the voids in Sato's Figure 9(b) extend to or above the tops of the adjacent layered structures, such a structure is not contrary to the language of claims 1 and 2, as that language would be understood in view of the Specification of the '849 patent. Pet. Reply 18–19. Further, during his deposition, Dr. Ho testified that the "top portions" taught by Sato are above the voids depicted in Sato's Figure 9(b). *Id*. at 21. The annotated Figure 9(b), showing Petitioner's annotations in red and Dr. Ho's annotations in blue, is reproduced below.



Ex. 1032, Fig. 9(b); *see* Ex. 1035, 61:8–63:15; *cf.* Pet. Reply 20 (reproducing Ex. 1030, Fig. 4 (as annotated)). Specifically, Dr. Ho annotated Sato's Figure 9(b) during the deposition to clearly indicate that the "top portions" are above the voids, separating them by a dashed blue line.

As the Patent Owner notes, drawings sometimes may not teach "precise proportions or particular sizes of objects when the specification is silent on the matter." *Hockerson-Halberstadt*, 222 F.3d at 956; *see* PO Resp. 28. Nevertheless, as noted above, we also do not ignore the teachings of the drawings, which clearly inform us that the voids may, but need not, extend above the level of the layered structures. *Marz*, 455 F.2d at 1072. Sato's drawings are not definitive on the size of the voids, but Dr. Ho's testimony is persuasive evidence of what a person of ordinary skill in the art would discern from these drawings. In particular, the depictions in the drawings and Dr. Ho's testimony teach that "top portions of spaces" may or may not be below the tops of the layered structures. Pet. Reply 22.

Accordingly, we are persuaded that Sato's teachings regarding the height of the voids are broad enough to encompass the recited limitations of claims 1 and 2.

Accordingly, after considering the arguments and evidence presented by each party, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the combined teachings of Sato and Lee would have rendered obvious claims 1 and 2 of the '849 patent.

c. Claims 3 and 4

Claims 3 and 4 are summarized above, and that summary is not repeated here. *See supra* Section I.B.5.c. Petitioner argues that the combined teachings of Sato and Lee render obvious the subject matter of claims 3 and 4. Pet. 57–58. Moreover, Dr. Baker provides a detailed mapping of the additional limitations of claims 3 and 4 onto Sato. Ex. 1003, B39–B41. In particular, with respect to claim 3, Petitioner argues that Sato teaches that silicon oxide film 19 is formed using "silane gas and oxygen." Pet. 58 (citing Ex. 1007 ¶ 43). Similarly, Petitioner argues that Lee teaches that "the dielectric material that fills the gate-to-gate spacing can be either silicon oxide or silicon nitride." *Id*. (citing Ex. 1006, 3). Further, with respect to claim 4, Petitioner argues that Sato teaches "floating-gate type memory cells wherein the charge storage element is a conductive polysilicon floating gate electrode 6 that stores electrical potential." *Id*.; *see* Ex. 1007 ¶¶ 41–43. We find Petitioner's arguments and evidence, including Dr. Baker's unrebutted testimony regarding the mapping of claims 3 and 4 on the teachings of Sato and Lee, persuasive.

Patent Owner does not contend that dependent claims 3 and 4 are separately patentable, but, instead, relies on its contentions with respect to

their base claim, claim 2. *See* PO Resp. 2–3. Because Patent Owner does not present arguments directed specifically to the recitations of claim 3 and 4, Patent Owner waives such arguments. *See* Paper 13, 3. In view of the analysis set forth above with respect to independent claim 2 (*see supra* Section II.C.3.a. and b.), Petitioner argues persuasively that the combined teachings of Sato and Lee would have rendered claims 3 and 4 obvious. Pet. 57–58; *see* Ex. 1003, B39–41. Thus, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the combined teachings of Sato and Lee would have rendered obvious claims 3 and 4 of the '849 patent.

d. Claim 5

Claim 5 is summarized above, and that summary is not repeated here. *See supra* Section I.B.5.d. Petitioner argues that the combined teachings of Sato and Lee render obvious the subject matter of claim 5. Pet. 58–59. Moreover, Dr. Baker provides a detailed mapping of the limitations of claim 5 onto Sato and Lee. Ex. 1003, B42. In particular, with respect to claim 5, Petitioner argues that "Lee discloses an exemplary nonvolatile EEPROM NAND memory array with gate-to-gate spacing of 0.12 μm and Sato discloses exemplary height dimensions for the components of the memory cell structures which, when summed, have a total height from the substrate of between 790 and 1290 nm." Pet. 51–52 (citing Ex. 1007 ¶ 42; Ex. 1006, 2, Fig. 1); *see* Ex. 1003 B16–B26 (claim limitation 1.3). Thus, Petitioner argues that the combined teachings of Sato and Lee teach "aspect ratios of between 6.58:1 to 10.75:1. In other words, Sato in view of Lee discloses wherein the height of the memory cell 'layered structures' is 6.58 to 10.75 times larger than the width between adjacent memory cells in the second

direction." Ex. 1007 ¶ 42; *see* Ex. 1003, B42. We find Petitioner's arguments and evidence, including Dr. Baker's testimony regarding the mapping of claim 5 on the teachings of Sato and Lee, persuasive.

Patent Owner does not contend that dependent claim 5 is separately patentable, but, instead, relies on its contentions with respect to its base claim, claim 2. *See* PO Resp. 2–3. Because Patent Owner does not present arguments directed specifically to the recitations of claim 5, Patent Owner waives such arguments. *See* Paper 13, 3. In view of the analysis set forth and summarized above with respect to independent claim 2 (*see supra* Section II.B.3.a. and b.), Petitioner argues persuasively that the combined teachings of Sato and Lee would have rendered claim 5 obvious. Pet. 58–59; *see* Ex. 1003, B42. Thus, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the combined teachings of Sato and Lee would have rendered obvious claim 5 of the '849 patent.

e. Claim 6

Claim 6 is summarized above, and that summary is not repeated here. *See supra* Section I.B.5.e. Petitioner argues that the combined teachings of Sato and Lee render obvious the subject matter of claim 6. Pet. 59–60. Moreover, Dr. Baker provides a detailed mapping of the limitations of claim 6 onto Sato and Lee. Ex. 1003, B43–B45. In particular, Petitioner argues that, referring to Sato's Figure 9(b), reproduced above (*see supra* Section II.C.2.), Sato teaches "a silicon oxide film 19 that is deposited so as to form a cavity between adjacent floating gate electrodes and control gate electrodes in the second column direction." Pet. 53–54. Further, Sato teaches that silicon oxide film 19 "is deposited in a single layer such that it

'overhangs' and fills the top portions of the spacing between memory cells, thus forming the cavity 20." *Id.* at 59–60 (citing Ex. 1007 ¶ 43).

Patent Owner does not contend that dependent claim 6 is separately patentable, but, instead, relies on its contentions with respect to its base claim, independent claim 2. *See* PO Resp. 2–3, 29–36. Because Patent Owner does not present arguments directed specifically to the recitations of claim 6, Patent Owner waives such arguments. *See* Paper 13, 3. In view of the analysis set forth and summarized above with respect to independent claim 2 (*see supra* Section II.C.3.a. and b.), Petitioner argues persuasively that the combined teachings of Sato and Lee would have rendered claim 6 obvious. Pet. 59–60; *see* Ex. 1003, B43–45. Thus, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the combined teachings of Sato and Lee would have rendered obvious claim 6 of the '849 patent.

f. Summary

Accordingly, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that the combined teachings of Sato and Lee would have rendered obvious claims 1–6 of the '849 patent.

III. CONCLUSION

For the foregoing reasons, we are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claims 1–6 are unpatentable under 35 U.S.C. 103(a) over the combined teachings of Takeuchi and Lee and over the combined teachings of Sato and Lee.

IV. ORDER

In consideration of the foregoing, it is hereby

ORDERED that claims 1–6 of the ’849 patent are unpatentable; and

FURTHER ORDERED that, because this Final Written Decision is final, a party to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

FOR PETITIONER:

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