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Paper 39
Entered: August 4, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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APPLE INC., HTC CORP., and HTC AMERICA, INC.,
Petitioners,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,
Patent Owner.

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Case IPR2016-00923[1]
Patent 5,812,789

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Before MICHAEL R. ZECHER, JAMES B. ARPIN, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

ZECHER, *Administrative Patent Judge*.

# FINAL WRITTEN DECISION
*Inter Partes* Review
*35 U.S.C. § 318(a) and 37 C.F.R. § 42.73*

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[1] Case IPR2016-00847 has been joined with this proceeding.

## I. BACKGROUND

Apple Inc. ("Apple") filed a Petition requesting an *inter partes* review of claims 1, 3–6, 11, and 13 ("the challenged claims") of U.S. Patent No. 5,812,789 (Ex. 1001, "the '789 patent"). Paper 2 ("Pet."). Patent Owner, Parthenon Unified Memory Architecture Limited Liability Corp., waived its right to file a Preliminary Response. Paper 8. We determined that the information presented in the Petition established that there was a reasonable likelihood that Apple would prevail in challenging claims 1, 3, 5, 11, and 13 of the '789 patent as unpatentable under 35 U.S.C. § 102(e), and claims 4 and 6 of the '789 patent as unpatentable under 35 U.S.C. § 103(a). Pursuant to 35 U.S.C. § 314, we instituted this *inter partes* review on August 23, 2016, as to all the challenged claims. Paper 10 ("Dec. on Inst.").

Upon instituting this proceeding, we considered a Petition filed by HTC Corp., HTC America, Inc., and LG Electronics, Inc. in Case IPR2016-00847 that challenged the same claims of the '789 patent at issue in this proceeding based on the same grounds of unpatentability. The Petition in Case IPR2016-00847 was accompanied by a Motion for Joinder that requested we join HTC Corp., HTC America, Inc., and LG Electronics, Inc. as parties to Case IPR2015-01944, which also challenged the same claims of the '789 patent at issue in this proceeding based on the same grounds of unpatentability. *HTC Corp. v. Parthenon Unified Memory Architecture LLC*, Case IPR2016-00847 (PTAB Apr. 7, 2016) (Papers 1 and 2). Based on a joint request by the parties in Case IPR2015-01944, we terminated that proceeding. *Samsung Elecs. Co. v. Parthenon Unified Memory Architecture LLC*, Case IPR2015-01944 (PTAB May 25, 2016) (Paper 12). We, nonetheless, authorized HTC Corp., HTC America, Inc., and LG

Electronics, Inc. to file a renewed or second motion for joinder seeking to join this proceeding. Case IPR2016-00847, Paper 11. Shortly thereafter, HTC Corp., HTC America, Inc., and LG Electronics, Inc. filed a Second Motion for Joinder. Case IPR2016-00847, Paper 12. Based on a joint request between LG Electronics, Inc. and Patent Owner, we terminated Case IPR2016-00847 only as to LG Electronics, Inc. Case IPR2016-00847, Paper 15. Pursuant to § 314(a), we instituted another *inter partes* review proceeding as to claims 1, 3–6, 11, and 13 of the '789 patent, and *granted* the Second Motion for Joinder only as to HTC Corp. and HTC America, Inc. (collectively, "HTC"). Paper 12.

During the course of trial, Patent Owner filed a Patent Owner Response. Paper 22 ("PO Resp."). Apple and HTC (collectively, "Petitioners") jointly filed a Reply to the Patent Owner Response. Paper 27 ("Pet. Reply"). A consolidated oral hearing with Case IPR2016-00924 was held on May 18, 2017, and a transcript of the hearing is included in the record. Paper 38 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1, 3–6, 11, and 13 of the '789 patent. For the reasons discussed below, we hold that Petitioners have demonstrated by a preponderance of the evidence that claims 1, 3, 5, 11, and 13 of the '789 patent are unpatentable under § 102(e), and claims 4 and 6 of the '789 patent are unpatentable under § 103(a).

### *A. Related Matters*

According to the parties, the '789 patent is involved in the following ten district court cases: (1) *Parthenon Unified Memory Architecture LLC v.*

*LG Electronics MobileComm, USA*, No. 2:15-cv-01950 (E.D. Tex.); (2) *Parthenon Unified Memory Architecture LLC v. Huawei Techs. Co.*, No. 2:14-cv-00687-JRG-RSP (E.D. Tex.); (3) *Parthenon Unified Memory Architecture LLC v. Motorola Mobility, Inc.*, No. 2:14-cv-00689-JRG-RSP (E.D. Tex.); (4) *Parthenon Unified Memory Architecture LLC v. HTC Corp.*, No. 2:14-cv-00690-RSP (E.D. Tex.); (5) *Parthenon Unified Memory Architecture LLC v. LG Electronics, Inc.*, No. 2:14-cv-00691-JRG-RSP (E.D. Tex.); (6) *Parthenon Unified Memory Architecture LLC v. Samsung Electronics Co.*, No. 2:14-cv-00902-JRG-RSP (E.D. Tex.); (7) *Parthenon Unified Memory Architecture LLC v. Qualcomm Inc.*, No. 2:14-cv-00930-JRG-RSP (E.D. Tex.); (8) *Parthenon Unified Memory Architecture LLC v. ZTE Corp.*, No. 2:15-cv-00225-JRG-RSP (E.D. Tex.); (9) *Parthenon Unified Memory Architecture LLC v. Apple, Inc.*, No. 2:15-cv-00621-JRG-RSP (E.D. Tex.); and (10) *STMicroelectronics, Inc. v. Motorola Inc.*, No. 4:03-cv-00276-LED (E.D. Tex.). Pet. 1–2;[2] Paper 32, 2. Petitioners also filed other petitions challenging the patentability of a certain subset of claims in related U.S. Patent No. 5,960,464 (Case IPR2016-00924).

### *B. The '789 Patent*

The '789 patent, titled "Video and/or Audio Decompression and/or Compression Device That Shares a Memory Interface," issued September

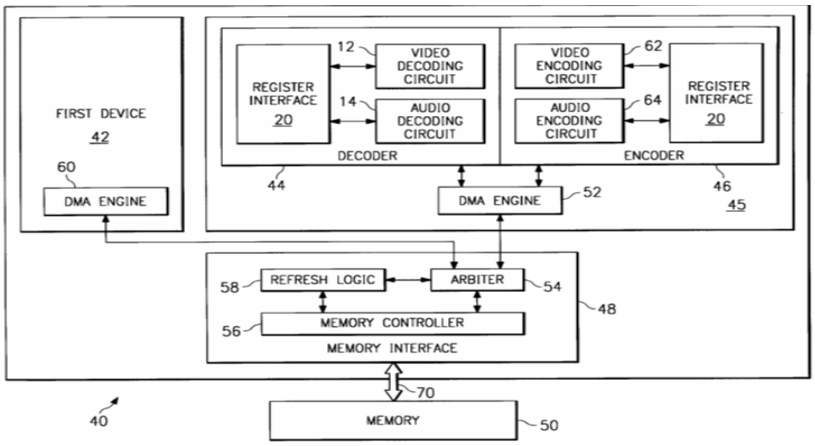
[2] The Petition and supporting evidence filed by HTC in Case IPR2016-00847 are essentially the same as the Petition and supporting evidence filed by Apple in Case IPR2016-00923. For clarity and ease of reference, all references to the Petition and supporting evidence throughout this Final Written Decision are to the Petition and supporting evidence filed by Apple in Case IPR2016-00923.

22, 1998, from U.S. Patent Application No. 08/702,911, filed on August 26, 1996. Ex. 1001, at [54], [45], [21], [22]. Because the application that led to the '789 patent was filed August 26, 1996, the '789 patent expired on August 26, 2016.

The '789 patent generally relates to an electronic system having a video or audio decompression/compression device and, in particular, to sharing a memory interface between such a device and another device in the electronic system. Ex. 1001, 1:18–23. In the Background section, the '789 patent discloses advantages associated with using encoders and decoders to compress and decompress video and audio sequences, respectively. *Id*. at 1:32–2:3. The '789 patent then proceeds to disclose the architecture of a conventional encoder/decoder prior to asserting that there are a number of problems associated with such an architecture. *Id*. at 2:4–25, Figs. 1a, 1b. According to the '789 patent, one of the problems includes dedicating memory to both the encoder and decoder, thereby increasing the cost of adding these components to an electronic system. *Id*. at 2:29–37.

The '789 patent purportedly solves this problem because the disclosed video or audio decompression/compression device does not need its own dedicated memory, but instead may share memory with another device and still operate in real time. Ex. 1001, 4:30–34. Figure 2 of the '789 patent, reproduced below, illustrates a diagram of an electronic system containing a device having a memory interface, as well as an encoder and decoder. *Id*. at 5:1–3.

FIG. 2




As shown in Figure 2 above, electronic system 40 includes first device 42, decoder 44, encoder 46, memory interface 48, and memory 50. Ex. 1001, 5:23–26. Each of first device 42, decoder 44, and encoder 46 access memory 50 through memory interface 48. *Id*. at 5:15–19. Memory interface 48 further includes arbiter 54 that is configured to arbitrate between first device 42, decoder 44, and encoder 46, when these components request access to memory 50. *Id*. at 6:15–18, 9:43–49.

### *C. Illustrative Claim*

Of the challenged claims, claim 1 is independent. Independent claim 1 is directed to an electronic system coupled to a memory. Each of claims 3–6, 11, and 13 directly or indirectly depends from independent claim 1. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. An electronic system coupled to a memory, comprising:
>
> a first device that requires access to the memory;
>
> a decoder that requires access to the memory sufficient to maintain real time operation; and
>
> a memory interface for coupling to the memory, and coupled to the first device and to the decoder, the memory

> interface having an arbiter for selectively providing access for the first device and the decoder to the memory and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.

Ex. 1001, 12:29–41.

*D. Prior Art Relied Upon*

Petitioners rely upon the following prior art references:

| **Inventor** | **U.S. Patent No.** | **Relevant Dates** | **Exhibit No.** |
|---|---|---|---|
| Artieri | 5,579,052 | issued Nov. 26, 1996, filed May 24, 1994 | 1036 |
| Lambrecht | 5,682,484 | issued Oct. 28, 1997, filed Nov. 20, 1995 | 1032 |

| **Non-Patent Literature** | **Exhibit No.** |
|---|---|
| Gordon E. Moore, *Cramming more components onto integrated circuits*, 38 ELECTRONICS (1965) ("Moore") | 1035 |

*E. Instituted Grounds of Unpatentability*

We instituted a trial based on the asserted grounds of unpatentability ("grounds") set forth in the table below. Dec. on Inst. 18.

| **Reference(s)** | **Basis** | **Claim(s) Challenged** |
|---|---|---|
| Lambrecht | § 102(e) | 1, 3, 5, 11, and 13 |
| Lambrecht and Artieri | § 103(a) | 4 |
| Lambrecht and Moore | § 103(a) | 6 |

## II. ANALYSIS

### *A. Claim Construction*

In an *inter partes* review proceeding, we generally construe claims in an unexpired patent by applying the broadest reasonable interpretation in light of the specification. 37 C.F.R. § 42.100(b). As we explain above, however, the '789 patent expired on August 26, 2016. Petitioners acknowledge as much when they assert that the '789 patent was set to expire in August 2016. Pet. 9–10.

As we explained in the Decision on Institution, because the '789 patent would expire shortly after we initiated this trial, we analyzed Petitioners' arguments through the lens of the claim construction standard that would apply to our Final Written Decision. *See* Dec. on Inst. 6–8. Thus, we construed the claims in accordance with the principles followed in district court. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc); *cf. In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) ("While claims are generally given their broadest possible scope during prosecution, the Board's review of the claims of an expired patent is similar to that of a district court's review." (citation omitted)).

"In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). The words of a claim generally are given their ordinary and customary meaning, and that is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent, including the specification.

*See Phillips*, 415 F.3d at 1312–13. Claims are not interpreted in a vacuum, but are a part of, and are read in light of, the specification. *See Slimfold Mfg. Co. v. Kinkead Indus., Inc.*, 810 F.2d 1113, 1116 (Fed. Cir. 1987). Although it is improper to read a limitation from the specification into the claims, the claims still must be read in view of the specification of which they are a part. *See Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1347 (Fed. Cir. 2004).

In the Decision on Institution, we addressed Petitioners' proposed constructions for the following two claim terms: (1) "video decoder" (claim 3); and (2) "real time" (all challenged claims). Dec. on Inst. 8–11. Upon reviewing the '789 patent in its entirety, we construed these claim terms as follows:

| **Claim Term** | **Construction** |
|---|---|
| "video decoder" | "hardware and/or software that translates data streams into video information" |
| "real time" | "[p]ertaining to a data-processing system that controls an ongoing process and delivers its outputs (or controls its inputs) not later than the time when these are needed for effective control" |

In its Patent Owner Response, Patent Owner does not address separately our initial constructions of these claim terms. *See* Paper 11, 3 ("The patent owner is cautioned that any arguments for patentability not raised in the response will be deemed waived."). Nor do Petitioners address our determinations in this regard in their Reply. *See* 37 C.F.R. § 42.23(b) ("A reply may only respond to arguments raised in the corresponding . . . patent owner response."). We, therefore, discern no reason to address or alter our initial construction of the claim terms "video decoder" and "real time" for the purposes of this Final Written Decision.

### *B. Anticipation by Lambrecht*

Petitioners contend that claims 1, 3, 5, 11, and 13 of the '789 patent are anticipated under § 102(e) by Lambrecht. Pet. 10–23. Petitioners explain how Lambrecht purportedly describes the subject matter of each challenged claim (*id*.), and rely upon the Declarations of Harold S. Stone, Ph.D. (Ex. 1030 ¶¶ 78–82; Ex. 1044 ¶¶ 2–20) to support their positions. In its Patent Owner Response, Patent Owner presents four arguments with respect to independent claim 1. PO Resp. 5–24. Patent Owner relies upon the Declaration of Mitchell A. Thornton, Ph.D., P.E., to support its positions. Ex. 2003 ¶¶ 39–60.

We begin our analysis with the principles of law that generally apply to a ground based on anticipation, followed by a brief overview of Lambrecht, and then we address the parties' contentions with respect to independent claim 1.

#### *1. Principles of Law*

To establish anticipation, "all of the elements and limitations of the claim must be shown in a single prior reference, arranged as in the claim." *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). When evaluating a single prior art reference in the context of anticipation, the reference must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). "'[T]he dispositive question regarding anticipation[, therefore, i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in that single reference." *Dayco Prods., Inc. v. Total Containment, Inc.*, 329

F.3d 1358, 1368 (Fed. Cir. 2003) (alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991)). We analyze this asserted ground based on anticipation with the principles stated above in mind.

### *2. Lambrecht Overview*

Lambrecht generally relates to a computer system that includes a system expansion bus, such as the Peripheral Component Interconnect ("PCI") bus, as well as a real time or multimedia bus that transfers periodic and/or multimedia data for real time, multimedia applications in order to increase system performance. Ex. 1032, 1:8–13. Figure 21 of Lambrecht, reproduced below, illustrates one embodiment of a computer system having a PCI bus that operates in different modes, one of which is a multimedia mode for high speed multimedia transfers. *Id*. at 6:59–61, 26:48–51.

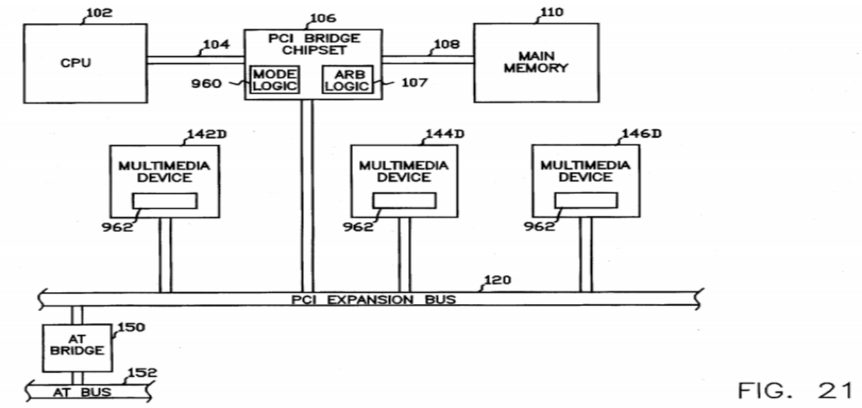



FIG. 21

As shown in Figure 21, the computer system includes central processing unit ("CPU") 102 coupled through CPU local bus 104 to PCI bridge chipset 106. Ex. 1032, 26:64–66. PCI bridge chipset 106 further includes various bridge logic, peripheral logic, arbitration logic 107, and mode logic 960. *Id*. at 26:66–27:3. PCI bridge chipset 106 is coupled to main memory 110 through memory bus 108. *Id*. at 27:4–5. Main memory

110 is preferably a dynamic random access memory, an extended data out memory, or other type of memory, as desired. *Id*. at 27:5–8. PCI bridge chipset 106 also interfaces with PCI bus 120 and uses mode logic 960 to place PCI bus 120 in either a normal PCI mode or in a real-time/multimedia mode optimized for multimedia transfers of periodic data. *Id*. at 27:10–11, 27:19–22. In this particular embodiment, multimedia bus 130 (not illustrated in Figure 21) optionally may augment or supplement PCI bus 120 when it is placed in multimedia mode. *Id*. at 27:29–31; *see also id*. at 27:62–65 (disclosing the same).

As further shown in Figure 21, one or more multimedia devices 142D–146D are coupled to PCI bus 120 and multimedia bus 130. Ex. 1032, 27:32–34. Multimedia devices 142D–146D are similar to multimedia devices 142–146 illustrated Figure 1 and may include, among other things, encoder or decoder devices. *Id*. at 27:43–50; *see also id. at* 8:13–19 (disclosing that various types of devices that may constitute multimedia devices 142–146 illustrated in Figure 1).

*3. Level of Skill in the Art*

There is evidence in the record before us that enables us to determine the knowledge level of a person of ordinary skill in the art. Relying on the testimony of its declarant, Dr. Stone, Petitioners assert that a person of ordinary skill in the art at the time of the invention of the ’789 patent would be an individual who possesses (1) an accredited Bachelor’s degree in electrical engineering, computer science, or computer engineering; and (2) at least three years of experience in the fields of data compression and overall computer system architecture. Pet. 10 (citing Ex. 1030 ¶¶ 74–77). Patent Owner’s declarant, Dr. Thornton, testifies that a person of ordinary skill in

the art at the time of the invention of the '789 patent would be an individual who possesses (1) an accredited Bachelor's degree in electrical engineering, computer engineering, *or an equivalent degree*; and (2) at least two to three years of experience in signal/image processing and computer architecture at both the systems and micro-architecture levels. Ex. 2003 ¶ 27. In lieu of the two to three years of experience, Dr. Thornton testifies that a person of ordinary skill in the art at the time of the invention of the '789 patent may hold a Master's or other graduate degree in electrical or computer engineering with a focus in computer architecture and signal/image processing, along with one year of relevant experience. *Id.*

Putting aside the subtle distinctions in the assessments of the level of skill in the art put forth by both declarants, Dr. Thornton testifies that, if he were to apply Dr. Stone's assessment of the level of skill in the art, his "analysis and conclusions would remain unchanged." Ex. 2003 ¶ 28. Because Dr. Stone's assessment of the level of skill in the art is consistent with the '789 patent and the asserted prior art, we adopt it and apply it to our evaluation below, but note that our conclusions would remain the same under Dr. Thornton's assessment.

*4. Claim 1*

In their Petitions, Petitioners rely upon the computer system in Figure 21 of Lambrecht to account for all the features required by independent claim 1. Pet. 10–19. An annotated version of Lambrecht's Figure 21 with Petitioners' corresponding claim mapping is reproduced below.

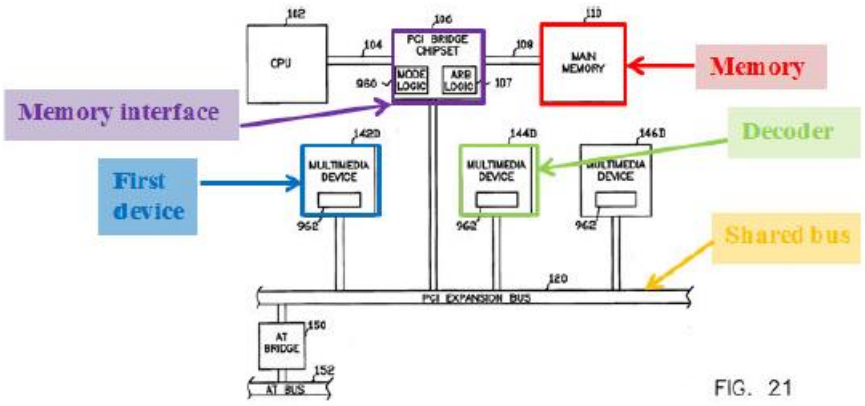



FIG. 21

Pet. 16; Pet. Reply 4. As shown in this annotated version of Lambrecht's Figure 21 above, Petitioners rely upon main memory 110, multimedia device 142D, multimedia device 144D, PCI bridge chipset 106, and PCI bus 120 to account for the shared "memory," "first device," "decoder," "memory interface," and "shared bus," respectively, as recited in independent claim 1. Pet. 12–19.

Petitioners then argue that Lambrecht discloses "a first device that requires access to memory" because multimedia device 142D accesses main memory 110 via PCI bus 120. Pet. 12–13 (citing Ex. 1032, 27:4–9, 27:32–34, 27:43–59; Ex. 1030 ¶ 78). Petitioners further argue that Lambrecht discloses "a decoder that requires access to the memory sufficient to maintain real time operation" because, when Lambrecht's PCI bus 120 is placed in multimedia mode, it allows multimedia device 144D sufficient access to main memory 110 in order to maintain real time operation. *Id.* at 13–14 (citing Ex. 1032, 27:32–34, 27:43–59; 27:66–28:2; Ex. 1030 ¶ 78). In addition, Petitioners argue that Lambrecht discloses "a memory interface for coupling to the memory, and coupled to the first device and to the decoder, the memory interface having an arbiter for selectively providing access for the first device and the decoder to memory,"

because PCI bridge chipset 106 includes arbitration logic 107 that selectively provides multimedia devices 142D and 144D access to (shared) main memory 110. *Id.* at 15–17 (citing Ex. 1032, 7:30–47, 26:66–27:9; Ex. 1030 ¶ 78).

Lastly, Petitioners argue that Lambrecht's PCI bus 120 describes the claimed "shared bus" because it is of "sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus." Pet. 17 (citing Ex. 1032, 5:33–48, 27:66–28:11; Ex. 1030 ¶ 78). According to Petitioners, Lambrecht's PCI bus 120 operates in a version of the multimedia mode called special "byte sliced mode," which allows for simultaneous, real time video and audio transfers and, as a result, provides sufficient bandwidth for both multimedia devices 142D and 144D to access (shared) main memory 110 simultaneously. *Id*. at 17–19 (citing Ex. 1032, 5:17–48, 19:39–54, 26:48–63, 27:66–28:11; Ex. 1030 ¶ 78).

In its Patent Owner Response, Patent Owner presents the following four arguments: (1) Lambrecht does not disclose "a shared bus . . . having a sufficient bandwidth to enable *the decoder to access the memory* and operate in real time"; (2) Lambrecht does not disclose "*a decoder* that requires access to the memory sufficient to maintain real time operation"; (3) Lambrecht does not disclose "a shared bus . . . having a sufficient bandwidth to enable the decoder to access the memory and *operate in real time*"; and (4) Lambrecht does not disclose "the bus having a sufficient bandwidth to enable the decoder to access the memory and *operate in real time when the first device simultaneously accesses the bus*." PO Resp. 6–24

(emphasis added by Patent Owner). We group Patent Owner's first and third arguments identified above and then address these arguments in turn.

*a. Lambrecht discloses "a shared bus . . . having a sufficient bandwidth to enable the decoder to access the memory and operate in real time," as recited in independent claim 1*

Independent claim 1 recites, in relevant part, "a shared bus . . . having a sufficient bandwidth to enable the decoder to access memory and operate in real time." Ex. 1001, 12:37–40.

In their Petitions, Petitioners contend that Lambrecht's PCI bus 120 describes the claimed "shared bus" because it is of "sufficient bandwidth to enable the decoder to access the memory and operate in real time." Pet. 17 (citing Ex. 1032, 5:33–48, 27:66–28:11; Ex. 1030 ¶ 78). According to Petitioners, Lambrecht's PCI bus 120 operates in a version of the multimedia mode called special "byte sliced mode," which allows for simultaneous, real time video and audio transfers and, as a result, provides sufficient bandwidth for both multimedia devices 142D and 144D to access (shared) main memory 110 simultaneously. *Id*. at 17–19 (citing Ex. 1032, 5:17–48, 19:39–54, 26:48–63, 27:66–28:11; Ex. 1030 ¶ 78); *see also id.* at 13–14 (arguing that, when Lambrecht's PCI bus 120 is placed in multimedia mode, it allows multimedia devices 142D and 144D sufficient access to main memory 110 in order to maintain real time operation) (citing Ex. 1032, 27:32–34, 27:43–59; 27:66–28:2; Ex. 1030 ¶ 78).

In its Patent Owner Response, Patent Owner's first and third arguments as to why Lambrecht does not disclose this disputed limitation presents the following layers of complexity: (1) whether Lambrecht discloses that multimedia device 144D is capable of accessing main memory 110 when PCI bus 120 is placed in multimedia mode; and (2) even assuming

Lambrecht discloses that multimedia device 144D is capable of accessing main memory 110 when PCI bus 120 is placed in multimedia mode, whether Lambrecht discloses that such access enables the multimedia device 144D to operate in real time. PO Resp. 6–13, 15–21. We address each in turn.

*i. Lambrecht's multimedia device 144D is capable of accessing main memory 110 when PCI bus 120 is placed in multimedia mode*

Patent Owner contends that, when Lambrecht's PCI bus 120 is placed in multimedia mode, it does not enable multimedia device 144D to access main memory 110. PO Resp. 6. According to Patent Owner, because the computer system illustrated in Lambrecht's Figure 21 is similar to the computer system illustrated in Lambrecht's Figure 1, one of ordinary skill in the art would have understood that these computer systems essentially operate in the same way. *Id.* at 7–8 (citing Ex. 2003 ¶ 41). Patent Owner then identifies three reasons why PCI bus 120 of Figure 21, when placed in multimedia mode, does not enable multimedia device 144D to access main memory 110. *Id.* at 8.

First, Patent Owner argues that multimedia bus 130 of Figure 1, which operates similar to PCI bus 120 in Figure 21, is not in communication with PCI bridge chipset 106 coupled to main memory 110 and, as a result, cannot transfer data from multimedia device 144 to main memory 110. PO Resp. 8–9 (citing Ex. 2003 ¶ 42). Second, Patent Owner argues that, when the PCI bus 120 of Figure 21 is placed in multimedia mode, it operates just like the multimedia bus 130 of Figure 1 to facilitate transfers between multimedia devices 142D–146D—not between multimedia device 144D and main memory 110. *Id.* at 9–10 (citing Ex. 1032, 8:8–28; Ex. 2003 ¶ 42). Third, Patent Owner argues that, because multimedia devices 142D–146D in

Figure 21 are the only devices equipped with interface logic 966 of bus interface circuitry 962 (i.e., purported software required to use the multimedia mode of PCI bus 120), one of ordinary skill in the art would have recognized that only multimedia devices 142D–146D are capable of using the multimedia mode of PCI bus 120 for data transfers. *Id.* at 10–13 (citing Ex. 1032, 26:48–60, 27:2–3, 27:18–22, 27:38–40, 27:57–62, 27:66–28:11, 28:15–19; Ex. 2003 ¶¶ 43–45).

In their Reply, Petitioners counter that Patent Owner's arguments ignore the express disclosures of Lambrecht's Figure 21 and attempt to limit the disclosure of this figure by improperly incorporating limitations from other embodiments, particularly those illustrated in Lambrecht's Figure 1. Pet. Reply 3, 5. Petitioners argue that Patent Owner's reliance on Lambrecht's Figure 1 is misplaced as the description of Lambrecht's Figure 21 explicitly states that mode logic 960 allows multimedia devices 142D–146D to "communicate with each other and with the CPU 102 and main memory 110 via the PCI bus 120, as is well known in the art." *Id.* at 6–7 (emphasis omitted) (quoting Ex. 1032, 27:57–59). Petitioners also argue that mode logic 960 allows multimedia devices 142D–146D to communicate date "using the PCI bus signal lines 120 when the PCI bus 120 is in the multimedia mode." *Id.* at 7 (emphasis omitted) (quoting Ex. 1032, 27:59–62). Based on these cited disclosures, Petitioners assert that Lambrecht explicitly discloses that PCI bus 120 in Figure 21, when placed in multimedia mode, provides for real time, multimedia data transfers between multimedia devices 142D–146D and main memory 110. *Id.* (citing Ex. 1044 ¶ 4).

In addition, Petitioners contend that there is nothing in reference to Lambrecht's Figure 21 that restricts the multimedia mode of PCI bus 120 to data transfers only between multimedia devices 142D–146D. Pet. Reply 7. Rather, Petitioners argue that Lambrecht's computer system illustrated in Figure 21 optionally provides for multimedia bus 130 "to augment or supplement" PCI bus 120 when it is placed in multimedia mode. *Id.* (quoting Ex. 1032, 27:30–31). According to Petitioners, providing optional multimedia bus 130 dedicated to enabling multimedia devices 142D–146D to transfer data there between does not require these devices to obtain bus mastership of PCI bus 120. *Id.* at 7–8 (citing Ex. 1032, 8:24–28; Ex. 1044 ¶ 5). With this in mind, Petitioners argue that Patent Owner's argument that PCI bus 120 in Figure 21, when placed in multimedia mode, is restricted to transferring data only between multimedia devices 142D–146D would render the optional inclusion of multimedia bus 130 redundant and unnecessary, as well as contradict the disclosure of other embodiments disclosed in Lambrecht, particularly that of Figure 6. *Id.* at 8–10 (citing Ex. 1032, 12:22–25, 12:29–31, 12:43–45; Ex. 1044 ¶¶ 6, 8). Petitioners also argue that Patent Owner's argument in this regard is contrary to the purpose of Lambrecht to "provide[] much greater performance for real-time applications." *Id.* at 10 (quoting Ex. 1032, Abstract) (citing Ex. 1044 ¶ 9).

Lastly, Petitioners disagree with Patent Owner's argument that, because multimedia devices 142D–146D in Figure 21 are the only devices equipped with interface logic 966 of bus interface circuitry 962, one of ordinary skill in the art would have recognized that only multimedia devices 142D–146D are capable of using the multimedia mode of PCI bus 120 for data transfers. Pet. Reply 12. Petitioners readily admit that only multimedia

devices 142D–146D in Figure 21 include interface logic 966, so that these devices can interface in multimedia mode, but, nonetheless, assert that Patent Owner overlooks other disclosures in Lambrecht. *Id.* (citing Ex. 1032, 27:38–40). In particular, Petitioners argue that Lambrecht's PCI bridge chipset 106 already possesses the capability to communicate with PCI bus 120 when it is placed in multimedia mode because (1) PCI bridge chipset 106 interfaces CPU 102 and main memory 110 with PCI bus 120; and (2) PCI bridge chipset 106 includes mode logic 960 for placing PCI bus 120 in either multimedia mode or normal PCI mode. *Id.* at 12–13 (citing Ex. 1032, 26:65–67, 27:4–5, 27:8–9, 27:19–22; Ex. 1044 ¶ 12). According to Petitioners, this capability of PCI bridge chipset 106 to communicate with PCI bus 120, when it is placed in multimedia mode, is further evidenced by the disclosure of Lambrecht's Figure 6, which includes chipset logic 106A that allows multimedia devices 142–146 to communicate with CPU 102 and main memory 110 via either PCI bus 120 or multimedia bus 130A. *Id.* at 13 (citing Ex. 1032, 12:23–25, 12:37–45; Ex. 1044 ¶ 13).

When considering Figure 21 and its corresponding description in Lambrecht together with the knowledge of one of ordinary skill in the art, we agree with Petitioners that, when Lambrecht's PCI bus 120 is placed in multimedia mode, it allows real time, multimedia data transfers between multimedia device 144D (which Petitioners identify as the decoder (Pet. 15)) and main memory 110. *See* Pet. 13–14, 17–19; Pet. Reply 3–7. Lambrecht discloses that "multimedia devices 142D–146D communicate with each other and with CPU 102 and main memory 110 via the PCI bus 120, as is well known in the art." Ex. 1032, 27:57–59. Lambrecht further discloses that "multimedia devices 142D–146D also communicate data between using

the PCI bus signal lines 120 when the PCI bus 120 is in the multimedia mode." *Id.* at 27:59–62; *see also id.* at Fig. 21 (illustrating how PCI bus 120 is coupled to multimedia devices 142D–146D and PCI bridge chipset 106, which, in turn, interfaces with main memory 110). Based on these disclosures, one of ordinary skill in the art would have understood that, in Figure 21 of Lambrecht, multimedia devices 142D–146D have access to main memory 110 in multimedia mode because Lambrecht discloses that multimedia devices 142D–146D communicate both with each other and main memory 110 via PCI bus 120, and also communicate data using the same PCI bus signal lines 120 when PCI bus 120 is in multimedia mode. *See* Ex. 1030 ¶ 78 (addressing the limitations recited in independent claim 1).

In addition, upon considering these cited disclosures in Lambrecht, Petitioners' declarant, Dr. Stone, testifies that one of ordinary skill in the art would have understood that, when PCI bus 120 in Figure 21 is placed in multimedia mode, it "provides for real-time[,] multimedia data transfers." Ex. 1044 ¶ 4. We credit Dr. Stone's testimony in this regard because it is consistent with Lambrecht's description of Figure 21. *See id.* (citing Ex. 1032, 26:53–56, 27:57–62). Moreover, there is nothing in reference to Figure 21 and its corresponding description suggesting that, when PCI bus 120 is placed in multimedia mode, multimedia device 144D is precluded from accessing main memory 110 and operating in real time.

Patent Owner's first and second reasons identified above, as well as the supporting testimony of its declarant, Dr. Thornton, are predicated on the notion that, because the computer system illustrated in Lambrecht's Figure 21 is similar to the computer system illustrated in Lambrecht's Figure 1, one

of ordinary skill in the art would have understood that these computer systems essentially operate in the same way. *See* PO Resp. 7–8; Ex. 2003 ¶¶ 40–42. Although Patent Owner and Dr. Thornton are correct that Lambrecht discloses that the computer system of Figure 21 is, indeed, "similar to" the computer system of Figure 1 (Ex. 1032, 26:51–52), these computer systems are not the same in all respects. We find that the similarities between these computer systems are limited to certain components that make up each computer system. That is, these computer systems each include CPU 102, CPU local bus 104, PCI bridge chipset 106, arbitration logic 107, memory bus 108, main memory 110, PCI bus 120, multimedia bus 130 (optional in Figure 21), and multimedia devices 142–146 (Figure 1), 142D–146D (Figure 21). *Compare* Ex. 1032, 7:30–8:2, Fig. 1, *with id.* at 26:64–27:56, Fig. 21. The similarities between these computer systems, however, end there. On the one hand, the computer system of Figure 1 depicts PCI bus 120 and multimedia bus 130 as mutually exclusive, and explicitly limits multimedia bus 130 to real time, multimedia transfers only between multimedia devices 142–146. *Id.* at 8:8–10, 8:23–25, Fig. 1 (illustrating how multimedia bus 130 only is coupled to multimedia devices 142–146 and not PCI bridge chipset 106). On the other hand, the computer system of Figure 21 depicts only PCI bus 120, which operates in one of two modes (i.e., a normal PCI mode or a real-time multimedia mode), and indicates that multimedia bus 130 is optional. Ex. 1032, 26:53–55, 27:23–25, Fig. 21; Ex. 1044 ¶ 4.

Put simply, the computer systems of Figure 1 and 21 are unique embodiments disclosed in Lambrecht, each of which operates in a different manner, including how their respective buses transfer data between the

multimedia devices, CPU, and shared memory. In essence, Patent Owner attempts to undermine Petitioners' position by advocating that the functionality of PCI bus 120 in Figure 21 should be limited to that of multimedia bus 130 in Figure 1. *See* PO Resp. 8. It is not entirely clear why Patent Owner compares multimedia bus 130 of Figure 1 to PCI bus 120 of Figure 21, as opposed to multimedia bus 130 of Figure 21. Putting this unusual comparison aside, we decline to adopt Patent Owner's position, which would suggest that we are improperly selecting disparate features from Lambrecht in determining whether a claim is anticipated (i.e., when PCI bus 120 in Figure 21 is placed in multimedia mode, we decline to limit it to real time, multimedia transfers only between multimedia devices 142D–146D in a manner similar to the functionality of multimedia bus 130 in Figure 1). *Cf. In re Arkley*, 455 F.2d 586, 587 (CCPA 1972) ("[T]he [prior art] reference must clearly and unequivocally disclose the claimed [invention] *or* direct those skilled in the art to the [invention] without any need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference." (emphasis added)).

Turning to Patent Owner's third reason identified above, we do not agree that, because multimedia devices 142D–146D in Figure 21 are the only devices equipped with interface logic 966 of bus interface circuitry 962, one of ordinary skill in the art would have recognized that only multimedia devices 142D–146D are capable of using the multimedia mode of PCI bus 120 for data transfers. *See* PO Resp. 10–13. Nor do we agree with Dr. Thornton's supporting testimony on this particular issue. *See* Ex. 2003 ¶¶ 43–45. Lambrecht discloses that PCI bridge chipset 106 is coupled to

both CPU 102 and main memory 110. Ex. 1032, 26:64–66, 27:4–5. PCI bridge chipset 106 includes mode logic 960, as well as a memory controller for interfacing with main memory 110. *Id.* at 27:2–3, 27:8–9. In particular, Lambrecht discloses that "mode logic 960 is operable to place PCI bus 120 in either a normal PCI mode or in a real-time/multimedia mode optimized for multimedia transfers of periodic data." *Id.* at 27:19–22; *see also id.* at 26:53–56 (disclosing the same). Petitioners' declarant, Dr. Stone, testifies that, because PCI bridge chipset 106 interfaces CPU 102 and main memory 110 with PCI bus 120, "a [person of ordinary skill in the art] would [have understood] that this mode logic [960] would be sufficient to interface PCI bus [120] to the main memory [110,] regardless of the PCI bus's communication mode." Ex. 1044 ¶ 12. We credit Dr. Stone's testimony in this regard because it is consistent with Lambrecht's descriptions of Figure 21 that we identify above.

Moreover, unlike Patent Owner's assertion and the supporting testimony of Dr. Thornton, Petitioners and the supporting testimony of Dr. Stone properly consider Lambrecht together with the knowledge that one of ordinary skill in the art would have derived from this prior art reference, as a whole. Dr. Stone testifies that, while using the multimedia mode of PCI bus 120 in Figure 21, "Lambrecht does not require any special logic in addition to the PCI bridge chipset [106] for the multimedia devices [142D–146D] to communicate with CPU [102] and main memory [110]." Ex. 1044 ¶ 13. We credit this testimony from Dr. Stone because it is consistent with Lambrecht, as a whole, specifically the embodiment illustrated in Figure 6. In this particular embodiment, Lambrecht discloses that PCI bridge chipset logic 106A communicates directly with multimedia bus 130A, thereby

allowing multimedia devices 142–146 to use multimedia bus 130A to access main memory 110, as desired. Ex. 1032, 12:37–45. Stated differently, Lambrecht does not disclose that PCI bridge chipset logic 106A in Figure 6 requires additional or special logic for it to allow multimedia devices 142–146 to transfer data to and from main memory 110 via multimedia bus 130A. Taking the knowledge that one of ordinary skilled in the art would have acquired from Figure 6 in Lambrecht and its corresponding description, there is no discernable reason as to why PCI bridge chipset 106 in Figure 21 would require the disclosure of additional or special logic beyond mode logic 960 in order to allow multimedia devices 142D–146D to use the multimedia mode of PCI bus 120 for real time data transfers with main memory 110.

*ii. Lambrecht enables multimedia device 144D operate in real time when PCI bus 120 is placed in multimedia mode*

Patent Owner reiterates its arguments that, when PCI bus 120 in Figure 21 of Lambrecht is placed in multimedia mode, it only transfers data between multimedia devices 142D–146D—not between multimedia device 144D and main memory 110. PO Resp. 17 (citing Ex. 2003 ¶ 51); *see also id.* at 19–20 (arguing the same). Patent Owner further contends that, even assuming PCI bus 120 in Figure 21 allows data transfers between multimedia device 144D and main memory 110 when it is placed in multimedia mode (which, according to Patent Owner, it does not), data could not be transferred between multimedia device 144D and main memory 110 in real time because data must be transmitted through PCI bridge chipset

106 and memory bus 108, neither of which are capable of supporting real time data transfers. *Id.* at 16–18 (citing Ex. 2003 ¶¶ 49–51).

In their Reply, Petitioners counter that Patent Owner's argument that placing PCI bus 120 in Figure 21 of Lambrecht in multimedia mode allows data transfers only between multimedia devices 142D–146D is incorrect because, as discussed above, these multimedia devices may access main memory 110 via PCI bus 120 in either the normal mode or multimedia mode. Pet. Reply 18. Petitioners also disagree with Patent Owner's argument that the computer system of Figure 21 cannot facilitate real time data transfers through PCI bridge chipset 106 and memory bus 108 because these components are not described specifically as being capable of operating in real time. *Id.* According to Petitioners, the '789 patent provides at least two examples as to what it means for a PCI bus to operate in real time—namely, the bus must have a bandwidth greater than 400 Mbytes per second. *Id.* at 18–19 (citing Ex. 1001, 6:29–32, 7:45–54, 8:57–62, 9:20–25). Petitioners assert that Lambrecht also discloses that its PCI bus may facilitate real time data transfers under the parameters identified in the '789 patent because Lambrecht incorporates by reference Shanley in its entirety, which, in turn, explains that a PCI bus may have a transfer rate of up to 524 Mbytes per second. *Id.* at 19 (citing Ex. 1032, 7:1–4; Ex. 1019, 31; Ex. 1044 ¶ 19). Relying on the reply declaration of Dr. Stone, Petitioners assert that one of ordinary skill in the art would have understood that Lambrecht's PCI bus 120 in Figure 21 is capable of supporting data transfers up to 524 Mbytes per second, which is greater than the 400 Mbyte per second transfer rate disclosed in the '789 patent as being

necessary to facilitate real time data transfers. *Id.* at 19–20 (citing Ex. 1044 ¶ 20).

As an initial matter, for the same reasons identified above, we agree with Petitioners that, when Lambrecht's PCI bus 120 is placed in multimedia mode, it allows real time, multimedia data transfers between multimedia device 144D and main memory 110. *See supra* Section II.B.4.a.i. That is, when considering Figure 21 and its corresponding description in Lambrecht together with the supporting testimony of Dr. Stone, one of ordinary skill in the art would have understood that, when PCI bus 120 is placed in multimedia mode, multimedia device 144D accesses main memory 110 and operates in real time. Ex. 1032, 27:57–62; Ex. 1044 ¶ 4.

As we explain above, we do not agree with Patent Owner's argument that, when PCI bus 120 in Figure 21 of Lambrecht is placed in multimedia mode, it transfers data only between multimedia devices 142D–146D—not between multimedia device 144D and main memory 110. *See* PO Resp. 17. This argument is predicated on the notion that, because Figure 1 and Figure 21 are similar, the embodiments depicted in these figures essentially operate in the same way by limiting the functionality of PCI bus 120 in Figure 21 to that of multimedia bus 130 in Figure 1. We decline to limit the functionality of PCI bus 120 in Figure 21 in this way as it would be improper to select disparate features from Lambrecht in determining whether a claim is anticipated. *Cf. Arkley*, 455 F.2d at 587.

We also do not agree with Patent Owner's argument that, even assuming PCI bus 120 allows data transfers between multimedia device 144D and main memory 110 when placed in multimedia mode, data could not be transferred between these two components in real time because data

must be transmitted through PCI bridge chipset 106 and memory bus 108, neither of which are capable of supporting real time data transfers. *See* PO Resp. 17–18. Nor do we credit the supporting testimony of its declarant, Dr. Thornton, on this particular issue. *See* Ex. 2003 ¶¶ 49–51. As we explain above, one of ordinary skill in the art would have understood that, in Figure 21 of Lambrecht, multimedia devices 142D–146D access main memory 110 in multimedia mode (*see supra* Section II.B.4.a.i (citing Ex. 1032, 27:57–62, Fig. 21)), which is a "mode optimized for real-time data transfers" (Ex. 1032, 27:67–28:2), and as Figure 21 illustrates, access to main memory 110 occurs via PCI bridge chipset 106 and memory bus 108.

Furthermore, how data is transferred in real time within the context of the '789 patent requires a closer look at the specification, particularly the disclosures regarding the bandwidth necessary for the "shared bus . . . to operate in real time," as claimed. The specification of the '789 provides a few general statements with respect to the bandwidth necessary for this bus to operate in real time. *See, e.g.*, Ex. 1001, 6:29–32 (disclosing that the bus "[has] a bandwidth greater than the bandwidth required for the decoder/encoder 45 to operate in real time"), 8:59–62 (disclosing the same), 9:23–25 (disclosing the same). In conjunction with two of these general statements, the specification discloses specific examples of what constitutes "a bandwidth greater than the bandwidth required for the decoder/encoder 45 to operate in real time"—namely, at least 400 Mbytes per second. *See*, *e.g.*, *id.* at 8:56–59 (disclosing that, in one embodiment, "the memory bus 167, which corresponds to the fast bus 70 [illustrated in Figure 2 of the '789 patent], . . . is capable of having a bandwidth of approximately 400

Mbytes/s"), 9:20–23 (disclosing essentially the same for another embodiment).

Although Lambrecht does not disclose explicitly the bandwidth of PCI bus 120 in Figure 21, it nonetheless incorporates by reference Shanley in its entirety. Ex. 1032, 7:1–4. Shanley, titled "PCI System Architecture" discloses that a PCI bus is capable of achieving "[t]ransfer rates of up to 524 Mbytes per second." Ex. 1019, 31.[3] Taking this knowledge that one of ordinary skill in the art would have acquired from Shanley, we credit the testimony of Petitioners' declarant, Dr. Stone, that Lambrecht's PCI bus (e.g., PCI bus 120 in Figure 21) "support[s] data transfer rates (e.g., memory reads or writes) up to 524 Mbytes per second, which is greater than the 400 Mbytes per second transfer rate [disclosed] in the '789 patent as being twice the bandwidth necessary to maintain real time operation of an MPEG decoder." Ex. 1044 ¶ 20. In other words, when considering Figure 21 and its corresponding description in Lambrecht together with the knowledge of one of ordinary skill in the art, we agree with Petitioners that, when PCI bus 120 is placed in multimedia mode, it supports data transfers at a rate sufficient to enable all the components coupled thereto, including PCI bridge chipset 106 that interfaces with main memory 110 via memory bus 108, to operate in real time. *See* Pet. Reply 18–20.

[3] All references to the page numbers in Shanley refer to the original page numbers located in the bottom right-hand or left-hand corner of each page in Exhibit 1019.

*b. Lambrecht discloses "a decoder that requires access to the memory sufficient to maintain real time operation," as recited in independent claim 1*

Independent claim 1 recites, in relevant part, "a decoder that requires access to the memory sufficient to maintain real time operation." Ex. 1001, 12:31–32.

In their Petitions, Petitioners contend that Lambrecht's multimedia device 144D coupled to PCI bus 120, and optionally coupled to multimedia bus 130, describes the claimed "decoder" because multimedia device 144D may constitute any one of a number of various input/out devices, including, among other things, Moving Picture Experts Group ("MPEG") decoder cards. Pet. 13–15 (citing Ex. 1032, 27:32–34, 27:43–56; Ex. 1030 ¶ 78). According to Petitioners, Lambrecht discloses that multimedia device 144D requires access to main memory 110 sufficient to operate in real time. *Id.* at 15 (citing Ex. 1032, 27:57–59, 27:66–28:2; Ex. 1030 ¶ 78).

In its Patent Owner Response, Patent Owner contends that, while Lambrecht's multimedia device 144D accesses main memory 110, it does not have the capability to maintain real time operation because Lambrecht does not disclose a bus that would allow such capability. PO Resp. 14 (citing Ex. 2003 ¶ 46). According to Patent Owner, Lambrecht contemplates multimedia devices that require their own dedicated multimedia memory. *Id.* at 14 (citing Ex. 1032, 20:57–65, Figs. 15, 16; Ex. 2003 ¶ 47). Patent Owner then asserts that, because Lambrecht discloses that the multimedia devices may have their own dedicated multimedia memories, and because Lambrecht discloses that the multimedia mode of PCI bus 120 in Figure 21 provides for real time transfer of multimedia data only among multimedia devices 142D–146D, a person of ordinary skill in the art would have

understood that previously decoded pictures must reside in dedicated memory present in the multimedia devices 142D–146D because the use of main memory 110 would violate the real time deadlines in accordance with the teachings of Lambrecht. *Id.* at 15 (Ex. 2003 ¶ 48).

In their Reply, Petitioners counter that Patent Owner's argument, once again, relies upon features from a different embodiment of Lambrecht (i.e., the embodiment in Figure 1) and assumes that these features apply to the embodiment in Figure 21. Pet. Reply 14. Petitioners maintain that, because Lambrecht's description of Figure 21 identifies an MPEG decoder as one of multimedia devices 142D–146D coupled to PCI bus 120, and these multimedia devices may access main memory 110 when PCI bus 120 is placed in the multimedia mode, Lambrecht discloses "a decoder that requires access to the memory," as claimed. *Id.* at 14–15 (citing Ex. 1032, 27:32–33, 27:51–56). Petitioners further argue that Patent Owner's assertion that multimedia devices 142D–146D must have their own dedicated memory runs directly counter to the purpose of Lambrecht's invention. *Id.* at 15. Petitioners also argue that Patent Owner's assertion in this regard is incorrect because it was known to those of ordinary skill in the art, prior to filing the '789 patent, that video decoders could either use dedicated multimedia memory, as evidenced by Figures 15 and 16 in Lambrecht, or access shared memory, as evidenced by Figures 6, 19, and 21 of Lambrecht. *Id.* at 16–17.

Upon reviewing Figure 21 and its corresponding description in Lambrecht, we agree with Petitioners that Lambrecht's multimedia device 144D discloses a decoder that accesses main memory 110 and operates in real time. *See* Pet. 13–15, 17–19; Pet. Reply 14–17. Lambrecht discloses that multimedia devices 142D–146D in Figure 21 "may be any of various

types of input/output devices," including, among other things, "MPEG decoder cards." Ex. 1032, 27:43–45, 27:50–56. As we explain above, Lambrecht further discloses that PCI bus 120, when placed in multimedia mode, provides for real time, multimedia data transfers between multimedia device 144D (i.e., the MPEG decoder) and main memory 110. *See supra* Section II.B.4.a.i.

We do not agree with Patent Owner's argument that, while Lambrecht's multimedia device 144D accesses main memory 110, it does not have the capability to maintain real time operation because Lambrecht does not disclose a bus that would allow such capability. *See* PO Resp. 14. Nor do we credit the supporting testimony of its declarant, Dr. Thornton, on this particular issue. *See* Ex. 2003 ¶ 46. Once again, this argument is predicated on the notion that, because Figure 1 and Figure 21 are similar, the embodiments depicted in these figures essentially operate in the same way by limiting the functionality of PCI bus 120 in Figure 21 to that of multimedia bus 130 in Figure 1. We decline to limit the functionality of PCI bus 120 in Figure 21 in this way as it would be improper to select disparate features from Lambrecht in determining whether a claim is anticipated. *Cf. Arkley*, 455 F.2d at 587.

We also do not agree with Patent Owner and Dr. Thornton that a person of ordinary skill in the art would have understood that previously decoded pictures must reside in dedicated memory present in each of Lambrecht's multimedia devices 142D–146D because the use of main memory 110 would violate the real time deadlines in accordance with the teachings of Lambrecht. *See* PO Resp. 15; Ex. 2003 ¶¶ 47, 48. This argument turns on whether Lambrecht's multimedia devices 142D–146D in

Figure 21 each require their own dedicated memory. Upon reviewing Figure 21 and its corresponding description, it is clear that multimedia devices 142D–146D share access to main memory 110. Ex. 1032, 27:57–59. This argument also is belied by other disclosures in Lambrecht. Indeed, Lambrecht itself serves as sufficient evidence that one of ordinary skill in the art would have understood that, prior to the '789 patent, decoders may either use their own dedicated memory, as evidenced by Figures 15 and 16, or share memory, as evidenced by Figures 6, 19, and 21. *Compare* Ex. 1032, 19:56–22:59 (disclosing embodiments where the multimedia devices have their own dedicated multimedia memory 160), *with id.* at 12:21–45, 24:40–28:11 (disclosing embodiments where the multimedia devices share main memory 110 with other components, such as CPU 102).

*c. Lambrecht discloses "the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus," as recited in independent claim 1*

Independent claim 1 recites, in relevant part, "the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus." Ex. 1001, 12:38–41.

In their Petitions, Petitioners contend that Lambrecht's PCI bus 120 describes the claimed "shared bus" because it is of "sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus." Pet. 17 (citing Ex. 1032, 5:33–48, 27:66–28:11; Ex. 1030 ¶ 78). According to Petitioners, Lambrecht's PCI bus 120 operates in a version of multimedia mode called "byte sliced mode," which allows for simultaneous, real time video and

audio transfers and, as a result, provides sufficient bandwidth for both multimedia devices 142D and device 144D to access (shared) main memory 110 simultaneously. *Id*. at 17–19 (citing Ex. 1032, 5:17–48, 19:39–54, 26:48–63, 27:66–28:11; Ex. 1030 ¶ 78).

In its Patent Owner Response, Patent Owner contends that, on the one hand, PCI bus 120 in Figure 21 must be placed in normal mode for multimedia device 142D to access main memory 110 because PCI bridge chipset 106 does not include additional or special logic that would allow multimedia device 142D to access main memory 110 when PCI bus 120 is placed in multimedia mode. PO Resp. 22–23 (Ex. 2003 ¶ 59). On the other hand, according to Patent Owner, one of ordinary skill in the art would have appreciated that multimedia device 144D must use PCI bus 120 in multimedia mode in order to access main memory 110 and operate in real time because, when PCI bus 120 is placed in normal mode, it is not capable of supporting the real time operation of multimedia device 144D. *Id.* at 23 (citing Ex. 1032, 1:60–2:2, 24:34–37). With these two scenarios in mind, Patent Owner argues that in order for multimedia devices 142D and 144D to access main memory 110 simultaneously, PCI bus 120 would have to be placed in both normal mode and multimedia mode at the same time. *Id.* (citing Ex. 2003 ¶ 59). Relying on the testimony of its declarant, Dr. Thornton, Patent Owner asserts that one of ordinary skill in the art would have understood that it is not possible for PCI bus 120 to be placed in both normal mode and multimedia mode at the same time and, as a result, it is not possible for PCI bus 120 to provide multimedia devices 142D and 144D simultaneous access to main memory 110. *Id.* at 23–24 (citing Ex. 1032, 27:18–22; Ex. 2003 ¶ 60).

In their Reply, Petitioners reiterate that neither PCI bridge chipset 106 nor main memory 110 in Figure 21 require any additional or special circuitry in order to communicate with multimedia devices 142D and 144D when the PCI bus 120 is placed in multimedia mode. Pet. Reply 20–21. Petitioners also argue that Patent Owner's assertion that it is impossible for PCI bus 120 to provide multimedia devices 142D and 144D simultaneous access to main memory 110 is based on the incorrect assumption that these multimedia devices cannot transfer data to and from main memory 110 when PCI bus 120 is placed in multimedia mode. *Id.* at 21. For essentially the same reasons identified above, Petitioners argue that Lambrecht's multimedia devices 142D and 144D communicate with main memory 110 when PCI bus 120 is placed in multimedia mode. *Id.* As one example, Petitioners argue that placing PCI bus 120 in multimedia mode may involve a special byte sliced mode, in which one multimedia device (e.g., multimedia device 142D) may transfer video data on PCI bus 120 to main memory 110 while at the same time another multimedia device (e.g., multimedia device 144D) may transfer audio data to main memory 110. *Id.* at 21–22 (citing Ex. 1032, 26:55–56, 28:3–5; Ex. 1043, 128:11–17).

We agree with Petitioners that, when Lambrecht's PCI bus 120 is placed in multimedia mode—specifically, the version of multimedia mode called special byte sliced mode—it possesses sufficient bandwidth to enable multimedia device 144D to access main memory 110 and operate in real time, even when multimedia device 142D accesses the PCI bus 120 simultaneously. *See* Pet. 17; Pet. Reply 20–21. Lambrecht discloses that the multimedia mode may include "placing . . . PCI bus 120 in a special mode optimized for real-time data transfers." Ex. 1032, 27:66–28:2. This special

"byte sliced mode . . . uses different byte lanes or channels of the PCI data lines for different types of multimedia transfers." *Id.* at 28:2–5. As just one example, "16 bits of the PCI bus [120] may be used for video transfers while the remaining 16 bites may be used for audio transfers simultaneously." *Id.* at 28:5–7. In other words, when PCI bus 120 in Figure 21 is placed in the version of multimedia mode called special byte sliced mode, it allows multimedia device 144D to gain access and transfer video data to/from main memory 110 in real time, while at the same time allowing multimedia device 142D to gain access and transfer audio data to/from main memory 110 in real time. During the cross-examination of Patent Owner's declarant, Dr. Thornton did not dispute that PCI bus 120 is capable of operating in this manner. *See* Ex. 1043, 128:11–17.

We do not agree with Patent Owner's argument that, PCI bus 120 in Figure 21 must operate in both normal mode and multimedia mode at the same time in order to allow multimedia devices 142D and 144D simultaneous access to main memory 110. *See* PO Resp. 22–24. Nor do we credit the supporting testimony of its declarant, Dr. Thornton, on this particular issue. *See* Ex. 2003 ¶¶ 59, 60. Contrary to this argument, and for essentially the same reasons identified above, we agree with Petitioners that, when Lambrecht's PCI bus 120 is placed in multimedia mode, it allows real time, multimedia data transfers between multimedia devices 142–146D and main memory 110. *See supra* Section II.B.4.a.i. That is, when considering Figure 21 and its corresponding description in Lambrecht together with the supporting testimony of Dr. Stone, one skilled in the art would have understood that, when PCI bus 120 is in multimedia mode, multimedia devices 142D–146D access main memory 110 and operate in real time.

Ex. 1032, 27:57–62; Ex. 1044 ¶ 4. In addition, based on our discussion above regarding how Lambrecht's PCI bus 120 may be placed in a version of multimedia mode called special byte sliced mode, multimedia devices 142D and 144D are capable of simultaneously accessing main memory 110 to transfer video and audio data in real time. Ex. 1032, 27:66–28:7.

To the extent both Patent Owner and Dr. Thornton reiterate that PCI bridge chipset 106 in Figure 21 does not include additional or special logic that would allow multimedia device 142D to access main memory 110 when PCI bus 120 is placed in multimedia mode, we do not agree. *See* PO Resp. 22–23; Ex. 2003 ¶ 59. As we explain above, taking the knowledge that one of ordinary skilled in the art would have acquired from Lambrecht, as a whole, there is no discernable reason as to why PCI bridge chipset 106 in Figure 21 would require the disclosure of additional or special logic beyond mode logic 960 in order to allow multimedia devices 142D–146D to use the multimedia mode of PCI bus 120 for real time data transfers with main memory 110. *See supra* Section II.B.4.a.i.

*d. Remaining limitations*

In its Patent Owner Response, Patent Owner does not address separately Petitioners' explanations and supporting evidence as to how Lambrecht discloses the remaining limitations recited in independent claim 1. *See generally* PO Resp. 6–24; Paper 11, 3. We have reviewed Petitioners' explanations and supporting evidence in this regard, and we agree with and adopt Petitioners' analysis showing that Lambrecht discloses these remaining limitations. *See* Pet. 11–13; Ex. 1030 ¶ 78.

*e. Summary*

Based on the record developed during trial, we conclude that Petitioners have demonstrated by a preponderance of the evidence that the subject matter of independent claim 1 is anticipated by Lambrecht.

*5. Claims 3, 5, 11, and 13*

In its Patent Owner Response, Patent Owner does not address separately Petitioners' explanations and supporting evidence as to how Lambrecht discloses the limitations recited in dependent claims 3, 5, 11, and 13. *See generally* PO Resp. 24. Rather, Patent Owner relies upon the same arguments it presents as to why Lambrecht does not disclose each and every limitation recited in independent claim 1 to rebut Petitioners' contentions that dependent claims 3, 5, 11, and 13 are anticipated by Lambrecht. *Id.* For the same reasons identified above with respect to independent claim 1, we do not agree with Patent Owner's arguments. *See supra* Section II.B.4. We have reviewed Petitioners' explanations and supporting evidence as to how Lambrecht discloses the limitations recited in these dependent claims, and we agree with and adopt Petitioners' analysis in this regard. Pet. 19–23; Ex. 1030 ¶¶ 79–82. Based on the record developed during trial, we conclude that Petitioners have demonstrated by a preponderance of the evidence that the subject matter of dependent claims 3, 5, 11, and 13 is anticipated by Lambrecht.

*C. Obviousness Based on the Combined Teachings of Lambrecht and Artieri*

Petitioners contend that dependent claim 4 of the '789 patent is unpatentable under § 103(a) over the combined teachings of Lambrecht and Artieri. Pet. 24–25. Petitioners explain how their proffered combination

teaches the subject matter of this challenged claim. *Id*. Petitioners also rely upon the Declaration of Dr. Stone to support their positions. Ex. 1030 ¶ 83. In its Patent Owner Response, Patent Owner does not address separately Petitioners' explanations and supporting evidence with respect to dependent claim 4, but rather directs us to its arguments in support of the patentability of independent claim 1. PO Resp. 24–25.

We begin our analysis with the principles of law that generally apply to a ground based on obviousness, followed by a brief overview of Artieri, and then we address Petitioners' contentions with respect to dependent claim 4.

*1. Principles of Law*

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze this asserted ground based on obviousness with the principles identified above in mind.

*2. Artieri Overview*

Artieri generally relates to picture processing systems and, in particular, to a system for decoding pictures that have been encoded in accordance with the MPEG standard. Ex. 1036, 1:7–9. According to Artieri, all MPEG decoders, especially those directed to the MPEG-2 standard, generally include a variable length decoder, a run-level decoder, an inverse quantizer circuit, an inverse discrete cosine transform circuit, a half-pixel filter, and a memory. *Id.* at 1:12–16, Fig. 1. These MPEG decoders input encoded data via one bus and output decoded data via another bus. *Id.* at 1:16–18. Between the input and output, the data passes through the variable length decoder, run-level decoder, inverse quantizer circuit, and inverse discrete cosine transform circuit. *Id.* at 1:18–21.

*3. Claim 4*

Claim 4 depends from independent claim 1, and further recites "wherein the decoder is capable of decoding a bitstream formatted to comply with the MPEG-2 standard." Ex. 1001, 12:48–50.

In their Petitions, Petitioners contend that, although Lambrecht does not disclose explicitly that its MPEG decoder (i.e., multimedia device 144D) is capable of decoding a bitstream formatted to comply with the MPEG-2 standard, it would have been obvious to one of ordinary skill in the art at the time of the invention of the '789 patent to modify Lambrecht's MPEG decoder such that it is capable performing MPEG-2 video decoding, as taught by Artieri. Pet. 24 (citing Ex. 1036, 1:6–18). According to Petitioners, the '789 patent readily admits that the MPEG-2 standard was already in use and well accepted. *Id.* at 25 (citing Ex. 1001, 1:33–67).

Petitioners then argue that, because the MPEG-2 standard was old and well known at the time of the invention of the '789 patent, its characteristics would have been understood and predictable to those of ordinary skill in the art. *Id.* (citing Ex. 1030 ¶ 83). Consequently, Petitioners assert that modifying Lambrecht's MPEG decoder to perform MPEG-2 video decoding, as taught by Artieri, would have been a combination of familiar elements in accordance with known methods to yield a predictable result. *Id.* (citing *KSR*, 550 U.S. at 416; Ex. 1030 ¶ 83).

In its Patent Owner Response, Patent Owner relies upon the same arguments it presents as to why Lambrecht does not disclose each and every limitation recited in independent claim 1 to rebut Petitioners' contentions that dependent claim 4 would have been obvious over the teachings of Lambrecht and Artieri. PO Resp. 24–25. For the same reasons identified above with respect to independent claim 1, we do not agree with Patent Owner's arguments. *See supra* Section II.B.4. In addition, we have reviewed Petitioners' explanations and supporting evidence as to how the combined teachings of Lambrecht and Artieri account for the additional limitation recited in dependent claim 4, as well as the articulated reason why a person of ordinary skill in the art would have combined the teachings of these prior art references, and we agree with and adopt Petitioners' analysis in this regard. Pet. 24–25.

Based on the record developed during trial, we conclude that Petitioners have demonstrated by a preponderance of the evidence that the subject matter of dependent claim 4 would have been obvious over the combined teachings of Lambrecht and Artieri.

### *D. Obviousness Based on the Combined Teachings of Lambrecht and Moore*

Petitioners contend that dependent claim 6 of the '789 patent is unpatentable under § 103(a) as obvious over the combined teachings of Lambrecht and Moore. Pet. 26–27. Petitioners explain how their proffered combination teaches the subject matter of this challenged claim. *Id.* Petitioners also rely upon the Declaration of Dr. Stone to support their positions. Ex. 1030 ¶ 84. In its Patent Owner Response, Patent Owner does not address separately Petitioners' explanations and supporting evidence with respect to dependent claim 6, but rather directs us to its arguments in support of the patentability of independent claim 1. PO Resp. 25.

We begin our analysis with a brief overview of Moore, and then we address Petitioners' contentions with respect to dependent claim 6.

#### *1. Moore Overview*

Moore generally relates to integrated electronics—both as they stand in the present and what they might become in the future. Ex. 1035, 1.[4] According to Moore, "[i]ntegrated electronics is established today." *Id.* at 2. Moore discloses that there are a number of advantages to integrated electronics, including "[r]educed cost" and "the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate." *Id.*

[4] All references to the page numbers in Moore refer to the page numbers inserted by Petitioners in the bottom left-hand corner of each page in Exhibit 1035.

*2. Claim 6*

Claim 6 depends from dependent claim 5, and further recites "wherein the decoder, the encoder and the memory interface are monolithically integrated into the first device." Ex. 1001, 12:53–55.

In their Petitions, Petitioners contend that, although Lambrecht does not disclose explicitly that its MPEG decoder (i.e., multimedia device 144D), encoder (i.e., multimedia device 146D), and memory interface (i.e., PCI bridge chipset 106) are integrated monolithically into the first device (i.e., multimedia device 142D), it would have been obvious to a person of ordinary skill in the art at the time of the invention of the '789 patent to integrate these components into a first device monolithically, as taught by Moore. Pet. 26 (Ex. 1035, 2; Ex. 1006; Ex. 1030 ¶ 84). Petitioners argue that, based on the integration teachings of Moore, one of ordinary skill in the art would have been motivated to apply those teachings to Lambrecht's computer system in Figure 21. *Id.* Petitioners also argue that, because chip integration was a well-known technique, its use with Lambrecht's computer system in Figure 21 would have led to predictable results. *Id.* at 26–27. Consequently, Petitioners assert that monolithically integrating Lambrecht's MPEG decoder, encoder, and memory interface into the claimed "first device," similar to the manner disclosed in Moore, would have been nothing more than a combination of familiar elements in accordance with known methods to yield a predictable result. *Id.* (citing *KSR*, 550 U.S. at 416; Ex. 1030 ¶ 84).

In its Patent Owner Response, Patent Owner relies upon the same arguments it presents as to why Lambrecht does not disclose each and every limitation recited in independent claim 1 to rebut Petitioners' contentions

that dependent claim 6 would have been obvious over the teachings of Lambrecht and Moore. PO Resp. 25. For the same reasons identified above with respect to independent claim 1, we do not agree with Patent Owner's arguments. *See supra* Section II.B.4. In addition, we have reviewed Petitioners' explanations and supporting evidence as to how the combined teachings of Lambrecht and Moore account for the additional limitation recited in dependent claim 6, as well as the articulated reason why a person of ordinary skill in the art would have combined the teachings of these prior art references, and we agree with and adopt Petitioners' analysis in this regard. Pet. 26–27.

Based on the record developed during trial, we conclude that Petitioners have demonstrated by a preponderance of the evidence that the subject matter of dependent claim 6 would have been obvious over the combined teachings of Lambrecht and Moore.

## III. CONCLUSION

Petitioners have demonstrated by a preponderance of the evidence that (1) claims 1, 3, 5, 11, and 13 of the '789 patent are unpatentable under § 102(e) as anticipated by Lambrecht; (2) claim 4 of the '789 patent is unpatentable under § 103(a) as obvious over the combined teachings of Lambrecht and Artieri; and (3) claim 6 of the '789 patent is unpatentable under § 103(a) as obvious over the combined teachings of Lambrecht and Moore.

## IV. ORDER

In consideration of the foregoing, it is

ORDERED that claims 1, 3–6, 11, and 13 of the ’789 patent are held to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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