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Paper No. 48
March 10, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.
Petitioner

v.

THE BOARD OF TRUSTEES OF THE UNIVERSITY OF ILLINOIS
Patent Owner

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Case IPR2013-00006
Patent 6,888,204 B1

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Before SALLY GARDNER LANE, BRYAN F. MOORE, and MICHAEL J. FITZPATRICK, *Administrative Patent Judges.*

FITZPATRICK, *Administrative Patent Judge.*

# FINAL WRITTEN DECISION
*35 U.S.C. § 318 and 37 C.F.R. § 42.73*

## BACKGROUND

Micron Technology, Inc. ("Micron") filed a Petition (Paper 3, "Pet.") requesting an *inter partes* review of all claims (i.e., claims 1-18) of U.S. Patent No. 6,888,204 B1 (the "'204 patent"). The Board of Trustees of the University of Illinois ("University") filed a Patent Owner Preliminary Response (Paper 11, "Prelim. Resp."). In a March 13, 2013, Decision to Institute (Paper 15, "Dec. on Pet."), the Board granted the Petition and instituted trial of all claims on the following grounds:

claims 1, 2, 4, and 5 as anticipated by Lisenker (Ex. 1004)[1];

claims 1, 2, 4-7, 9-16, and 18 as obvious over Lisenker;

claims 1, 2, 4-7, 9-16, and 18 as obvious over Lisenker and Gise (Ex. 1010)[2];

claim 3 as obvious over Lisenker, Gise, and Nicollian (Ex. 1012)[3];

claims 6-18 as obvious over Lisenker, Gise, and Ito (Ex. 1008)[4];

claim 10 as obvious over Lisenker, Gise, Ito, and Mikawa (Ex. 1005)[5].

claims 1-5 as obvious over Deal (Ex. 1009)[6] and Lisenker; and

claims 6-18 as obvious over Deal, Lisenker, and Ito.

Dec. on Pet. 27.

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[1] WO 94/19829 to Lisenker et al. (Sep. 1, 1994).
[2] PETER GISE & RICHARD BLANCHARD, SEMICONDUCTOR AND INTEGRATED CIRCUIT FABRICATION TECHNIQUES 129-131 (Reston Publishing Co., Inc. 1979).
[3] E.H. NICOLLIAN, *Electrical Properties of the Si-$SiO_2$ Interface and its Influence on Device Performance and Stability*, 14(5) J. VAC. SCI. TECHNOL. 1112 (Sept./Oct. 1977).
[4] US 4,980,307 to Ito et al. (Dec. 25, 1990).
[5] R.E. MIKAWA & P.M. LENAHAN, *Electron Spin Resonance Study of Interface States Induced by Electron Injection in Metal-Oxide-Semiconductor Devices*, 59 (6) J. APPL. PHYS. 2054 (Mar. 15, 1986).
[6] US 4,027,380 to Deal et al. (June 7, 1977).

After institution, the University filed a Patent Owner Response (Paper 24, "PO Resp."). In it, the University opposes the grounds of unpatentability on two general bases: (1) the Board's findings, in instituting trial, regarding Lisenker are incorrect; and (2) objective indicia prove the claims would not have been obvious. Micron filed a Reply (Paper 26). Oral hearing was held on December 9, 2013.[7]

The Board has jurisdiction under 35 U.S.C. § 6(c). This final written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during the trial. Issues and arguments raised prior to institution of trial, but not made during trial, are not addressed necessarily in this Decision.

As discussed below, Micron has shown by a preponderance of the evidence that claims 1-18 of the '204 patent are unpatentable.

A. Related Proceedings

Micron indicates that it is a named defendant in a pending district court case concerning the '204 patent brought by the University and captioned *The Board of Trustees of the University of Illinois v. Micron Technology, Inc.*, Case No. 2:11-cv-02288 (C.D. Ill.). Pet. 1.

Also, Micron filed two additional petitions, which we granted, for *inter partes* reviews of two related patents: IPR2013-00005, regarding U.S. Patent No. 6,444,533, and IPR2013-00008, regarding U.S. Patent No. 5,872,387.

[7] A transcript of the final hearing is included in the record.

B. The '204 Patent (Ex. 1002)

The '204 patent, titled "Semiconductor Devices And Methods For Same," is assigned to the University. Ex. 1002, 1. The '204 patent issued from U.S. Application Serial No. 09/160,657, filed September 25, 1998. *Id*.

The '204 patent "relates to methods for treating semiconductor devices or components thereof in order to reduce the degradation of semiconductor device characteristics over time." Ex. 1002, col. 1, ll. 22-25. In particular, the '204 patent discloses methods of treating a semiconductor device by passivation of (or annealing[8]) the device with deuterium, an isotope of hydrogen. *Id*. at col. 2, ll. 36-39; Prelim. Resp. 1. The '204 patent explains:

> [T]reatment with deuterium provides a reduction in the depassivation or "aging" of semiconductor devices due to hot-carrier effects. Such aging is evidenced, for example, by substantial degradations of threshold voltage, transconductance, or other device characteristics. In accordance with the present invention, semiconductor devices are fabricated using deuterium to condition the devices and stably reduce the extent of these degradations.

Ex. 1002, col. 3, ll. 40-48.

Prior to the '204 patent, passivation with hydrogen[9] was "a well-known and established practice in the fabrication of semiconductor devices" to remove defects that affect the operation of the devices. Ex. 1002, col. 1, ll. 26-28; Ex. 1001 (Reed Decl.) ¶¶ 13-14. According to the '204 patent, it

[8] Micron's witness testified that passivation is also referred to as annealing. Ex. 1001 (declaration of Michael L. Reed, Ph.D. ("Reed Decl.")) ¶ 14.
[9] Our use of the term "hydrogen" and the symbol "H" in this Decision refers to naturally occurring hydrogen, which we understand to be predominantly protium, but may include trace amounts of deuterium.

was "discovered that semiconductor devices, for example including MOS[10] devices, can be advantageously treated with deuterium to improve their operational characteristics." Ex. 1002, col. 2, ll. 32-36.

C. Illustrative Claim

Independent claim 1 is illustrative of the claimed subject matter and reads as follows:

> 1. A semiconductor device comprising an n-channel field effect transistor including a drain formed in a semiconductive layer, a source formed in said semiconductive layer, a channel extending between the drain and the source, a gate insulating layer over said channel, an interface between a semiconductive silicon layer and a gate insulating layer, and conductive contacts to said drain, source and on said gate insulating layer, said field effect transistor structurally characterized by the retention or deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature above about 200º C. so as to increase the resilience of the field effect transistor to hot electron effects during operation.

## ANALYSIS

A. Claim Construction

In an *inter partes* review, "[a] claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b). That construction must be consistent with the specification, and the claim language should be read in light of the specification, as it would be interpreted by one of ordinary skill in the art. *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed. Cir.

[10] MOS refers to metal oxide semiconductor. Ex. 1002, col. 1, ll. 44-45; Ex. 1001 ¶ 9.

2010). Thus, we give claim terms their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) ("The ordinary and customary meaning is the meaning that the term would have to a person of ordinary skill in the art in question.") (internal quotation marks omitted).

In instituting trial, we gave each claim term its broadest reasonable interpretation, as understood by one of ordinary skill in the art and consistent with the disclosure of the '204 patent, as neither party had argued persuasively that any claim or term should be construed otherwise. Micron pointed out that the claims should be interpreted as product-by-process claims. Pet. 13. We agree.

*1. Claim 1*

Claim 1, as corrected by a December 20, 2005, Certificate of Correction (Ex. 1003, 569), states:

> 1. A semiconductor device comprising an n-channel field effect transistor . . . structurally characterized by the retention of deuterium at said interface *resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature above about 200º C.* so as to increase the resilience of the field effect transistor to hot electron effects during operation (emphasis added).

"[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself." *In re Thorpe*, 777 F.2d 695, 697 (Fed. Cir. 1985). Thus, for patentability purposes, we look to the product claimed, not the process by which it is made. *See id*. ("If the product in a product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even

though the prior product was made by a difference process."); *Amgen Inc. v. F. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1366 (Fed. Cir. 2009) ("It has long been the case that an old product is not patentable even if it is made by a new process.") (citing *General Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938)). Claim 1 requires retention of deuterium at the interface. A reference teaching retention of deuterium at the interface meets this requirement even if formed by a process different than that which is recited, unless evidence is put forth establishing an unobvious difference between the claimed product and the prior art product. *See In re Marosi*, 710 F.2d 799, 803 (Fed. Cir. 1983).

The University maintains that the specific process recited by claim 1 (post-fabrication passivation in deuterium) is required by the claim under an exception to the product-by-process rule. PO Resp. 20 (citing *Greenliant Sys., Inc. v. Xicor LLC*, 692 F.3d 1261 (Fed. Cir. 2012)). In *Greenliant*, the court held:

> [T]here is an exception to this general rule that the process by which the product is made is irrelevant. . . . [I]f the process by which a product is made imparts structural and functional differences distinguishing the claimed product from the prior art, then those differences are relevant as evidence of no anticipation although they are not explicitly part of the claim.

*Greenliant*, 692 F.3d at 1268 (quotation marks omitted). The University alleges that the process recited in claim 1 imparts a structural and functional difference resulting in a lifetime extension of the semiconductor device of between 10 and 50 times. PO Resp. 21. In support, the University refers to "experimental data included in the specification of the '204 patent" but does not provide a citation. *Id.* In fact, the experimental data in the Specification does not link lifetime extension to *post-fabrication* passivation with

deuterium. Rather, it links lifetime extension to deuterium passivation in general (i.e., as opposed to the prior art method using hydrogen). *See* Ex. 1002, Figs. 2-3, col. 5, ll. 60-65 ("[D]ramatic decreases in the degradation of threshold voltage and transconductance are observed when deuterium is used to passivate the devices, as compared to hydrogen passivation (see FIGS. 2 and 3, respectively). These decreases represent practical lifetime improvements by factors of about ten to fifty . . . ."); col. 7, ll. 47-49 ("[T]ransistors sintered in deuterium typically exhibit lifetimes 10 times longer than those sintered in hydrogen.").

Although claim 1 requires retention of deuterium at the interface, a reference teaching retention of deuterium at the interface meets this requirement even if formed by a process different than that which is recited, unless evidence is put forth establishing an unobvious difference between the claimed product and the prior art product. *See In re Marosi*, 710 F.2d at 803.

*2. Claims 6, 10, 13, 14, and 15*

Each of independent claims 6, 10, 13, 14, and 15 is directed to a product that is defined, partially at least, by a recited process similar to the process in claim 1. Claims 6, 10, 13, and 14 require deuterium at the "interface" and claim 15[11] requires deuterium at the "interposed gate insulator film," but not as a result of any particular process. *See Thorpe*, 777 F.2d at 697; *Amgen*, 580 F.3d at 1366.

[11] Claim 15 was corrected by the December 20, 2005 Certificate of Correction. Ex. 1003, 569.

*3. Claim 9*

Claim 9 is dependent from claim 6 and additionally recites "deuterium atoms from said post-fabrication passivation covalently bonded at said interface." This too is a product-by-process limitation, which requires deuterium atoms covalently bonded at the interface, but not as a result of any particular process. *See Thorpe*, 777 F.2d at 697; *Amgen*, 580 F.3d at 1366.

B. Prior Art References In Trial

*4. Lisenker (Ex. 1004)*

Lisenker discloses "a method for producing semiconductor devices in which hydrogen-containing bonds in silicon dioxide are replaced with deuterium containing bonds. Specifically Si-H bonds are replaced with Si-D bonds and Si-OH bonds are replaced with Si-OD bonds." Ex. 1004, 5, l. 36 – 6, l. 3. Lisenker further discloses how the method may be carried out, stating:

> a silicon wafer is contacted with a deuterium containing material to form Si-D and Si-OD bonds in a silicon dioxide layer and on a silicon surface at an interface with the silicon dioxide layer. Typical silicon dioxide layers suitable for treatment according to the present invention include isolation oxides, gate oxides, and various other oxide layers commonly used with semiconductor devices. According to the invention, deuterium or a deuterium-containing material is directed onto the device by, for example, annealing in a deuterium containing atmosphere, and/or cleaning with a deuterium compound such as $D_2O$, $D_2SO_4$, and DCl. In general, any hydrogen containing material used in VLSI[12] fabrication can be replaced with corresponding deuterium containing material.

*Id*. at 4, ll. 20-34. Finally, Lisenker discloses the benefits of the method and

[12] VLSI stands for "very large scale integration." Ex. 1011 (THOMAS E. DILLINGER, VLSI ENGINEERING 4 (Prentice Hall, 1988)).

how those benefits are obtained, stating:

> The stability of oxide layers is improved in the present invention because the bond energy of the Si-H and Si-OH bonds is increased by replacing the hydrogen atoms with deuterium atoms. The Si-D and Si-OD bonds thus formed provide completed silicon dangling bonds that are less likely to break when exposed to electrical stresses. Therefore, the deuterium containing devices of the present invention have improved stability, quality, and reliability.

*Id.* at 4, l. 35 – 5, l. 5.

*5. Ito (Ex. 1008)*

Ito is titled "Process For Producing A Semiconductor Device Having A Silicon Oxynitride Insulative Film." Ex. 1008, 1. Ito discloses that "[t]he gate insulation film should have a thickness of from approximately 30 to 3000 angstroms." *Id*. at col. 9, ll. 41-43. Ito further discloses:

> The insulative film, which is formed by a nitridation of the thermal oxidation of the silicon substrate, has such a structure that this oxidation film is gradually converted to silicon oxynitride from the surface to the interior of this film.

*Id.* at col. 8, ll. 38-42.

*6. Nicollian (Ex. 1012)*

Nicollian discloses:

> The remaining problem is to maintain interface-trap and fixed-charge densities within specified limits during the life of the integrated circuit to insure stable operation. This stability is achieved by the use of coatings and encapsulants which isolate the device from its environment, and by operating the device at low temperatures so that changes in interface-trap and fixed-charge densities occur so slowly that device characteristics remain within specifications during device life.

Ex. 1012, 1121.

*7. Deal (Ex. 1009)*

Deal is titled "Complementary Insulated Gate Field Effect Transistor Structure And Process For Fabricating The Structure." Ex. 1009, 1. It discloses a field effect transistor with an interface between a semiconductive silicon layer and a gate oxide layer. *Id*. at col. 9, ll. 54-56. Deal further discloses:

> The complementary field-effect transistor structure is then completed as shown in FIG. 7 by applying conductive connectors and defining them to produce metal layer 50 which interconnects p-region 36d and n-region 37s and metal layers 51 and 52 which provide electrical contact with p-region 36s and n-region 37d, respectively. Interconnection of one source/drain region of the p-channel device and one source/drain region of the n-channel device produces a complementary field-effect circuit with the switching properties described above. . . . An anneal of the structure in a hydrogen-containing ambient in the temperature range of 350º-500º C. is carried out to minimize the fast interface state density, which also adversely affects threshold voltages and other device characteristics. Finally, scratch-protection layers and packaging is provided in accordance with established practices.

*Id*. at col. 9, ll. 33-53. Deal does not disclose using deuterium for the above-described annealing.

*8. Gise (Ex. 1010)*

Gise is titled "Semiconductor & Integrated Circuit Fabrication Techniques." Ex. 1010, 1. Gise discloses:

> Either during the alloy step or directly following it, the wafers are often exposed to a gas mixture containing hydrogen (or occasionally another gas). This step is usually called an "anneal" step. The anneal step is designed to optimize and stabilize device characteristics. Hydrogen is thought to combine with uncommitted atoms at or near the silicon-silicon

> dioxide interface, thus reducing their effect on device performance. Typical anneal temperatures are 400º – 500º C for times of 30 minutes to 60 minutes.

*Id.* at 130-31.

*9. Mikawa (Ex. 1005)*

Mikawa is titled "Electron Spin Resonance Study of Interface States Induced by Electron Injection in Metal-Oxide-Semiconductor Devices." Ex. 1005, 2054. Mikawa discloses:

> It has often been proposed that hydrogen is involved in the electron trapping event in thermal oxides on silicon. In order to test this notion, we have subjected some sets of dry MOS oxides (described earlier) to 10% $H_2$/90% $N_2$ anneals and others to 10% $D_2$/90% $N_2$ anneals.

Ex. 1005, 2057.

C. Claims 1, 2, 4, and 5 As Anticipated By Lisenker

Anticipation requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). A limitation is inherently described by a prior art reference if it is necessarily present in the reference. *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1377 (Fed. Cir. 2003).

*1. Claim 1*

Claim 1 requires "an n-channel field effect transistor including a drain formed in a semiconductive layer, a source formed in said semiconductive layer, a channel extending between the drain and the source, a gate insulating layer over said channel, an interface between a semiconductive

silicon layer and a gate insulating layer, and conductive contacts to said drain, source and on said gate insulating layer."

Lisenker expressly discloses a field effect transistor. Ex. 1004, 1, l. 16 (disclosing a "MOSFET")[13]; 11, l. 6 (disclosing "MOS transistors").[14] We credit the testimony of Dr. Reed that the Lisenker field effect transistor is of the n-channel type because "a disclosure referencing MOSFETs would be applicable to N-channel MOSFETs unless explicitly directed otherwise." Ex. 1001 ¶ 10. We also credit his testimony that "Lisenker's reference to MOSFET devices necessarily includes N-channel devices. For example, Lisenker's discussion of hot electrons (the N-type carrier) produced in the channel region indicates that the channel is N-type." *Id*. at ¶ 34 (citing Ex. 1004, col. 4, ll. 2-10). The University does not dispute that the Lisenker MOSFET is an n-channel field effect transistor.

Lisenker does not disclose expressly all of the sub-structures of the field effect transistor that are recited in claim 1. However, Micron argues that these structures are inherent to a MOSFET, based primarily on the following testimony of Dr. Reed:

> All MOSFETs have a gate insulating layer interposed between a semiconductor substrate, typically silicon, and a gate electrode. In the semiconductor layer, a channel extends between a drain and source. Electrical connections to the gate, source, and drain are made through ohmic contacts. Voltages are applied to these contacts in order to regulate the conductivity of the channel and the current flowing between the

[13] A MOSFET is a metal oxide semiconductor *field effect transistor*. Ex. 1002, col. 1, ll. 44-45 (emphasis added).
[14] Dr. Reed testified that "in the semiconductor industry, the term 'MOS transistor' is understood to mean MOS field effect transistor." Ex. 1001 ¶ 34.

> source and drain. These elements set forth above are necessarily present in a MOSFET such that the disclosure or discussion of a MOSFET in a reference would include the disclosure of each of its attendant elements.

Ex. 1001 ¶ 9; *see also* ¶ 34.

We find this testimony persuasive in establishing that Lisenker discloses "an n-channel field effect transistor including a drain formed in a semiconductive layer, a source formed in said semiconductive layer, a channel extending between the drain and the source, a gate insulating layer over said channel, an interface between a semiconductive silicon layer and a gate insulating layer, and conductive contacts to said drain, source and on said gate insulating layer" as required by claim 1. The University does not dispute that Lisenker discloses this limitation.

Claim 1 additionally requires the retention of deuterium at said interface so as to increase the resilience of the field effect transistor to hot electron effects during operation. The University argues that Lisenker does not enable retention of deuterium because it allegedly teaches deuterium passivation that occurs only prior to formation of the metal contacts (or pre-metallization passivation). PO Resp. 23-24. However, Lisenker is not so limited. It teaches the use of deuterium—as opposed to using hydrogen—"throughout the VLSI fabrication procedure." Ex. 1004, 8, ll. 29-30. And, although the University characterizes this teaching as an "isolated passage" (*see* PO Resp. 12), it is not. Lisenker includes numerous additional teachings that undermine the University's argument that Lisenker's use of deuterium is limited to pre-metallization passivation, including the following:

> "In general, any hydrogen containing material used in VLSI fabrication can be replaced with corresponding deuterium containing material." Ex. 1004, 4, ll. 32-34.
>
> "In one aspect of the present invention, VLSI fabrication flows employ deuterium contained compounds in many or all of the fabrication steps that would normally employ hydrogen or a hydrogen containing compound." *Id*. at 5, ll. 6-9.
>
> "The formation of Si-D and Si-OD bonds is accomplished in the present invention by contacting a silicon wafer with deuterium or a deuterium containing compound before, during, and/or after formation a device oxide layer." *Id*. at 6, ll. 10-14.
>
> "A typical fabrication procedure will include various doping, etching, annealing, deposition, cleaning, passivation, and oxidation steps. In each instance in which hydrogen or a hydrogen containing compound is employed, deuterium or a deuterium containing compound can be used in its place." *Id*. at 8, ll. 30-35.

The University implies that Micron witness Dr. Reed conceded, on cross-examination, that Lisenker is limited to pre-metallization passivation. In particular, the University directs us to the following testimony:

> Q. So Lisenker is teaching that one should not anneal the deuterium until after metallization?
>
> MR. RIFFE: Objection, form.
>
> THE WITNESS: That's not the way I read this.

PO Resp. 13 (citing Ex. 2013, 88, ll. 13-17). This testimony does not support the University's argument. As is evident on its face, counsel for the University asked Dr. Reed whether Lisenker was *limited* to post-metallization passivation, and he answered in the negative. That answer is

consistent with the disclosure of Lisenker. *See, e.g.*, Ex. 1004, 8, ll. 29-30 ("The present invention can be implemented throughout the VLSI fabrication procedure.").

In addition to enabling retention of deuterium, Lisenker also describes and claims it. For example, Lisenker discloses:

> The regions where the deuterated bonds provide the greatest benefit in terms of device performance is at the interface of silicon-silicon dioxide layers. Thus, the semiconductor devices of this invention will have at this interface a ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds that is substantially greater than ratio of naturally occurring deuterium to hydrogen.

Ex. 1004, 10, ll. 29-35; *see also id*. at 12, ll. 15-17 (Lisenker claim 3: "The semiconductor device of claim 2 wherein the ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds is greater than about 99:1.").

Claim 1 of the '204 patent requires an "increase in resilience of the field effect transistor to hot electron effects during operation." The University argues that: (1) the Decision to Institute found that this limitation is not disclosed expressly in Lisenker; and (2) the limitation also is not disclosed inherently in Lisenker. PO Resp. 23. Neither argument is persuasive.

Contrary to the University's assertion, we did find that Lisenker expressly discloses this limitation. *See* Paper 15, 17 (quoting Ex. 1004, 5, ll. 4-5 ("[D]euterium containing devices of the present invention have improved stability, quality, and reliability.")). Also, increased resilience to hot electron effects is an inherent result of greater deuterium retained at the interface. The University does not dispute that fact, and, indeed, it is the basis of the claims of its patent. PO Resp. 2; *see also King Pharms., Inc. v.*

*Eon Labs, Inc.*, 616 F.3d 1267, 1276 (Fed. Cir. 2010) ("Because the '128 patent discloses no more than taking metaxalone with food, to the extent such a method increases the bioavailability of metaxalone, the identical prior art method does as well."). Lisenker teaches devices having greater amounts of deuterium retained at the interface relative to other prior art devices and, therefore, having increased resilience.

Claim 1 is anticipated by Lisenker.

*2. Claims 2, 4, and 5*

Claims 2, 4, and 5 depend from claim 1. Claim 2 requires that the "gate insulating layer comprises silicon dioxide." Claim 4 requires that the "gate insulating layer comprises an oxide of silicon." Claim 5 requires that the "gate insulating layer comprises silicon dioxide or silicon oxy nitride."

Lisenker discloses all of these additional limitations, as it discloses the use of silicon as the semiconductive layer and silicon dioxide in the gate insulator. Ex. 1004, 4, ll. 20-27. The University does not dispute that Lisenker discloses these limitations.

Claims 2, 4, and 5 are anticipated by Lisenker.

D. Claims 1, 2, 4-7, 9-16, and 18 As Obvious Over Lisenker

*1. Claims 1, 2, 4, and 5*

For at least the reasons discussed above with respect to anticipation, the subject matter of claims 1, 2, 4, and 5 would have been obvious over Lisenker. Further, Dr. Reed testified that post-metallization passivation was a standard processing step in the prior art. Ex. 1001 ¶¶ 15, 35. The University does not dispute that testimony. Indeed, it previously conceded the fact during prosecution of the '204 patent. Ex. 1003, 458 ¶ 15 (declaration of Robert M. Wallace, Ph.D. citing a 1995 article and testifying

that "post metal hydrogen annealing had been in widespread use in the semiconductor industry for many years"). Dr. Reed notes Lisenker's teaching that any hydrogen-containing material used in VLSI fabrication can be replaced with corresponding deuterium-containing material, and concludes that "it would have been apparent to perform Lisenker's annealing process after the metallization steps have been performed." Ex. 1001 ¶¶ 35, 36.

In opposition, the University asserts that one of ordinary skill would have ignored the teachings of Lisenker. PO Resp. 9-11, 14. In particular, it argues that the fundamental theory underlying Lisenker's teachings is that "the Si-D bond is significantly stronger than the Si-H bond." *Id*. at 9 (providing no citation to Lisenker).[15] But, according to the University, Lisenker erroneously relies on energy values for bonds not at the interface. *Id*. at 10. The University further argues that a person of ordinary skill in the art at the time of the invention would have known that "the energies for Si-D and Si-H bond disassociation *at the silicon surface* are identical or substantially identical." *Id*. (emphasis added). Therefore, the University reasons, such a person "would have concluded that the teachings of Lisenker were immaterial to the problem facing the inventors of the '204 patent, *i.e*., how to solve for hot carrier effects involving bonds at the silicon substrate." *Id*. (citing *In re Young*, 927 F.2d 588 (Fed. Cir. 1991)).

Contrary to the implication of the University's argument, however, the scope of the prior art is not limited to solutions that are directed to the

[15] Lisenker states that "[t]he stability of oxide layers is improved in the present invention because the bond energy of the Si-H and Si-OH bonds is increased by replacing the hydrogen atoms with deuterium atoms." Ex. 1004, 4, l. 35 – 5, l. 1.

problem the patentees set out to solve. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 419 (2007) ("In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103."). Additionally, we disagree with the further implication that Lisenker is not concerned with solving for hot carrier effects involving bonds at the silicon surface (or silicon-silicon dioxide interface). *See* Ex. 1004, 4, ll. 2-12 (discussion by Lisenker of problems caused by hot electrons at the silicon-silicon dioxide interface); Fig. 1 (illustrating an improved silicon-silicon dioxide interface in accordance with the Lisenker invention).

Also, the University's reliance on *In re Young* is not persuasive. *Young* does not support the proposition that a prior art reference may be ignored. *Young*, 927 F.2d at 591 ("Even if tending to discredit [the] Carlisle [patent], [the] Knudsen [article] cannot remove Carlisle from the prior art. Patents are part of the literature of the art and are relevant for all they contain."). In *Young*, the court held that, "[w]hen prior art contains apparently conflicting references, the Board must weigh each reference for its power to suggest solutions to an artisan of ordinary skill." *Id*. Here, the University has presented evidence conflicting, allegedly, with Lisenker's underlying theory of operation. But, the University has not provided a reference conflicting with Lisenker's express teaching that "deuterium containing devices of the present invention have improved stability, quality, and reliability." Ex. 1004, 5, ll. 4-5. Accordingly, we are not persuaded that a person of ordinary skill in the art would have ignored Lisenker.

*2. Claims 6, 10, 13, 14, and 15*

Each of independent claims 6, 10, 13, 14, and 15 is similar to claim 1 and additionally requires a gate insulating/dielectric layer/film "having a thickness not exceeding about 55 Angstroms." We find that Lisenker, as discussed above and below, teaches the subject matter of these claims except for the thickness limitation.

The Supreme Court has held that the obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418. In that regard, we credit the testimony of Micron's witness, Dr. Reed, that, at the time of filing the '204 patent, it would have been apparent to one of ordinary skill in the art to reduce the thickness of the gate insulating film of Lisenker to about 55 Angstroms or less, consistent with the general, decades-long trend of device miniaturization in the semiconductor industry. Ex. 1001 ¶ 38.

We also credit Dr. Reed's testimony that, at the time of filing the '204 patent, others already had made gate insulating films having thicknesses of about 55 Angstroms or less. *Id*. at ¶¶ 39, 43. The combination of familiar elements according to known methods to achieve predictable results, such as reducing the thickness of the gate insulating film of Lisenker to 55 Angstroms or less, is likely to be obvious. *See KSR*, 550 U.S. at 416.

We further note that the University does not argue, or direct us to evidence, to show criticality of the thickness limitation, such that we might conclude that obviousness has not been shown. S*ee generally* PO Resp.; *see*

Prelim. Resp. 2. Rather, the University's prior art-based arguments are directed exclusively to Lisenker.

*3. Claims 7, 11, 12, and 16*

Claim 7 is dependent on claim 6 and additionally requires that the "gate insulating layer comprises silicon dioxide." Claim 11 is dependent on claim 10 and additionally requires that the "the semiconductive layer comprises silicon, and the gate dielectric film includes a silicon compound." Claim 12 is dependent on claim 11 and additionally requires that the "silicon compound comprises an oxygen or a nitrogen containing silicon compound." Claim 16 is dependent on claim 15 and additionally requires that the "gate insulator comprises an oxide of silicon."

Lisenker discloses all of these additional limitations, as it discloses the use of silicon as the semiconductive layer and silicon dioxide in the gate insulator. Ex. 1004, 4, ll. 20-27. The University does not dispute that Lisenker teaches these limitations.

*4. Claim 9*

Claim 9 is dependent on claim 6 and additionally recites "deuterium atoms from said post-fabrication passivation covalently bonded at said interface." We have construed this product-by-process limitation to require deuterium atoms covalently bonded at the interface, but not as a result of any particular process. Lisenker discloses deuterium atoms in covalent bonds at the interface. Ex. 1004, 5, ll. 15-24 ("Devices of this invention will preferably have substantial numbers of Si-H and/or Si-OH bonds replaced with Si-D and/or Si-OD bonds."); *see also id*. at Fig. 1 (illustrating deuterium atoms in covalent bonds at a silicon-silicon dioxide interface). The University does not dispute that Lisenker teaches this limitation.

*5. Claim 18*

Claim 18 is dependent on claim 15 and additionally requires that the "the field effect transistor comprises an n-channel device subject in operation to hot electron stress." As set forth above in the anticipation analysis, based on Dr. Reed's testimony, we find that Lisenker teaches the limitation of an n-channel field effect transistor. Ex. 1001 ¶¶ 10, 34 (citing Ex. 1004, 4, ll. 2-10). The University does not dispute that Lisenker teaches this limitation.

Micron has made a prima facie showing that the subject matter of claims 1, 2, 4-7, 9-16, and 18 would have been obvious over Lisenker.

E. Claims 1, 2, 4-7, 9-16, and 18 As Obvious Over Lisenker and Gise

For this ground, Micron additionally relies on Gise as allegedly teaching a post-metal annealing (in hydrogen) for about an hour. Gise does teach this. Ex. 1010, 130-31. Further, we credit the testimony of Dr. Reed that "it would have been apparent to perform Lisenker's annealing process after the metallization steps have been performed" in light of Gise's teaching. Ex. 1001 ¶ 36.

In opposing prima facie obviousness on this ground, the University merely relies on its prior and unpersuasive arguments regarding Lisenker. PO Resp. 17. Micron has made a prima facie showing that the subject matter of claims 1, 2, 4-7, 9-16, and 18 would have been obvious over Lisenker and Gise.

F. Claim 3 As Obvious Over Lisenker, Gise, and Nicollian

Claim 3 is dependent on claim 1 and additionally requires that the semiconductor device "is encapsulated." Nicollian discloses "the use of coatings and encapsulants" to isolate a semiconductor device from its

environment to promote stable operation of it. Ex. 1012, 1121. We credit the testimony of Dr. Reed that encapsulation "has long been incorporated into integrated circuit manufacturing" and that "[a]t the time of the priority date of the '204 patent, it would have been apparent to include an encapsulation step as taught by Nicollian in the device of Lisenker in order to prevent physical damage and corrosion to the semiconductor device." Ex. 1001 ¶¶ 45-46.

In opposing prima facie obviousness on this ground, the University concedes Nicollian teaches the additional limitation recited in claim 3. PO Resp. 17. It opposes this ground only on its prior and unpersuasive arguments regarding Lisenker. *Id*. Micron has made a prima facie showing that the subject matter of claim 3 would have been obvious over Lisenker, Gise, and Nicollian.

G. Claims 6-18 As Obvious Over Lisenker, Gise, and Ito

Micron relies on Ito for teaching two things: (1) a gate insulator having a thickness not exceeding about 55 Angstroms (as required by all of claims 6-18); and (2) a gate insulator comprising silicon oxynitride (as required by claims 8 and 17).

We already have determined above that the subject matter of claims 6, 7, 9-16, and 18 would have been obvious over Lisenker alone as well as over Lisenker in view of Gise. In doing so, however, we did not find an express teaching within Lisenker or Gise of the thickness limitation of about 55 Angstroms or less. Ito provides such an express teaching. *See* Ex. 1008, col. 9, ll. 41-43 (teaching gate insulative layers as thin as approximately 30 Angstroms). Ito also teaches gate insulative layers that comprise silicon oxynitride, as required by claims 8 and 17. *Id*. at col. 8, ll. 38-42.

We credit the testimony of Dr. Reed that, at the time of the priority date of the '204 patent, it would have been apparent to substitute Ito's thin insulating layer comprising oxynitride for the silicon dioxide layer disclosed by Lisenker because miniaturization of semiconductor elements was a common endeavor among those in the semiconductor industry and because silicon oxynitride was known to improve the resilience of MOSFETs to hot carrier effects. Ex. 1001 ¶ 44.

In opposing prima facie obviousness on this ground, the University merely relies on its prior and unpersuasive arguments regarding Lisenker. PO Resp. 17-18. Micron has made a prima facie showing that the subject matter of claims 6-18 would have been obvious over Lisenker, Gise, and Ito.

H. Claim 10 As Obvious Over Lisenker, Gise, Ito, and Mikawa

Claim 10 recites a passivation "atmosphere comprising about 10% deuterium and about 90% nitrogen." As noted in the Decision to Institute, Mikawa discloses passivation atmospheres of both "10% $H_2$/90% $N_2$" and "10% $D_2$/90% $N_2$." Dec. 9. In its petition, and perhaps unintentionally, Micron relies on Mikawa for teaching a passivation atmosphere comprising "about 10% *hydrogen* and about 90% nitrogen." Pet. 59 (emphasis added). The University argues that the Decision to Institute "cites to ***no*** evidence that one of skill in the art would have been motivated to substitute the hydrogen taught in Mikawa with the deuterium specified in claim 10." PO Resp. 18. That is not true. Lisenker provides such evidence, and it was pointed out in the Decision. *See, e.g.*, Dec. 6 (quoting Ex. 1004, 4, ll. 32-34 ("In general, any hydrogen containing material used in VLSI fabrication can be replaced with corresponding deuterium containing material.")).

Micron has made a prima facie showing that the subject matter of claim 10 would have been obvious over Lisenker, Gise, Ito, and Mikawa.

I. Claims 1-5 As Obvious Over Deal and Lisenker

Micron asserts that Deal teaches the subject matter of these claims except for the retention of deuterium at the interface. Pet. 28-29. We agree and note that the University does not dispute the asserted teachings of Deal. PO Resp. 18-19.

Micron next asserts that it would have been obvious for a person of ordinary skill in the art at the time of the invention of the '204 patent to modify Deal to employ deuterium instead of hydrogen as taught by Lisenker to increase the resiliency of the field effect transistor to hot electron effects. Pet. 28-29. Dr. Reed testified:

> At the time of the priority date of the '204 patent, the benefits of substituting deuterium for hydrogen were known. As I have discussed previously, Lisenker teaches the substitution of deuterium for hydrogen and states that such a substitution results in "bonds that are less likely to break when exposed to electrical stresses," which improves device "stability, quality, and reliability." It would have been apparent to incorporate the teachings of Lisenker with the '380 patent [i.e., Deal] because both references are directed to improving the quality of the $Si/SiO_2$ interface, which has a direct impact on the device quality. Lisenker suggests that "any hydrogen containing material used in VLSI fabrication can be replaced with corresponding deuterium containing material," which would include the '380 patent's post-metallization anneal.

Ex. 1001 ¶ 49 (footnotes omitted).

In opposing prima facie obviousness on this ground, the University merely relies on its prior arguments regarding Lisenker. PO Resp. 18-19. However, the argument that Lisenker is limited to pre-metal annealing and,

thus, results in no increase in deuterium at the interface is misplaced here (in addition to being erroneous). It is Deal, and not Lisenker, that is relied on for its teaching of post-metal annealing. That teaching is undisputed. And, as Dr. Reed testified, Lisenker suggests to the person of ordinary skill in the art to modify Deal's post-metal anneal by substituting deuterium for hydrogen.

Micron has made a prima facie showing that the subject matter of claims 1-5 would have been obvious over Deal in view of Lisenker.

J. Claims 6-18 As Obvious Over Deal, Lisenker, and Ito

Here, Micron again relies on Ito for teaching a gate insulator having a thickness not exceeding about 55 Angstroms (as required by claims 6-18), which gate insulator comprises silicon oxynitride (as required by claims 8 and 17).

As set forth above, we credit the testimony of Dr. Reed that, at the time of the priority date of the '204 patent, it would have been apparent to substitute Ito's thin insulating layer comprising oxynitride for the silicon dioxide layer disclosed by Lisenker because miniaturization of semiconductor elements was a common endeavor among those in the semiconductor industry and/or silicon oxynitride was known to improve the resilience of MOSFETs to hot carrier effects. Ex. 1001 ¶ 44.

In opposing prima facie obviousness on this ground, the University again relies exclusively on its prior arguments regarding Lisenker. PO Resp. 19. But, it is Deal, and not Lisenker, that is relied on for its teaching of post-metal annealing. That teaching is undisputed. And, as Dr. Reed testified, Lisenker suggests to the person of ordinary skill in the art to modify Deal's post-metal anneal by substituting deuterium for hydrogen.

Micron has made a prima facie showing that the subject matter of claims 6-18 would have been obvious over Deal, Lisenker, and Ito.

K. Objective Indicia

The University argues that certain objective indicia, or secondary considerations, demonstrate non-obviousness of the claims. *See Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966) ("Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy."). In particular, the University argues that the claimed invention of the '204 patent yielded unexpected results and that others failed to eliminate hot carrier effects. PO Resp. 4-8.

The University's evidence of unexpected results is not persuasive because it does not compare the results of the claimed invention of the '204 patent to the closest prior art, which is Lisenker. *See* PO Resp. 4-7; *In re Baxter Travenol Labs.*, 952 F.2d 388, 392 (Fed. Cir. 1991) ("[W]hen unexpected results are used as evidence of nonobviousness, the results must be shown to be unexpected compared with the closest prior art."). Lisenker expressly discloses that "deuterium containing devices of the present invention have improved stability, quality, and reliability" relative to those containing hydrogen. Ex. 1004, 5, ll. 4-5. Thus, when properly considering Lisenker, the beneficial results of substituting deuterium for hydrogen are expected. *See In re Skoner*, 517 F.2d 947, 950 (CCPA 1975) ("Expected beneficial results are evidence of obviousness of a claimed invention. Just as unexpected beneficial results are evidence of unobviousness.").

With respect to the alleged failure of others, the University argues that the "continued use [in the prior art] of hydrogen passivation reflects a systemic failure in the art to solve the problem faced by the inventors of the '204 patent." PO Resp. 8. Thus, the University again fails to account for the prior art teachings of Lisenker, which already had proposed the substitution of deuterium for hydrogen during passivation, and indeed, throughout the VLSI fabrication process.

Having considered all of the evidence, including Patent Owner's secondary considerations evidence, we conclude that the claims would have been obvious.

## CONCLUSION

Petitioner, Micron, has demonstrated by a preponderance of the evidence that claims 1-18 of the '204 patent are unpatentable as follows:

claims 1, 2, 4, and 5 are anticipated by Lisenker;

claims 1, 2, 4-7, 9-16, and 18 would have been obvious over Lisenker;

claims 1, 2, 4-7, 9-16, and 18 would have been obvious over Lisenker and Gise;

claim 3 would have been obvious over Lisenker, Gise, and Nicollian;

claims 6-18 would have been obvious over Lisenker, Gise, and Ito;

claim 10 would have been obvious over Lisenker, Gise, Ito, and Mikawa.

claims 1-5 would have been obvious over Deal and Lisenker; and

claims 6-18 would have been obvious over Deal, Lisenker, and Ito.

ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1-18 of the ’204 patent are CANCELLED.

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