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Paper 31
Entered: August 6, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HEWLETT-PACKARD COMPANY,
Petitioner,

v.

MCM PORTFOLIO, LLC,
Patent Owner.

Case IPR2013-00217
Patent 7,162,549

Before JONI Y. CHANG, GLENN J. PERRY, and JENNIFER S. BISK, *Administrative Patent Judges.*

BISK, *Administrative Patent Judge*.

FINAL WRITTEN DECISION

35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Petitioner Hewlett-Packard Company ("HP") filed a Petition (Paper 2, "Pet.") to institute an *inter partes* review of claims 7, 11, 19, and 21 (the "challenged claims") of U.S. Patent No. 7,162,549 (Exhibit 1001, "the '549 patent") under 35 U.S.C. §§ 311-319. Patent Owner MCM Portfolio, LLC ("MCM") filed a Preliminary Response. Paper 9. On September 10, 2013, we instituted trial (Paper 10; "Decision"), concluding that Petitioner had demonstrated a reasonable likelihood of showing that the challenged claims are unpatentable under 35 U.S.C. § 103 over U.S. Patent No. 6,199,122 (Ex. 1005) ("Kobayashi") combined with WO 98/03915 (Ex. 1007) ("Kikuchi"). Decision 3, 16.

We have jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

Petitioner has shown by a preponderance of evidence that claims 7, 11, 19, and 21 are *unpatentable*.

B. Related Proceedings

The parties list several cases pending in the Eastern District of Texas that would affect or be affected by the decision in this proceeding, including *Technology Properties Limited, LLC v. Hewlett-Packard Co.*, No. 6:12-cv-208 (E.D. Tex. Mar. 28, 2012), in which the '549 patent is asserted against Petitioner. *See* Pet. 1; Paper 6, 1. On February 11, 2014, after a finding of No Violation of Section 337 in a concurrent proceeding at the International Trade Commission (No. 337-TA-841), a stay of the 6:12-cv-208 case was lifted and it was consolidated with *Technology Properties Limited, LLC v. Cannon, Inc. et al.*, No. 6:12-cv-202 (E.D. Tex. Mar. 28, 2012). A

Markman Hearing is currently scheduled in that case for October 8, 2014. *Technology Properties Limited, LLC v. Cannon, Inc. et al.*, No. 6:12-cv-202 (E.D. Tex. Mar. 14, 2014).

In addition, the '549 patent is the subject of a pending reissue proceeding, US Application 12/351,691. We ordered a stay of that examination pending the termination or completion of this proceeding. Paper 8.

C. The '549 Patent

The '549 patent relates to controllers for flash-memory cards. Ex. 1001, 1:21-22. As described in the "Background of the Invention," at the time of the invention, removable flash-memory cards were commonly used with digital cameras to allow for convenient transfer of images from a camera to a personal computer. *Id.* at 1:26-56. These prior art flash-memory cards were available in several formats, including CompactFlash, SmartMedia, MultiMediaCard (MMC), Secure Digital Card (SD), and Memory Stick card. *Id.* at 2:28-55. Each of the card formats required a different interface adapter to work with a personal computer. *Id.* at 3:9-25.

The Specification describes a need for a flash-memory card reader that accepts flash-memory cards of several different formats using a universal adapter. *Id.* at 3:52-63. In response to this need, the '549 patent describes various improvements to flash-memory card readers, including by determining whether a particular flash-memory card includes a controller and, if not, performing operations to manage error correction for the flash-memory card. *Id.* at 3:24-65.

D. Illustrative Claim

Claim 7, reproduced below, is illustrative of the claimed subject matter:

> 7. A method comprising:
>
> using a controller chip to interface a flash storage system with or without a controller to a computing device, the controller chip comprising a flash adapter, wherein the flash storage system comprises a flash section and at least a medium ID;
>
> determining whether the flash storage system includes a controller for error correction; and
>
> in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

II. ANALYSIS

A. Seventh Amendment

As a preliminary matter, MCM argues that *inter partes* review proceedings violate the Seventh Amendment. PO Resp. 2-13. The U.S. Court of Appeals for the Federal Circuit, however, has previously rejected this argument in the context of reexaminations. *Patlex Corp. v. Mossinghoff*, 758 F.2d 594, 603-05 (Fed. Cir. 1985) (holding that even when applied retroactively, the reexamination statute does not violate the jury trial guarantee of the Seventh Amendment); *see also Joy Techs., Inc. v. Manbeck*, 959 F.2d 226, 228-29 (Fed. Cir. 1992) (affirming the holding in *Patlex*), *other grounds superseded by statute*, 35 U.S.C. § 145, *as recognized in In re Teles AG Informationstechnologien*, 747 F.3d 1357 (Fed. Cir. 2014). *Inter partes* review proceedings continue the basic functions of the reexamination proceedings at issue in *Patlex*—authorizing the Office to reexamine the

validity of an issued patent and to cancel any claims the Office concludes should not have been issued. Patent Owner does not identify any constitutionally-significant distinction between reexamination proceedings and *inter partes* review proceedings. Thus, for the reasons articulated in *Patlex*, we conclude that *inter partes* reviews, like reexaminations, comply with the Seventh Amendment.

B. Claim Construction

We construe all terms, whether or not expressly discussed here, using the broadest reasonable construction in light of the '549 patent specification. 37 C.F.R. § 42.100(b). For the purposes of the decision to institute we expressly construed the following terms: (1) "flash adapter" and "flash adapter section" as "a section of the controller chip that enables communication with the flash storage system" and (2) "bad block mapping" as a type of error correction. Decision 5-6. In the post-institution briefs, the parties do not dispute these constructions. *See* Paper 23 ("PO Resp."); Paper 24 ("Reply"). For purposes of this decision, we continue to apply these constructions.

C. Overview of Kobayashi

Kobayashi describes a memory device for a computer with a converter that converts serial commands of the computer to parallel commands that are then used to control a storage medium (which can be a flash-memory card). Ex. 1005, 2:55-64, 3:63-65. This configuration is shown in Figure 1, which is reproduced below.

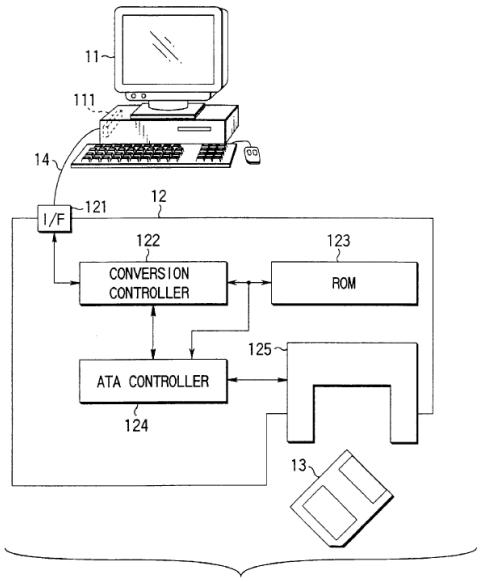


FIG. 1

Figure 1 is a block diagram of computer 11 with reader/writer 12 and flash-memory card 13. *Id.* at 5:54-58. The reader/writer includes conversion controller 122, ATA controller 124, and a connector 125 for reading a flash-memory card 13. *Id.* at 6:5-9.

One of the several embodiments described by Kobayashi is shown in Figure 11, reproduced below.

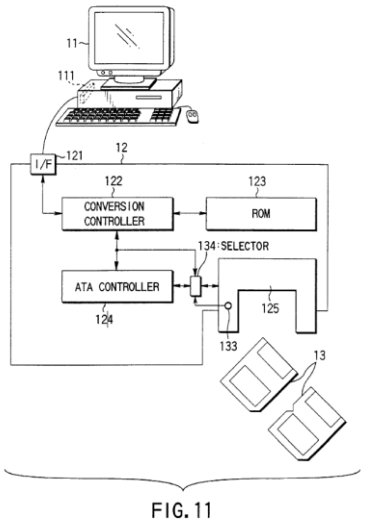


FIG. 11

Figure 11 depicts an embodiment described by Kobayashi. In the embodiment depicted in Figure 11, flash-memory cards 13 both with and without controllers may be used. *Id.* at 12:59-65. Sensor 133 determines the type of flash-memory card 13 mounted on connector 125. *Id.* at 12:59-13: 2. When a flash-memory card with no controller is detected, selector 134 connects ATA controller 124 and connector 125. *Id.* at 13:2-5. When a flash-memory card with a controller is detected, selector 134 connects conversion controller 122 and connector 125.

D. Overview of Kikuchi

Kikuchi describes a flash-memory card and controller 10 having an interface connected to host computer 14. Ex. 1007, Abstract. Figure 1 of Kikuchi is reproduced below.

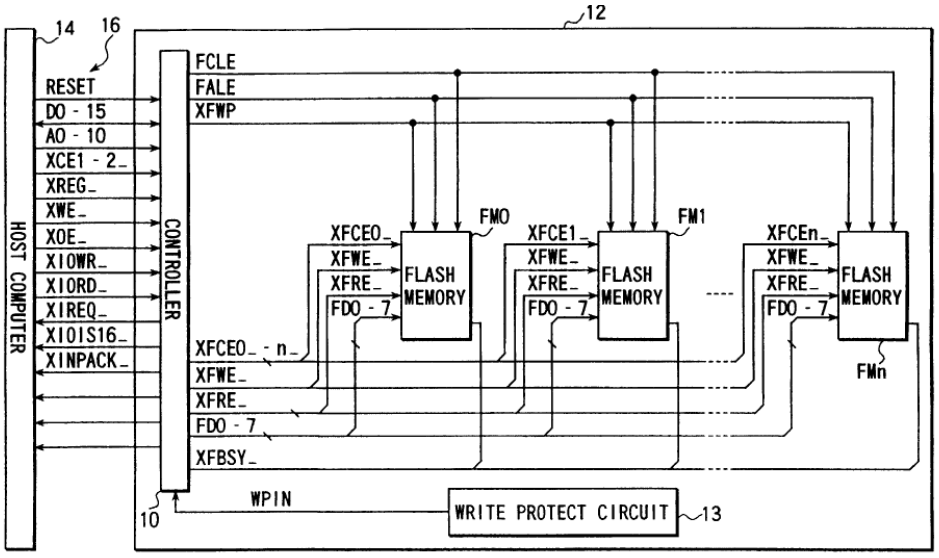
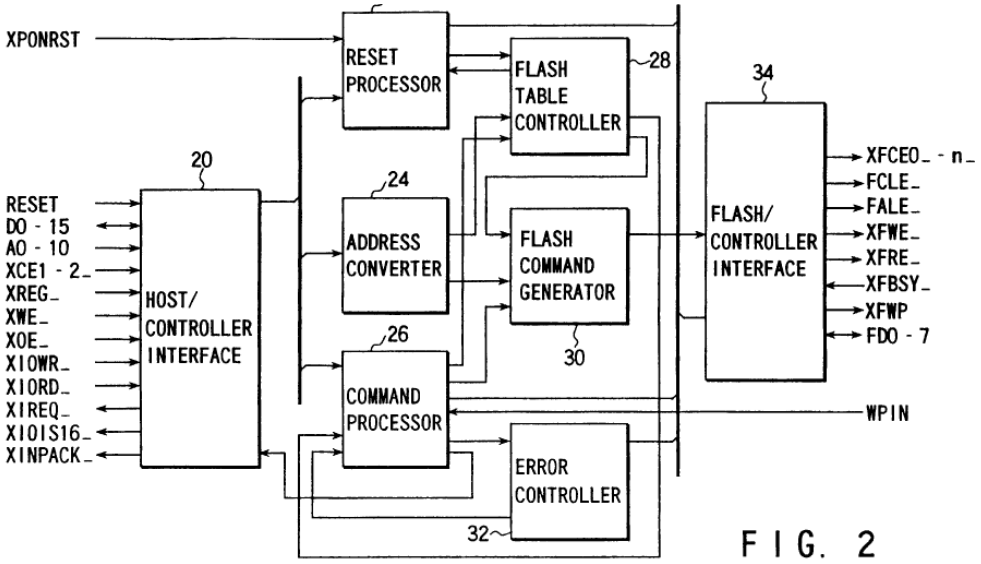


FIG. 1

Figure 1 shows the flash memory card with "one-chip controller" 10 on the flash-memory card. *Id.* at 9:10-15[1]. Figure 2 of Kikuchi is reproduced below.



F I G. 2

Figure 2 is a block diagram showing the functional arrangement of controller 10, including error controller 32, that performs error control for read and write operations. *Id.* at 11:14-20; 13:17-19. Error controller 32 also "performs a block substituting process or the like in the event of a failure or error." *Id.* at 13:17-21. In a separate embodiment, controller 10 "refers to the block quality flag contained in the block status information of the redundant portion of the readout information . . . to check whether the head block BL0 is non-defective or not" and "detects a non-defective block BLj having the highest address rank." *Id.* at 20:20-21:5.

E. Obviousness over Kobayashi and Kikuchi

HP asserts that a person of ordinary skill in the art would have found the challenged claims obvious over the combination of Kobayashi and

[1] In this opinion, page numbers for this exhibit refer to the number at the right hand bottom of the page, not the number in the top middle of the page.

Kikuchi. Pet. 42-57 (citing Ex. 1008 (Declaration of Dr. Sanjay Banerjee) ¶¶ 102-122). In particular, HP asserts that Kobayashi discloses every limitation of the challenged claims except the details of error correction. *Id.* at 47-48. HP relies on Kikuchi as describing the recited error correction. *Id.* at 48-49. In addition, HP asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the two references, which both describe ATA controllers that work with flash-memory cards with, or without, on-card controllers, in order to "reliably retain stored data." Pet. 50 (citing Ex. 1008 ¶ 121 (quoting Ex. 1007 (Kikuchi), 4:1-3)).

We are persuaded that a preponderance of the evidence demonstrates that the combination of Kobayashi and Kikuchi discloses each of the limitations of the challenged claims, as presented in HP's Petition. *See* Pet. 42-57; Ex. 1008 ¶¶ 102-122. We are also persuaded that a preponderance of the evidence demonstrates that a person of ordinary skill in the art would have combined the Kobayashi and Kikuchi references. *See* Pet. 50; Ex. 1008 ¶ 121.

MCM explicitly addresses only the requirement of "a controller chip," arguing that Kobayashi does not disclose using a single chip with the claimed functionality, but instead has "multiple chips that perform distinct functions." PO Resp. 14. Specifically, MCM argues that Kobayashi discloses two controllers as separate chips: 122 that exclusively interfaces with cards having controllers, and 124 that exclusively interfaces with cards that do not have controllers. PO Resp. 22. Based on this assertion, MCM argues (1) that the Petition should be dismissed because HP did not point out the single chip requirement explicitly in the Petition (*id.* at 14-21), and

(2) that the combination of Kobayashi and Kikuchi would not yield the claimed invention, which requires a single chip (*id.* at 21-24). We do not find either argument persuasive.

First, we are persuaded that HP sufficiently discussed the single-chip limitation in its Petition. The Petition explicitly points to Kikuchi's disclosure of "controller 10 as a single chip controller." Pet. 49 (citing Ex. 1007, 7:10-22, 9:11-19); *see also* Pet. 48, 53, 55; Ex. 1008 ¶¶ 114-117. Moreover, Petitioner also asserts that "Kobayashi's controller 122 is a 'one-chip microprocessor.'" Pet. 44 (quoting Ex. 1006, 5:66-6:4, 6:12-22); *see also* Pet. 53, 55. These statements, combined with HP's assertion that combining the teachings of the two references is merely "a combination of prior art elements according to known methods to yield predictable results" (Pet. 50-51), were sufficient for us to determine that Petitioner had a reasonable likelihood of showing unpatentability of the challenged claims. Decision 14-16. We are not persuaded otherwise by Patent Owner's post-institution arguments.

Second, this evidence supports a determination that one of ordinary skill in the art would have had both the knowledge and the inclination to place the functionality taught by Kobayashi and Kikuchi on a single chip. *See* Ex. 1007, 7:12-15 ("This flash memory card has a one-chip controller. . . ."); Ex. 1008 ¶¶ 122-23. In fact, MCM conceded at the oral hearing that it was not beyond the skill of one of ordinary skill at the time of the invention to put multiple functions into a single chip and that, in fact, it is common practice to do so.

> JUDGE PERRY: Counsel, are you saying that it is beyond the skill of one of ordinary skill at the time of this invention to put multiple functions integrated into a single chip?

> MR. HELLER: Not at all.
>
> JUDGE PERRY: You are not saying that?
>
> MR. HELLER: Not at all when you have a motivation to do so.
>
> JUDGE PERRY: Isn't it kind of a common practice for those who design integrated circuits to put multiple functions into those circuits?
>
> MR. HELLER: It probably is common practice, but they have to have a motivation to do so.
>
> JUDGE BISK: Is there some reason not to put them on a single chip? It seems like it is just a design choice, whether it is one chip, two chips, 10 chips. Is there a particular reason why the number of chips matters?
>
> MR. HELLER: It is not that. It is, why would you do that? Why would you put all that functionality into a single chip?

Paper 30 ("Tr."), 30:17-31:4.

MCM's assertion—that even if Kikuchi's error correction is incorporated into Kobayashi's ATA controller 124 the result would not yield the claimed invention—misses the point. PO Resp. 20. The relevant inquiry is whether the claimed subject matter would have been obvious to those of ordinary skill in the art in light of the combined teachings of the references. *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981). "Combining the *teachings* of references does not involve an ability to combine their specific structures." *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973). Patent Owner does not argue that applying the teachings of Kikuchi and Kobayashi so that the claimed functionality is on a single chip would have been "uniquely challenging or difficult for one of ordinary skill in the art" at the time of the invention. *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)).

We conclude that a preponderance of the evidence demonstrates that claims 7, 11, 19, and 21 are unpatentable based on the combination of Kobayashi and Kikuchi.

III. CONCLUSION

Petitioner has shown, by a preponderance of the evidence, that the challenged claims would have been obvious over the combination of Kobayashi and Kikuchi.

Accordingly, it is

ORDERED that claims 7, 11, 19, and 21 of the '549 patent are determined to be *unpatentable*;

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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