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Paper 60
Entered: February 19, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SYNOPSYS, INC.
Petitioner

v.

MENTOR GRAPHICS CORPORATION
Patent Owner

Case IPR2012-00042
Patent 6,240,376 B1

Before HOWARD B. BLANKENSHIP, SALLY C. MEDLEY, and JENNIFER S. BISK, *Administrative Patent Judges*.

BISK, *Administrative Patent Judge*.

FINAL WRITTEN DECISION

35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Petitioner, Synopsys, Inc. ("Synopsys"), filed a petition on September 26, 2012, for *inter partes* review of claims 1-15 and 20-33 of U.S. Patent No. 6,240,376 B1 ("the '376 Patent") pursuant to 35 U.S.C. §§ 311-319. Paper 1 ("Pet."). Patent Owner, Mentor Graphics Corporation ("Mentor Graphics"), filed a preliminary response on December 28, 2012. Paper 15 ("Prelim. Resp."). On February 22, 2013, the Board denied the petition as to claims 10, 12-15, 20-27, and 30-33, and instituted trial for claims 1-9, 11, 28, and 29, on one ground of unpatentability, anticipation by U.S. Patent No. 6,132,109 ("Gregory") (Ex. 1007). Paper 16 ("Decision to Institute").

After institution of trial, Mentor Graphics filed a patent owner response. Paper 28 ("PO Resp."). Mentor Graphics also filed a substitute motion to amend claims by submitting proposed new claims 34-43 for claims 1, 5, 28, 2, 3, 6, 8, 9, 11, and 29, respectively. Paper 31 ("Mot. to Amend"). Synopsys filed a reply to the patent owner response (Paper 36; "Reply"), and also an opposition to Mentor Graphics's motion to amend (Paper 35; "Opp."). Mentor Graphics then filed a reply in support of its motion to amend. Paper 39 ("Reply Mot. to Amend").

In preparation for oral hearing, both parties filed and fully briefed motions to exclude. Paper 42 ("Mentor Graphics's Motion to Exclude"); Paper 44 ("Synopsys's Motion to Exclude"). Oral hearing was held November 14, 2013. Paper 59 ("Transcript").

The Board has jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

Synopsys has shown that claims 5, 8, and 9 are unpatentable. Synopsys, however, has not met its burden to show by a preponderance of the evidence that claims 1-4, 6, 7, 11, 28, and 29 are unpatentable.

Mentor Graphics's motion to amend claims is *denied.*

B. The '376 Patent

The '376 patent generally relates to the fields of simulation and prototyping of integrated circuits. Ex. 1001, col. 1, ll. 10-11. In particular, the patent describes "debugging synthesizable code at the register transfer level during gate-level simulation." *Id.* at ll. 11-13.

As described in the Background of the Invention, integrated circuit design begins with a description of the behavior desired in a hardware description language ("HDL") such as Very High Speed Integrated Circuit Description Language ("VHDL"). *Id.* at ll. 14-25. A subset of HDL source code is referred to as Register Transfer Level ("RTL") source code. *Id.* at ll. 28-30. This RTL source code can be simulated using software, which typically offers robust debugging functionality for analyzing and verifying the design, including navigating the design hierarchy, viewing the RTL source code, setting breakpoints on a statement of RTL source code to stop the simulation, and viewing and tracing variables and signal values. *Id.* at ll. 44-54. However, although flexible, software RTL simulators are slow compared with hardware emulation. *Id.* at ll. 55-63. Thus, it often is desirable to use gate-level simulation to verify complex designs. *Id.*

The RTL description of a circuit can be used by synthesis tools to generate a "gate-level netlist," which, in turn, can be converted to a format suitable for programming a hardware emulator. *Id.* at ll. 35-42. A gate-level netlist represents the circuit to be simulated and ultimately is comprised of

combinatorial or sequential logic gates (e.g. AND, NAND, and NOR gates, or flip-flops and latches) and a description of their interconnections using signals (signals are also referred to as nets). *Id.* at col. 4, ll. 5-17. As discussed, gate-level simulation is useful for validation of a circuit design. *Id.* at col. 1, ll. 55-67. However, one disadvantage of gate-level simulation is that much of the high-level information from the RTL source code is lost during synthesis, resulting in debugging functionality that is limited severely in comparison with that available in software RTL simulation. *Id.* at col. 2, ll. 1-23.

The ’376 patent describes a method of synthesizing RTL source code such that the resulting gate-level simulation can support the traditional debugging tools of setting breakpoints, mapping signal values to particular source code lines, and stepping through the source code to trace variable values. *Id.* at ll. 1-30. The Summary of the Invention describes facilitating debugging during gate-level simulation by: (1) generating “instrumentation logic indicative of the execution status of at least one synthesizable statement within the RTL source code”; (2) generating a gate-level netlist from the RTL source code; and (3) during simulation, evaluating the instrumentation logic of the gate-level netlist to enable RTL debugging. *Id.* at ll. 26-39.

The ’376 patent describes two main embodiments for implementing this method. The first embodiment modifies the gate-level netlist to provide instrumentation signals “implementing the instrumentation logic and corresponding to synthesizable statements within the RTL source code.” *Id.* at ll. 40-43. This modification of the gate-level netlist can be done either by modifying the RTL source code directly or by generating the modified gate-

level netlist during synthesis. *Id.* at ll. 43-46. The second embodiment ("the cross-reference embodiment") describes storing the instrumentation signals in a cross-reference database instead of modifying the gate-level netlist. *Id.* at ll. 47-52.

Figure 2 of the '376 patent, reproduced below, illustrates "one embodiment of the instrumentation process in which instrumentation is integrated with the synthesis process." *Id.* at col. 5, ll. 9-11.

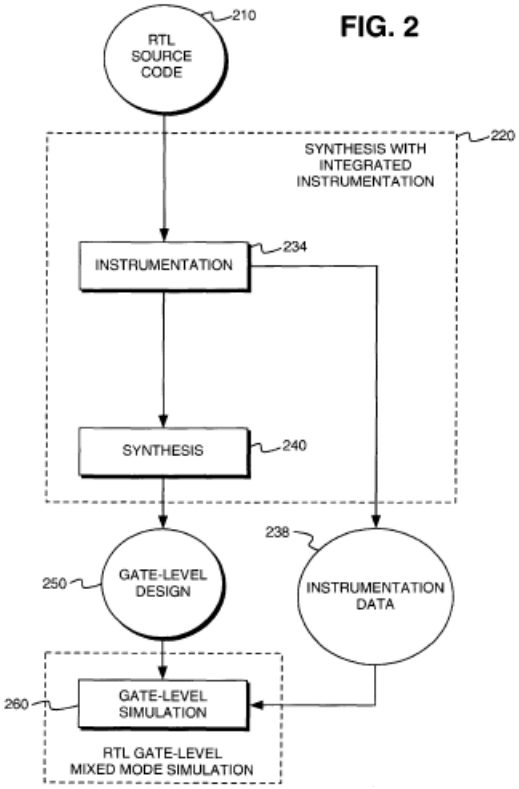


Figure 2, above, shows that RTL source code 210 is provided to synthesis process 220, which includes instrumentation step 234 followed by synthesis step 240. *Id.* at ll. 11-16. In the first embodiment, in which the gate level netlist is modified to include instrumentation signals, the resulting gate-level design 250 "contains additional logic to create the additional instrumentation output signals referenced in instrumentation data 238." *Id.* at ll. 17-30.

Instrumentation data 238 is implemented as gates that can then be simulated. *Id.* at col. 6, ll. 32-37.

In the cross-reference embodiment, "the RTL source code is analyzed to generate a cross-reference database as instrumentation data 238 without modifying the gate-level design." *Id.* at col. 5, ll. 31-33. In this embodiment, "[t]he instrumentation data 238 is likely to contain considerably more complex logic to evaluate during simulation." *Id.* at ll. 42-45.

The '376 patent describes tradeoffs between the two main embodiments. *Id.* at l. 45. For example, the first embodiment reduces the complexity of the logic to be evaluated during simulation, resulting in faster simulation time. *Id.* at ll. 46-64. However, because the gate-level design used during simulation is modified to accommodate the debugging logic, the design actually used for production will differ from that used during simulation, and, thus, the simulation may not reproduce accurately the production behavior of the circuit. *Id.* On the other hand, the cross-reference embodiment typically results in greater complexity of instrumentation logic to evaluate during simulation, resulting in longer simulation time. *Id.* at ll. 65-67. In addition, some of the evaluation may be performed by software, instead of hardware, eliminating direct verification of the target system through in-situ verification. *Id.* at col. 5, l. 65 – col. 6, l. 11. However, the technique does not affect the original gate-level design, and the instrumentation data can be eliminated after testing without disrupting the gate-level design. *Id.* Because of these various tradeoffs, the '376 patent mentions generally, but does not describe in detail, alternate

embodiments that combine the two main embodiments "in order to trade off simulation speed, density, and verification accuracy." *Id.* at col. 6, ll. 17-22.

The '376 patent subsequently describes (in Figures 3, 12, and 17 and the related text) three methods of modifying the gate-level netlist. *Id.* at col. 13, ll. 38-40. As described when discussing the first embodiment above, the '376 patent discloses that these three methods can be applied either by modifying the RTL source code directly by applying the method to the source code before it is synthesized independently of the synthesis process (*id.* at ll. 55-59), as shown in Figures 3, 12, and 17, or they can be integrated into the synthesis tool so that actual modification of the RTL source code is not required (*id.* at ll. 60-67).

Figure 3, reproduced below, illustrates a method of modifying RTL source code for sequential statements that depend only on the value of the inputs and can be synthesized to logic networks of combinatorial gates and latches ("level-sensitive RTL source code"). *Id.* at col. 7, ll. 13-22, 40-43.

FIG. 3

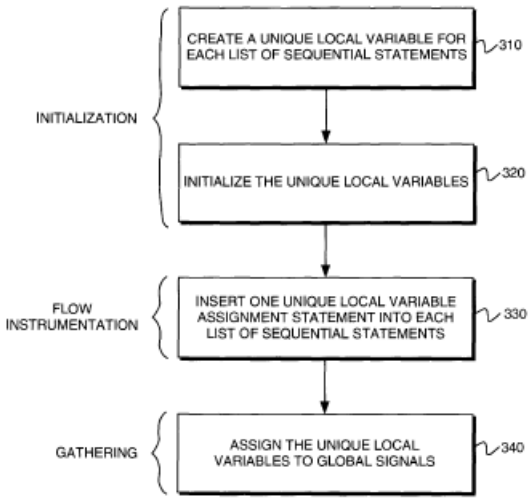
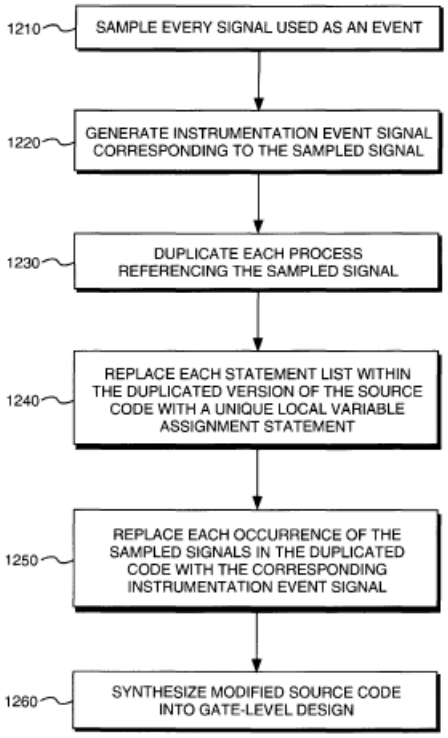


Figure 3, above, shows a method in which a unique local variable is created for each list of adjacent sequential statements in step 310, each of

these variables is initialized to zero in step 320, and one unique variable assignment statement is inserted into each list of adjacent sequential statements corresponding to an executable branch in step 330. *Id.* at ll. 40-50. At the end of the process, all the unique local variables are assigned to global signals in step 340. *Id.* at ll. 50-54.

Figure 12, reproduced below, illustrates a method of modifying RTL source code having references to signal events, typically used to describe edge-sensitive devices such as flip-flops. *Id.* at col. 9, ll. 27-32, 63-64.

FIG. 12



The method shown in Figure 12, above, begins with step 1210, in which every signal whose state transition serves as the basis for the determination of another signal is sampled. *Id.* at ll. 63-67. An instrumentation signal event is generated in step 1220, and every process that references a signal event is duplicated in step 1230. *Id.* at col. 9, l. 67 –

col. 10, l. 7. In step 1240 each list of sequential statements within the duplicate version of the code is replaced by a unique local variable assignment. In step 1250, each time a signal event is referenced in the duplicated version of the code, it is replaced by the sampled signal event computed in step 1210. *Id.* at col. 10, ll. 7-12. Finally, the RTL source code is synthesized, in step 1260, to generate gate-level logic, including the instrumentation signals. *Id.* at ll. 12-14.

Figure 17, reproduced below, illustrates a method of modifying RTL source code for processes themselves for subsequent determination of whether the process is active during gate-level simulation. *Id.* at col. 11, ll. 43-46.

FIG. 17

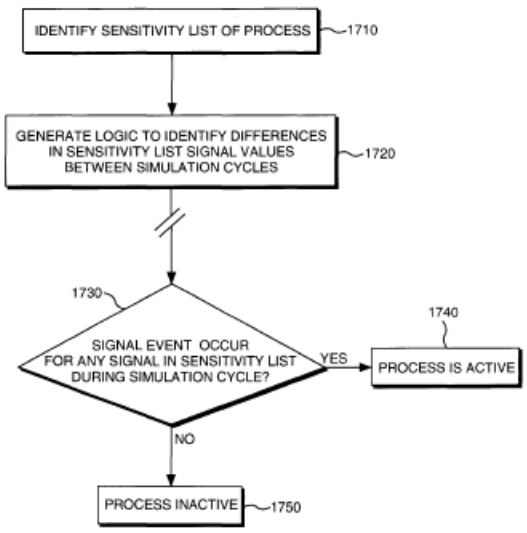


Figure 17, above, shows a method in which the sensitivity list of a process is identified in step 1710, logic is generated to compare the signals in the sensitivity list between consecutive simulation cycles in step 1720, and during gate-level simulation in step 1730, a determination is made as to whether an event has occurred on any of the sensitivity list signals. *Id.* at

ll. 48-53. If the signal indicates a difference during a simulation cycle, as indicated by step 1740, the process is active; otherwise, the process is inactive, as indicated by step 1750. *Id.* at ll. 53-58.

C. Illustrative Claims

Three of the claims involved in this proceeding, claims 1, 5, and 28, are independent. All three are reproduced below:

1. A method comprising the steps of:

a) identifying at least one statement within a register transfer level (RTL) synthesizable source code; and

b) synthesizing the source code into a gate-level netlist including at least one instrumentation signal, wherein the instrumentation signal is indicative of an execution status of the at least one statement.

5. A method of generating a gate level design, comprising the steps of:

a) creating an instrumentation signal associated with at least one synthesizable statement contained in a register transfer level (RTL) synthesizable source code; and

b) synthesizing the source code into a gate-level design having the instrumentation signal.

28. A storage medium having stored therein processor executable instructions for generating a gate-level design from a register transfer level (RTL) synthesizable source code, wherein when executed the instructions enable the processor to synthesize the source code into a gate-level netlist including at least one instrumentation signal, wherein the instrumentation signal is indicative of an execution status of at least one synthesizable statement of the source code.

II. ANALYSIS

A. 35 U.S.C. § 315(b)

As a threshold issue, Mentor Graphics argues that this proceeding is barred by virtue of the relationship between Synopsys and the companies of Synopsys Emulation and Verification, S.A. and EVE-USA, Inc. (collectively "EVE"). PO Resp. 2-22. Mentor Graphics bases these arguments on the following facts.

Luc Burgun, a named inventor of the '376 patent, was, at one time, a Mentor Graphics employee. PO Resp. 3 (citing Ex. 2028: Ex. 5 at 1-4.[1] Burgun assigned all rights in the invention claimed in the '376 patent to Mentor Graphics. *Id.* (citing Ex. 2029: Ex. 2 at 3). Subsequently, Burgun left Mentor Graphics and went to work for EVE. *Id.* In 2006, Mentor Graphics filed suit against EVE in the United States District Court for the District of Oregon, alleging that EVE's ZeBu emulators infringed the '376 patent. *Id.* at 4 (citing Ex. 2001); *Mentor Graphics Corp. v. EVE-USA, Inc.*, 06-341-AA (D. Or. 2006). That case was dismissed with prejudice pursuant to a settlement agreement. Ex. 2003. Shortly after filing the petition in the present case, EVE and Synopsys jointly filed a declaratory judgment action in the United States District Court for the Northern District of California, seeking a ruling of non-infringement and invalidity of the '376 patent. Ex. 2004. The complaint states that "[o]n September 27, 2012, Synopsys, Inc. entered into an agreement to acquire the business of EVE," which acquisition "is expected to close in the immediate future." *Id.* at ¶ 13.

[1] Exhibits 2028 and 2029 are large exhibits, not paginated consecutively, including many non-sequentially numbered Exhibits. Throughout this Decision, citations to these exhibits will be of the form "Ex. 202[8 or 9]: [Ex. # within Ex. 202X at page number of that Ex. #]."

Mentor Graphics contends that the acquisition took place on October 4, 2012. PO Resp. 4-5 (citing Ex. 2029: Ex. 34 at 20).

1. Privity

Mentor Graphics argues that this *inter partes* review is barred because Synopsys and EVE were in privity at the time of the Decision to Institute. *Id.* at 6-7. Mentor Graphics asserts that based on this relationship the complaint served on EVE in the May 2006 case should trigger § 315(b). *Id.* at 6. We disagree with Mentor Graphics's contentions.

35 U.S.C. § 315(b) states as follows:

> An inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent. The time limitation set forth in the preceding sentence shall not apply to a request for joinder under subsection (c).

The Office promulgated a rule interpreting § 315(b), 37 C.F.R. § 42.101(b), which states that:

> A person who is not the owner of a patent may file with the Office a petition to institute an inter partes review of the patent unless:
> . . .
> (b) The petition requesting the proceeding is filed more than one year after the date on which the petitioner, the petitioner's real party-in-interest, or a privy of the petitioner is served with a complaint alleging infringement of the patent.

This rule makes clear that it is only privity relationships up until the time a petition is filed that matter; any later-acquired privies are irrelevant.

Furthermore, privity is a "flexible and equitable" doctrine rooted in common law. Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756,

48,759 (Aug. 14, 2012). Consistent with this doctrine, we also take into consideration the nature of the relationship between the parties at the time that the statutorily-referenced complaint was served. *See, e.g.*, *Taylor v. Sturgell*, 553 U.S. 880, 892 (2008) ("A person who was not a party to a suit generally has not had a 'full and fair opportunity to litigate' the claims and issues settled in that suit."); *Mars Inc. v. Nippon Conlux Kabushiki-Kaisha*, 58 F.3d 616, 619 (Fed. Cir. 1995) (applying res judicata to parent corporation because it controlled wholly-owned subsidiary during prior litigation). Mentor Graphics has not alleged that Synopsys was a privy of EVE in 2006 when EVE was served with a complaint alleging infringement of the '376 patent. Thus, there is no contention that Synopsys had any control of this previous suit or even had notice of it, along with an opportunity to participate while it was still pending. *See Richards v. Jefferson Cnty., Ala.*, 517 U.S. 793 (1996) (holding no estoppel where subsequent plaintiffs were not provided notice of first suit nor adequately represented in it). Thus, this lack of relationship between Synopsys and EVE in the 2006 litigation is another reason to conclude that there was no privity relationship between Synopsys and EVE sufficient to trigger § 315(b)'s prohibitions.

Moreover, no record evidence suggests that Synopsys's petition for review was timed to inject delay into an already-pending litigation and, thus, this case does not implicate the concerns that this statute appears designed to address. H.R. REP. NO. 112-98, at 45 (2011) (explaining § 315(b) as "*Time limits during litigation*. Parties who want to use inter partes review during litigation are required to seek a proceeding within 12 months of being served with a complaint alleging infringement of the patent."); 157 CONG. REC.

S1326 (daily ed. Mar. 7, 2011) (statement of Sen. Sessions) ("The bill also includes many protections that were long sought by inventors and patent owners . . . . It imposes time limits on starting an inter partes or post-grant review *when litigation is pending* . . . . All of these reforms will help to ensure that post-grant review operates fairly and is not used for purposes of harassment or delay." (emphasis added)).

Thus, we conclude that there was no privity relationship between Synopsys and EVE sufficient to trigger § 315(b)'s prohibitions, and we decline to dismiss the *inter partes* review on this basis.

2. Real Party-in-interest

Mentor Graphics argues that this *inter partes* review is barred because EVE is a real party-in-interest to this *inter partes* review. PO Resp. 7-14. Mentor Graphics asserts that, therefore, the complaint served on EVE in the May 2006 case should trigger § 315(b). *Id*. at 6. Mentor Graphics admits that "on the date the petition for this [*inter partes* review] was filed, Synopsys had not yet acquired EVE and therefore had at best merely a prospective interest in the ZeBu products." *Id.* at 9. Mentor Graphics, however, asserts that because Synopsys had a prospective interest in invalidating the '376 patent when the petition was filed, "Synopsys was acting as an agent for the benefit of EVE." *Id.* at 10. Thus, according to Mentor Graphics, at the time of filing, Synopsys was a third-party beneficiary for whose benefit the action was brought and, therefore, a real party-in-interest. *Id.* at 7-10.

Mentor Graphics also contends that Synopsys allowed EVE to direct or control content of the petition for this *inter partes* review because Synopsys (1) specifically acquired EVE because of its expertise in the

technology field to which the '376 patent is directed; (2) jointly asserted with EVE the same non-infringement and invalidity claims and defenses with respect to the '376 patent, using the same counsel, in the jointly-filed declaratory judgment litigation; and (3) planned and coordinated the timing of the filing of the petition in this case and the declaratory judgment complaint with EVE. PO Resp. 12-13. Based on these contentions, Mentor Graphics asserts that Synopsys and EVE "conspired together to conceal EVE's status as a 'real party-in-interest' to circumvent and thwart the statutory estoppel provisions." *Id.* at 14.

As discussed above, 37 C.F.R. § 42.101(b) makes clear that it is only relationships up until the time a petition is filed that matter. Mentor Graphics does not point to persuasive evidence to support its assertions that Synopsys allowed EVE to direct or control content of the petition filed in this case or any other evidence that EVE was a real party-in-interest prior to the filing of the petition. Although Mentor Graphics filed a Motion for Additional Discovery on the topic of real party-in-interest (Paper 21), this motion was denied because it did not articulate clearly why such discovery was "necessary in the interest of justice" as required by 35 U.S.C. § 316(a)(5) (Paper 24). In fact, the entirety of Mentor Graphics's explanation of why it needed additional discovery on the subject of real party-in-interest was the following:

> Thus, while the request interest of justice, [sic] as required by 37 C.F.R. § 42.51(b)(2), in order to allow the Patent Owner an opportunity to show the applicability of a § 315(b) bar under the legal standard adopted by the Board. This includes the opportunity to show further (1) . . . (4) the status of EVE as a real party-in-interest to this IPR.

Paper 21 at 2-3.

Thus, because Mentor Graphics has not supported sufficiently its assertions that EVE was a real party-in-interest at the time the petition in this case was filed, we decline to dismiss the *inter partes* review on this basis.

B. Assignor Estoppel

Mentor Graphics argues that Synopsys is barred from challenging the validity of the '376 patent by assignor estoppel. PO Resp. 14-22. The Board has determined previously, and we agree, that assignor estoppel is not a basis for denying a petition requesting *inter partes* review:

> Under the AIA, "a person *who is not the owner of a patent* may file with the Office a petition to institute an inter partes review of the patent." 35 U.S.C. § 311(a) (emphasis added). Consequently, under the statute, an assignor of a patent, who is no longer an owner of the patent at the time of filing, may file a petition requesting *inter partes* review. This statute presents a clear expression of Congress's broad grant of the ability to challenge the patentability of patents through *inter partes* review.

Athena Automation Ltd. v. Husky Injection Molding Sys. Ltd., IPR2013-00290, slip op. at 12-13 (PTAB Oct. 25, 2013), Paper No. 18; *see also Palo Alto Networks, Inc. v. Juniper Networks, Inc.*, IPR2013-00369, slip op. at 11-14 (PTAB Dec. 19, 2013), Paper No. 16.

Mentor Graphics further asserts that even if Synopsys is not barred from requesting *inter partes* review, the Board should exercise its discretion to dismiss this *inter partes* review because of the relationship between Mr. Burgun and Synopsys.[2] PO Resp. 16-19. Mentor Graphics further argues,

[2] This case does not require us to reach the issue of whether Mr. Burgun is in privity with Synopsys, as asserted by Mentor Graphics (PO Resp. 16-19), because we conclude that even if Mentor Graphics established such a relationship, Mentor Graphics has not shown a sufficient basis to bar

more generally, that equitable considerations weigh against granting the petition, including that Synopsys is in privity with EVE and shares personnel with EVE, including Mr. Burgun. *Id.* at 19. Moreover, according to Mentor Graphics, "[i]t would be wholly against the principles of assignor estoppel to allow Synopsys to receive the benefit of the acquisition of EVE, but avoid EVE's equitable obligations." *Id.* at 22.

We are not persuaded, however, that the equitable doctrine of assignor estoppel provides an exception to the statutory mandate that any person who is not the owner of a patent may file a petition for *inter partes* review. Accordingly, we decline to dismiss the *inter partes* review based on Mentor Graphics's estoppel arguments.

C. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). Claim terms are also given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). The construction that stays true to the claim language

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Synopsys from further participation in, or dismissal of, this *inter partes* review.

and most naturally aligns with the inventor's description is likely the correct interpretation. *Id.* at 1250.

1. "Instrumentation Signal"

Construction of the term "instrumentation signal," required by each of the claims at issue in this proceeding, is central to the patentability determination. *See* PO Resp. 29-37; Reply 2-8. For example, claims 1 and 28 recite "including at least one instrumentation signal, wherein the instrumentation signal is indicative of an execution status." Claim 5, the third, and final, challenged independent claim, recites "creating an instrumentation signal associated with at least one synthesizable statement contained in a register transfer level (RTL) synthesizable source code."

a. Construction Adopted in the Decision to Institute

Although neither the petition nor the preliminary response set forth a specific construction for "instrumentation signal," the Board adopted, for purposes of the Decision to Institute, an interpretation that "the claimed instrumentation signal at least encompasses an output signal created during synthesis of RTL source code by inserting additional logic, preserved from the source code, that indicates whether the corresponding RTL source code statement is active." Decision to Institute 10.

Mentor Graphics argues that this construction is only partially correct. PO Resp. 30. Specifically, Mentor Graphics agrees that "instrumentation signals" encompass "inserting additional logic." *Id.* According to Mentor Graphics, however, the requirement that the "additional logic is preserved from the source code" is contrary to how one of ordinary skill in the art would understand the term in light of the specification. *Id.* at 35 (citing Ex. 2027 ¶¶ 38-39). Mentor Graphics points to language in the '376 patent

specification stating that "[i]nstrumentation is the process of preserving high-level information through the synthesis process." PO Resp. 35-36 (quoting Ex. 1001, col. 5, ll. 3-4). Mentor Graphics's expert, Dr. Majid Sarrafzadeh, states that preserving information here refers to permitting relation back from the execution of the gate level netlist to the corresponding statements in the RTL source code, not the preservation of *logic* itself from the source code. Ex. 2027 ¶ 40.

We find this argument, along with the supporting evidence, persuasive. The language of the '376 patent also supports this conclusion. For example, immediately following the language quoted above, the '376 specification states that "[i]nstrumentation permits simulation of a gatelevel netlist at the level of abstraction of RTL simulation by *preserving some of the information* available at the source code level through the synthesis process." Ex. 1001, col. 5, ll. 4-8 (emphasis added).

b. Definition of "Instrumentation"

In proposing an alternative construction for "instrumentation signal," Mentor Graphics initially asserts that the customary meaning of the term "instrumentation" to those of skill in the art is "additional code inserted into a program to monitor and/or collect information about the program behavior or operation during program execution." PO Resp. 31. Dr. Sarrafzadeh testifies that this is how the term is "generally recognized and understood in the programming language arts." Ex. 2027 ¶ 30 (citing IEEE Standard Glossary of Software Engineering Terminology, IEEE Std 610.12-1990 at 41 ("Devices or instructions installed or inserted into hardware or software to monitor the operation of a system or component."); National Bureau of Standards [NBS] Special Publication 500-75 Validation, Verification, and

Testing of Computer Software at 48 (1981) ("The insertion of additional code into the program in order to collect information about program behavior during program execution.")). We agree that this is the ordinary and customary meaning of the first word—"instrumentation"—of the term "instrumentation signal."

c. Specification

Mentor Graphics further asserts that the term "instrumentation signal" requires that "the signal be provided by logic that is *additional* to the design logic resulting from the synthesis of the RTL source code." PO Resp. 30. In other words, the instrumentation signal cannot be created solely by preserving circuit components.

Synopsys argues that Mentor Graphics's construction is too narrow and that the broadest reasonable construction of "instrumentation signal" is broad enough to include creation solely using preservation of circuit components. Reply 4-8.

According to Mentor Graphics, one of ordinary skill would understand the following excerpts of the specification "to effectively define" "instrumentation signal" to require that instrumentation logic be added to the gate-level netlist (PO Resp. 31-32):

> Generally *instrumentation logic* is created for a synthesizable statement in the RTL source code either by modifying the RTL source code or by analyzing the RTL source code during the synthesis process. The *instrumentation logic* provides an output signal indicative of whether the corresponding synthesizable statement is active. A gate-level design including the instrumentation output signal is then synthesized. Referring to FIG. 2, *the resulting gate-level design 250 contains additional logic to create the additional instrumentation output signals* referenced in instrumentation data 238.

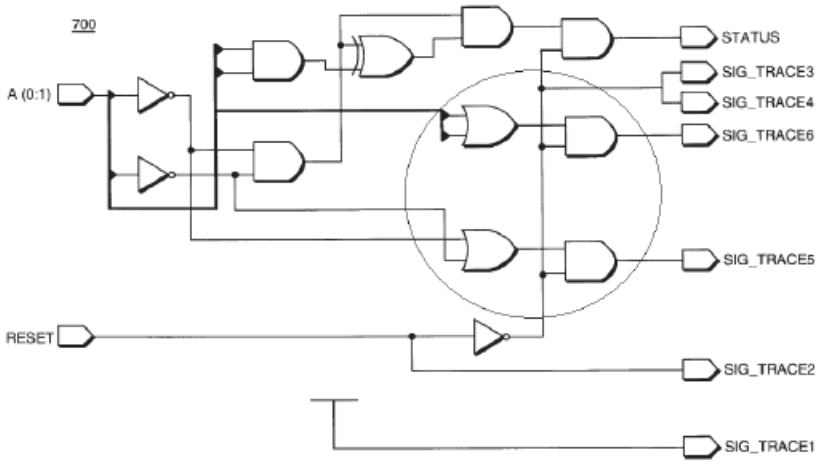
Ex. 1001, col. 5, ll. 21-30 (emphasis added by Mentor Graphics).

> FIG. 7 illustrates one embodiment of the logic 700 generated through instrumentation. In particular, FIG. 7 illustrates the *additional gate-level logic added* to generate signals SIG_TRACE1 through SIG_TRACE6 from synthesis of the modified source code.

Id. at col. 8, ll. 60-64 (emphasis added by Mentor Graphics). We are not persuaded that the quoted language qualifies as a limiting definition of "instrumentation signal." "To be his own lexicographer, a patentee must use 'a special definition of the term [that] is clearly stated in the patent specification or file history.'" *Laryngeal Mask Co. v. Ambu*, 618 F.3d 1367, 1372 (Fed. Cir. 2010) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1580 (Fed. Cir. 1996)). The specification here does not indicate clearly the patentee's intent to define or limit the definition of "instrumentation signal." Indeed, the first excerpt relied upon by Mentor Graphics is extracted from a paragraph that begins: "In one embodiment . . . ." Similarly, the second excerpt begins by stating that it "illustrates one embodiment." Thus, all of the language relied upon by Mentor Graphics as "effectively defin[ing]" the term, refers only to illustrative examples. It is well-settled that when claim language is broader than the preferred embodiment, the claims are not to be confined to that embodiment. *DSW, Inc. v. Shoe Pavilion, Inc.*, 537 F.3d 1342, 1348 (Fed. Cir. 2008). Moreover, "just as the preferred embodiment itself does not limit claim terms, mere inferences drawn from the description of an embodiment of the invention cannot serve to limit claim terms, as they are insufficient to require a narrower definition of a disputed term." *Johnson Worldwide Assocs., Inc. v. Zebco Corp.*, 175 F.3d 985, 992 (Fed. Cir. 1999) (internal citations omitted).

Mentor Graphics adds that Figure 7, which "illustrates the additional gate-level logic added to generate signals SIG_TRACE1 through SIG_TRACE6 from synthesis of the modified source code [shown in Figure 6]" (Ex. 1001, col. 8, ll. 61-64), supports its narrow construction. Dr. Sarrafzadeh testifies that this can be shown with an annotated copy of Figure 7, reproduced below.

FIG. 7



Ex. 2027 ¶ 33. The annotated copy of Figure 7, above, illustrates gate-level logic synthesized from modified RTL source code. Ex. 1001, col. 3, ll. 29-30. Dr. Sarrafzadeh testifies that the circle was added to emphasize the instrumentation logic (two AND gates and two OR gates) added to the original circuit shown in Figure 5. Ex. 2027 ¶ 33.

As pointed out by Synopsys (Reply 6), however, this Figure actually supports a broader construction of "instrumentation signal." The additional logic within the marked circle is required only for four (SIG_TRACE3, SIG_TRACE4, SIG_TRACE5, and SIG_TRACE6) of the six instrumentation signals included in the figure. SIG_TRACE1 and SIG_TRACE2 are shown with no additional logic gates. Mentor Graphics

attempts to explain away this incongruity in its argument by stating that the specification itself is incorrect. For example, at the final hearing, in response to the question "[w]hat you're telling us about additional logic, is it consistent with the patent at column 9 when it talks about Figure 10 where it calls SIG_TRACE1 and SIG_TRACE2 instrumentation signals?" counsel for Mentor Graphics stated:

> The patent with respect to Figures 7 and 10 calls all of the added signals instrumentation signals, that is correct, but we do not believe that all of those are instrumentation signals as that term should be included. It was an unfortunate, but expedient way to group all of the signals that have been added to Figure 7 and Figure 10. Some of those signals do not, however, provide any additional information. First, they're not logic.

Paper 59 (Transcript) 28-29. We are not persuaded that the term "instrumentation signal" should be limited such that it is inconsistent with explicit statements in the specification.

d. Alternate Embodiment

In addition, Mentor Graphics argues that the challenged claims should be construed to exclude the cross-reference embodiment. PO Resp. 33. The '376 patent explicitly states that in the cross-reference embodiment, "the gate-level netlist is not modified but the instrumentation signals implementing the instrumentation logic are contained in a cross-reference database." Ex. 1001, col. 2, ll. 47-50. Moreover, in both of the main embodiments, "instrumentation signals indicate the execution status of the corresponding cross-referenced synthesizable statement." *Id.* at ll. 50-52. Thus, in order to limit the definition of "instrumentation signal" as used in claims 1, 5, and 28 to signals created by additional instrumentation logic added to the gate-level netlist, Mentor Graphics contends that the challenged

claims exclude this embodiment. PO Resp. 33. Specifically, Dr. Sarrafzadeh testifies that "[c]laims 1, 5 and 28 do not describe [the cross-reference] embodiment because in this embodiment, rather than adding instrumentation signals (and associated logic) to the specified circuit, an external 'cross-reference database' uses 'already existing signals' to evaluate whether a particular line of source code is active." Ex. 2027 ¶ 35 (citing Ex. 1001, col. 5, ll. 31-37). This argument is circular, however, and does not explain why claims 1, 5, and 28 require additional logic be added to the gate-level netlist.

Moreover, during cross-examination, Dr. Sarrafzadeh admitted to not understanding the details of how the alternate cross-reference embodiment would work. For example, when questioned about language in the specification stating that "[w]ith respect to source code analysis, cross-reference instrumentation data including the instrumentation signals can be used to count the number of times a corresponding statement is executed in the source code" (Ex. 1001, col. 2, l. 66 – col. 3, l. 2), Dr. Sarrafzadeh answered that the '376 patent does not "show a method for doing this, [the patent] just draw[s] certain conclusions, and without showing and describing these designs, I would not have—it would not be clear what they mean here." Ex. 1019, 28:19 – 29:13. Further, Dr. Sarrafzadeh stated that his conclusions related to the cross-reference embodiment were based on his determination that the specification did not explain in detail how it would be implemented. *Id.* at 21:23 – 22:25.

It is true that "claims need not be construed to encompass all disclosed embodiments when the claim language is clearly limited to one or more embodiments." *TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc.*, 529 F.3d

1364, 1375 (Fed. Cir. 2008). Here, the claim language is broad enough to include the alternative cross-reference embodiment. Moreover, the written description does not evidence a clear intent to limit the invention to a singular embodiment. In fact, as described above, the specification describes two main embodiments, and multiple alternate embodiments that combine the two main embodiments. In fact, the first embodiment of the '376 patent is described in the most detail; however, "although the specifications may well indicate that certain embodiments are preferred, particular embodiments appearing in a specification will not be read into the claims when the claim language is broader than such embodiments." *Electro Med. Sys., S.A. v. Cooper Life Scis., Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994). In the present case, neither the claim language nor the specification suggests limiting the scope of the subject matter to a single embodiment.

e. Examiner's Reasons for Allowance

Mentor Graphics also points to the following language in the "'examiner's statement of reasons for allowance' in application (SN 09/127,584) that issued as the '376 patent" (PO Resp. 33):

> The current invention allows for the *insertion of instrumentation logic* which executes to function as a simulation breakpoint to be applied to gate-level circuit simulation. This is done by *inserting instrumentation points into the Register Transfer Level (RTL) design*, which can then be synthesized to the gate-level description . . . . The current invention extends [the higher level debugging of cited prior art] to a lower level in the design process, namely in the gate-level description that has been synthesized from the RTL description. This advantageously allows for the use of simulation breakpoints implemented by *inserting "instrumentation logic*

> *into the RTL description* (as indicated in the specification pg. 42, line 24) in a gate-level circuit simulation.

Ex. 2027 ¶ 35 (quoting Ex. D) (underlining in original; italics added by Mentor Graphics). We are not persuaded by this argument. The language quoted from the reasons for allowance makes it clear that the invention *allows for*, but does not state that the invention *requires*, additional logic to be added to the gate-level netlist resulting from the synthesis of the RTL source code. Moreover, Mentor Graphics neglects to include, in the quoted language, the last sentence of the paragraph, which states: "This provides a distinct advance over the prior art methods of matching input vectors to output vectors and attempting to back out the fault based only on these vectors." Ex. 2027: Ex. D at 106. This last sentence clarifies that the Examiner's statements were directed to distinguishing the claimed process of using instrumentation signals from the prior art methods of comparing input and output vectors, not to providing a definition of "instrumentation signal" or indicating that the instrumentation signal cannot be created solely using preservation of circuit components.

f. Definition of "Instrumentation Signal"

Thus, although we agree with Mentor Graphics that the definition of "instrumentation signal" does not require that additional logic inserted during synthesis of RTL source code is "preserved from the source code," we do not agree that "instrumentation signal" excludes creation by preserving already existing circuit components. Instead, we determine that the broadest reasonable construction of "instrumentation signal," in light of the '376 patent specification, at least includes an output signal created during synthesis of RTL source code by inserting additional code into a

program that indicates whether the corresponding RTL source code statement is active.

2. "Execution Status"

The term "execution status" is recited in claims 1-4, 28, and 29. Mentor Graphics states that "in the HDL context, 'execution status' refers to information regarding whether particular HDL statements have been executed or not." PO Resp. 37 (citing Ex. 2027 ¶ 41). This definition is consistent with the use of the term in the '376 patent. For example:

> In some cases the execution status of each branch of the code can be determined even though every branch is not explicitly instrumented. To verify the execution status of every branch, the instrumentation process need only ensure that each branch is instrumented either explicitly or implicitly through the instrumentation of other branches.

Ex. 1001, col. 12, ll. 33-38.

Synopsys does not address explicitly this proposed definition.

We determine that the broadest reasonable construction of "execution status" in light of the '376 patent specification is information regarding whether a particular HDL instruction has been performed.

D. Alleged Anticipation by Gregory under 35 U.S.C. § 102(e)

Synopsys asserts that claims 1-9, 11, 28, and 29, are unpatentable under 35 U.S.C. § 102(e) as anticipated by Gregory. As discussed above, claims 1, 5, and 28 are independent. Claims 2, 3, and 4 depend, directly or indirectly, from claim 1. Claims 6-9 and 11 depend, directly or indirectly, from claim 5. Claim 29 depends from claim 28.

To establish anticipation, each and every element in a claim, arranged as is recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008);

Karsten Mfg. Corp. v. Cleveland Golf Co., 242 F.3d 1376, 1383 (Fed. Cir. 2001).

We have reviewed Synopsys's anticipation argument and supporting evidence, including Gregory's disclosure and the detailed claim chart appearing on pages 31-43 of the Petition. The claim chart persuasively reads all elements of each of claims 5, 8, and 9 onto the disclosure of Gregory. Despite the counter-arguments in Mentor Graphics's Patent Owner Response, and the evidence cited therein, which we also have considered, Synopsys has shown, by a preponderance of the evidence, that each of claims 5, 8, and 9 is unpatentable under 35 U.S.C. § 102(e) as anticipated by Gregory. *See* 35 U.S.C. § 316(e).

For claims 1-4, 6, 7, 11, 28, and 29, however, we give significant weight to the testimony of Mentor Graphics's expert, Dr. Sarrafzadeh, who persuasively explains that Gregory does not disclose each and every element of the claims. Synopsys does not provide sufficient evidence to rebut this testimony. Thus, as described below, we conclude that Synopsys has not met its burden to show by a preponderance of the evidence, as required by 35 U.S.C. § 316(e), that claims 1-4, 6, 7, 11, 28, and 29 are unpatentable.

1. Gregory (Ex. 1007)

Gregory "relates to . . . debugging digital circuits constructed using logic or behavioral synthesis." Ex. 1007, col. 1, ll. 12-15. Gregory describes a method of "providing a designer with the ability to mark the synthesis source code in the places that the designer wants to be able to debug" by "mark[ing] the source code with a particular text phrase, such as 'probe[,'] along with some additional optional information." *Id.* at col. 8, ll. 21-26. Further, Gregory describes a translation process that "interjects

information into the netlist" when it encounters a probe statement and "generates a circuit th[at] provides the same function as it did without the 'probe' statement, but adds additional information or components to the initial circuit that indicate that certain components should not be replaced during optimization" (col. 8, ll. 26-30). These components "are traceably related to the source HDL" and they "facilitate[] debugging." *Id.* at col. 8, ll. 35-41.

2. Claims 1-4, 28, and 29

Synopsys asserts that Gregory discloses claim 1's limitation of "synthesizing the source code into a gate-level netlist including at least one instrumentation signal, wherein the instrumentation signal is indicative of an execution status of the at least one statement." Pet. 31-32. Synopsys explains that "[s]ynthesizing the FIG. 8 VHDL code produces the gate-level circuit illustrated in FIG. 9, which includes the instrumentation signal tempout, which indicates an execution status of the instrumented statement." *Id.* at 32. Figures 8 and 9 of Gregory are reproduced below.

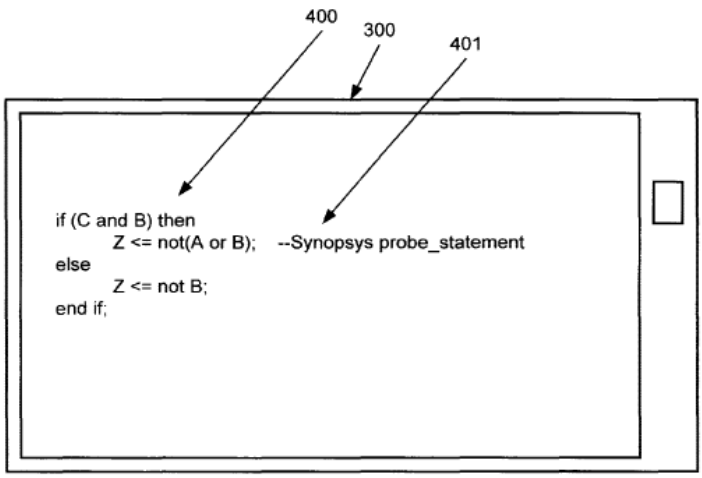


Figure 8, above, illustrates VHDL source code with a probe inserted.

Ex. 1007, col. 9, ll. 55-56. Gregory explains that the probe is "a directive to the translator" that "indicates that this particular VHDL statement should be processed so that it will be possible to relate analysis information to this point in the circuit." *Id*. at col. 12, ll. 54-61.

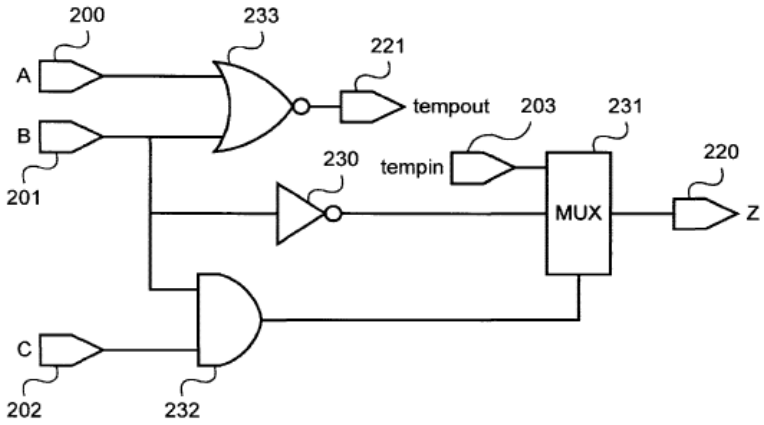


Figure 9, above, illustrates a circuit that a translator could produce using the source code with probe inserted shown in Figure 8. *Id*. at ll. 62-67. As discussed, Synopsys points to "tempout" as constituting the instrumentation signal. Pet. 32.

Mentor Graphics argues that tempout does not equate to the claimed "instrumentation signal" and Synopsys has not shown that Gregory discloses an "instrumentation signal, wherein the instrumentation signal is indicative of an execution status of the at least one statement."

Mentor Graphics argues that Gregory fails to disclose the claimed "instrumentation signal" because "tempout" does not involve additional logic, but instead simply preserves identified circuit nets during the optimization process. PO Resp. 41-46. This argument, however, requires a narrower construction of the term "instrumentation signal" than we have adopted, as discussed above. Thus, we agree with Synopsys that "tempout" qualifies as an "instrumentation signal" as we have construed that term.

Mentor Graphics also argues that "tempout" is not "indicative of an execution status," as required by claim 1. *Id.* at 46-50. Mentor Graphics points out that, in its petition, the only element Synopsys describes with particularity as disclosing this particular limitation of claim 1 is the "tempout" signal of Figure 9. *Id.* at 49-50. Dr. Sarrafzadeh testifies that in Figure 9, the result of the "tempout" signal is not indicative of the execution status of the HDL statement identified in Figure 8. Ex. 2027 ¶ 73. According to Dr. Sarrafzadeh, "tempout" reflects the result of "not (A or B)," while the HDL statement identified in Figure 8 is "Z<=not (A or B)," executed conditionally based on whether the "if" condition (if (C and B) then)) is true. *Id.* at ¶¶ 73-74. The execution status of the HDL statement thus depends on whether the "if" condition is true or not, but "tempout" does not indicate this information. *Id.*

In response to this argument, Synopsys asserts that Mentor Graphics improperly is looking solely at the 'tempout' signal and, in doing so, excluding an alternate embodiment also described in Gregory. Reply 10-11. Specifically, Synopsys argues that because execution status of every branch can be verified implicitly and not every branch need be instrumented, Mentor Graphics's argument is incorrect. *Id.* at 11 (citing Ex. 1001, col. 12, ll. 33-38). According to Synopsys, it is not necessary to determine the "C and B" condition in the "if" statement of Figure 8 to meet the "execution status" requirement. *Id.* Synopsys, however, does not point to any expert testimony to support these statements.

We give substantial weight to Mentor Graphics's expert testimony. Dr. Sarrafzadeh explains, persuasively, that the "tempout" signal is not "indicative of an execution status of the at least one statement" as required

by claim 1, where "execution status" is information regarding whether the particular source code instruction, identified in Figure 8, has been performed. *See* Ex. 2027 ¶¶ 73-78. Synopsys's unsupported argument to the contrary is not persuasive. Moreover, Synopsys only points to "tempout" in its petition (Pet. 32; 42-43) as disclosing this element of claim 1. Whether or not a particular embodiment requires the execution status of every branch to be verified explicitly, the claim language of claim 1 requires an "instrumentation signal, wherein the instrumentation signal is indicative of an execution status of the at least one statement." Synopsys has not shown persuasively that the "tempout" signal of Figure 9 discloses this limitation.

Gregory does not state explicitly that "tempout," or any other element, indicates an "execution status" of an HDL instruction. Although, as discussed, Gregory states that a probe "is a directive to the translator" that "indicates that this particular VHDL statement should be processed so that it will be possible to relate analysis information to this point in the circuit," (col. 12, ll. 54-61), we agree with Mentor Graphics that Synopsys does not point to any disclosure in Gregory that "analysis information" includes "execution status." PO Resp. 47. In fact, when Gregory discusses "analysis," it generally refers to characteristics of the circuit, such as timing and power, which are not related to "execution status" as we have construed that term. *See, e.g.*, Ex. 1007, col. 7, l. 59 – col. 8, l. 10; col. 12, ll. 49-61; col. 16, ll. 25-50.

Alternatively, Synopsys argues that Gregory *does* indicate the execution status of the "if" condition at the output of AND gate 232 in Figure 9. Reply at 11. Here, Synopsys appears to be arguing that B and C,

as opposed to the "tempout" signal, are the claimed "instrumentation signals." *Id.* ("Any argument that signals B and C cannot be instrumentation signals ignores the alternate embodiment which specifically contemplates implicit instrumentation and the use of already existing signals to determine execution status.").

We are not persuaded by this argument. To the extent that Synopsys is arguing that an element other than "tempout" discloses this limitation of claim 1, the argument is presented for the first time in Synopsys's reply and is not responsive to arguments made in Mentor Graphics's response. 37 CFR 42. 23(b). Moreover, Synopsys does not point to any evidence or persuasive argument to explain how B and C disclose the claimed instrumentation signal.

Synopsys has not shown that Gregory discloses the limitation "instrumentation signal, wherein the instrumentation signal is indicative of an execution status of the at least one statement." Thus, we conclude that Synopsys has not met its burden to show, by a preponderance of the evidence, that Gregory anticipates independent claim 1. *See* 35 U.S.C. § 316(e). Because independent claim 28 includes the same limitation, Synopsys also has not met its burden to show, by a preponderance of the evidence, that Gregory anticipates independent claim 28. For the same reasons, we conclude that Synopsys has not met its burden with regard to claims 2-4 and 29, which depend, either directly or indirectly, from claims 1 and 28.

3. Independent Claim 5

Independent claim 5 includes the limitation "creating an instrumentation signal associated with at least one synthesizable statement

contained in a register transfer level (RTL) synthesizable source code." Synopsys points to the analysis of claim 1 to show that this limitation is anticipated by Gregory. Pet. 34. In addition, to support its argument, Synopsys points to Gregory's Figures 12, 16, and 18 and the associated text describing a "block probe methodology for instrumenting all of the signals within a process statement." *Id.* at 34-35. Specifically, Synopsys asserts that the "signals 'temp_out' in FIG. 18 are instrumentation signals associated with the VHDL (RTL) statements within the instrumented 'process.'" *Id.* at 35. Figures 12, 16, and 18 are reproduced below.

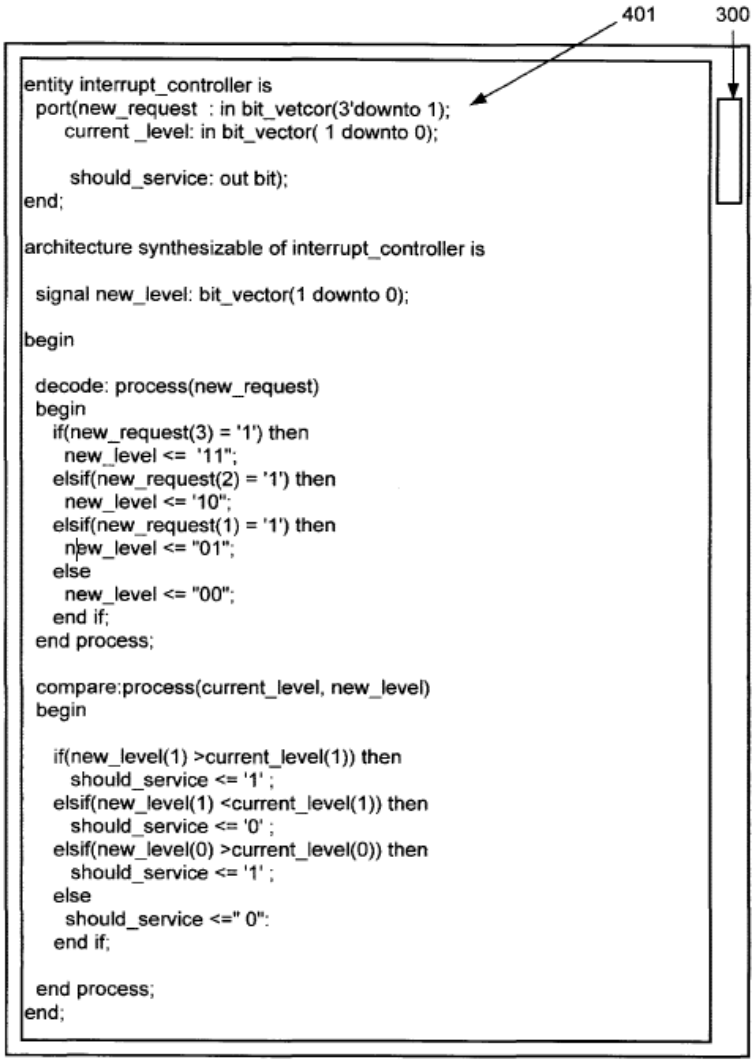
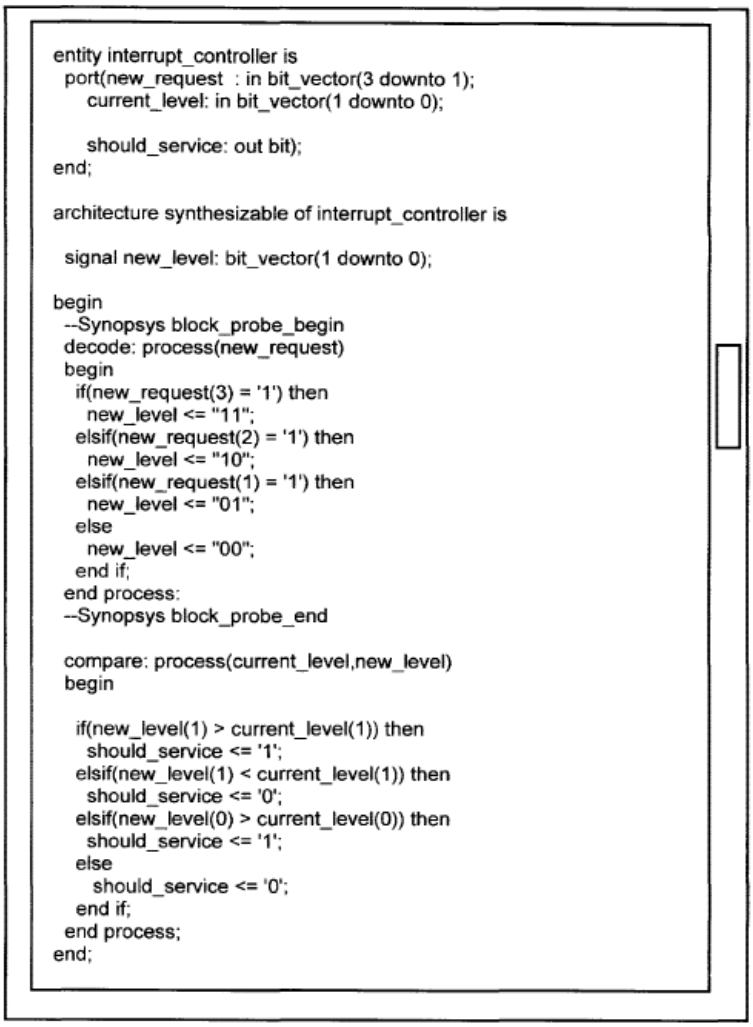


Figure 12

Figure 12, above, illustrates VHDL source code without probes using two process blocks. Ex. 1007, col. 9, ll. 64-65.



```
entity interrupt_controller is
  port(new_request  : in bit_vector(3 downto 1);
     current_level: in bit_vector(1 downto 0);

     should_service: out bit);
end;

architecture synthesizable of interrupt_controller is

  signal new_level: bit_vector(1 downto 0);

begin
  --Synopsys block_probe_begin
  decode: process(new_request)
  begin
    if(new_request(3) = '1') then
      new_level <= "11";
    elsif(new_request(2) = '1') then
      new_level <= "10";
    elsif(new_request(1) = '1') then
      new_level <= "01";
    else
      new_level <= "00";
    end if;
  end process;
  --Synopsys block_probe_end

  compare: process(current_level,new_level)
  begin

    if(new_level(1) > current_level(1)) then
      should_service <= '1';
    elsif(new_level(1) < current_level(1)) then
      should_service <= '0';
    elsif(new_level(0) > current_level(0)) then
      should_service <= '1';
    else
       should_service <= '0';
    end if;
  end process;
end;
```

Figure 16

Figure 16, above, illustrates the VHDL source code of Figure 12 with two block probes installed. *Id.* at col. 10, l. 7.

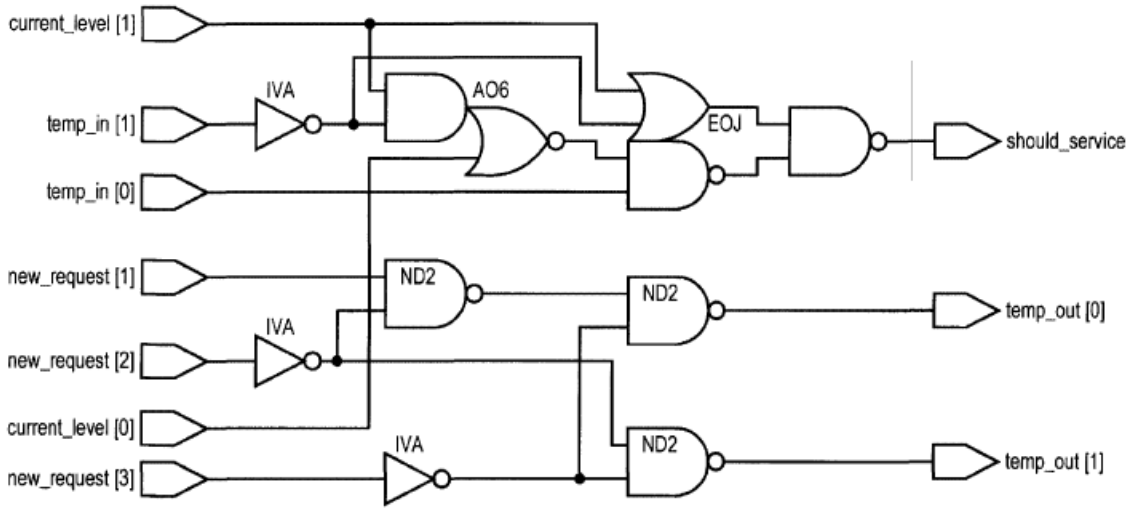


Figure 18, above, illustrates the circuit obtained by optimizing the circuit of Figure 17—a circuit generated by translating the VHDL source code of Figure 16. *Id.* at col. 10, ll. 9-12.

Mentor Graphics argues that Gregory fails to disclose the claimed "instrumentation signal" because "temp_out" does not involve additional logic, but instead simply preserves identified circuit nets during the optimization process. PO Resp. 53-56. This argument, however, requires a narrower construction of the term "instruction signal" than we have adopted, as discussed above.

Mentor Graphics also argues, without detailed explanation, that "[t]he proposed challenges to claims 3, 4, 5, 6, 7, 9, 11, 28, and 29 rely on portions of Gregory that are not arranged as recited in the claim." *Id.* at 40. This argument appears to be based on the statement in Gregory that Figures 12-19 "show another way to use probes to evaluate the performance of blocks of HDL code." Ex. 2007, col. 13, ll. 29-31. Thus, according to Mentor Graphics, the challenges to all the recited claims improperly combine portions of Gregory concerning Figures 12 and 16 with an alternate embodiment described in Figures 8 and 9. We are not persuaded that

Figures 12 through 19 are an entirely separate embodiment from that described in Figures 8 and 9. Instead, the difference between the two examples is that the initial source code differs. *See id.* at Figs. 8, 12. Furthermore, as described below, Gregory discloses all the limitations of claim 5 without any improper combination of embodiments.

We conclude that Gregory discloses all the limitations of claim 5 arranged as recited in the claim. Gregory discloses "a method of generating a gate level design." Ex. 1007, Abstract. Gregory also discloses "synthesizing the source code into a gate-level design having the instrumentation signal" by describing that the translation, or synthesis process, injects information into the resulting netlist when a probe is encountered, which results in components of the final circuit that are traceably related to the source code. Ex. 1007, col. 8, ll. 21-30. Either "tempout," as shown in Figure 9, or "temp_out," as shown in Figure 18, qualifies as "instrumentation signals" as construed above.

Finally, we determine that Gregory discloses "creating an instrumentation signal associated with at least one synthesizable statement contained in a register transfer level (RTL) synthesizable source code" as required by claim 5. For example, Gregory states that "any analytic result related to [tempout of Figure 9] . . . can be identified with the probe statement 401 in the HDL." Ex. 1007, col. 13, ll. 15-20. This language describes an "instrumentation signal" ("tempout") "associated" (identified) "with at least one synthesizable statement" (statement 401 in the HDL of Figure 8).

4. Dependent claims 6 and 7

Claim 6 depends from claim 5 and adds the limitation:

> wherein step a) further comprises the step of:
>
> (i) inserting a unique variable assignment statement into the source code, wherein the variable assignment statement is adjacent to at least one associated sequential statement; and
>
> (ii) inserting a unique output signal assignment statement into the source code, wherein the unique output signal is assigned a value associated with the unique variable.

Synopsys relies on Figures 16 and 18 of Gregory as disclosing this additional limitation. Pet. 35-36. Specifically, Synopsys asserts that the statements in Figure 16 adjacent each of the if, elsif, and else statements ("new_level <=") qualify as unique local variable statements. *Id.* at 35. Synopsys adds that synthesizing the VHDL code in Figure 16 produces the circuit of Figure 18 with "instrumentation signals" "temp_out" that are "assigned the value of the new_level local variable with a[n] initial, second value." *Id.* at 36.

Mentor Graphics argues that Gregory does not disclose the "variable assignment statement" limitation of claim 6. PO Resp. 56-57. Again, we give substantial weight to Mentor Graphics's expert testimony on this issue. Dr. Sarrafzadeh testifies, persuasively, that the "new_level" assignment in Figure 16 is a *signal* assignment and not a *variable* assignment. Ex. 2027 ¶ 84 (explaining that in VHDL variables are declared by the term "VARIABLE" and signals are assigned using the symbol ":="). Dr. Sarrafzadeh explains that "Gregory does not disclose including variable assignments, but instead only preserves signal assignments," which are substantively different than variable assignments. *Id.* at ¶¶ 85-87.

In response, Synopsys argues that Mentor Graphics does not use the broadest reasonable construction of the term "variable assignment statement" and improperly limits the scope of the claim to distinctions in terms provided by VHDL when the specification broadly talks about other HDL languages. Reply 13-14. We are not persuaded by Synopsys's argument. Mentor Graphics, in explaining its argument in terms of VHDL, is not limiting the scope of the claimed subject matter, but instead is responding to Synopsys's assertion that certain VHDL code shown in Gregory discloses the limitations of claim 6. We conclude that Synopsys has not met its burden with regard to claim 6. For the same reasons, we conclude that Synopsys has not met its burden with regard to claim 7, which depends from claim 6.

5. Dependent Claims 8 and 9

Claim 8 depends from claim 5 and adds the limitation:

> wherein step a) is repeated to create a unique instrumented output signal for each list of sequential statements in the source code, wherein each list corresponds to a synthesizable executable branch of the source code.

Synopsys relies on Figure 16 of Gregory as disclosing this additional limitation. Pet. 36-37. Specifically, Synopsys asserts that the "VHDL of FIG. 16 creates a unique instrumented output signal corresponding to the unique values of new_level for each list of sequential (if-then) statement," each of the statements being in a different branch of the VHDL. *Id.* at 37.

Claim 9 depends from claim 5 and adds the limitation:

> c) generating cross-reference instrumentation data mapping each statement in a selected list to the instrumented output signal associated with that list for every list in the source code.

Synopsys relies on Figure 16 and related language in Gregory as disclosing this limitation. Pet. 37 (citing Ex. 1007, col. 8, ll. 35-41).

For claim 8, Mentor Graphics relies solely on its argument made for claim 5 that Gregory fails to disclose the claimed "instrumentation signal" because "temp_out" does not involve additional logic, but instead simply preserves identified circuit nets during the optimization process. PO Resp. 59. As discussed, this argument is not persuasive.

For claim 9, Mentor Graphics also argues, without detailed explanation, that "[t]he proposed challenges to claims 3, 4, 5, 6, 7, 9, 11, 28, and 29 rely on portions of Gregory that are not arranged as recited in the claim." *Id.* at 40. As discussed above, we do not find this argument persuasive.

We conclude that Gregory discloses all the limitations of dependent claims 8 and 9.

6. Dependent Claim 11

Claim 11 depends from claim 5. Mentor Graphics argues that in its claim chart, Synopsys does not assert that claim 11 is anticipated by Gregory, but only that it would have been obvious over Gregory. Pet. 38. In reply, Synopsys states that "the Petition explicitly states that 'Gregory (Ex. 1007) *anticipates* claims 1-9, 11-14, 24-25 and 28-33 under section 102.'" Reply 15 (citing Pet. 4, 12, 38). This statement, however, is not evidence of anticipation. We agree with Mentor Graphics that nothing in the petition or in further briefing points to any language in Gregory that discloses all the limitations of claim 11. Thus, Synopsys has not met its burden with regard to claim 11.

E. Mentor Graphics's Motion to Amend Claims

Mentor Graphics filed a motion to amend claims. Paper 31 ("Mot. to Amend"). Mentor Graphics proposes nine substitute claims 34-36 and 38-43.[3] Mentor Graphics proposes that substitute claims 34, 35, and 36 are contingent substitute claims to replace original independent claims 1, 5, and 28, respectively, to be considered only if the original patent claim it replaces is unpatentable. *Id.* at 5. Similarly, proposed substitute claims 38-43 are contingent substitute claims to replace original dependent claims 3, 6, 8, 9, 11, and 29, respectively. *Id.* Because we determine that claims 5, 8, and 9 are anticipated by Gregory, the contingency has materialized for these claims, and, thus, we consider proposed substitute claims 35, 40, and 41.

As the moving party, Mentor Graphics bears the burden of proof to establish that it is entitled to the relief requested. 37 C.F.R. § 42.20(c). The proposed amendment is not entered automatically, but only upon Mentor Graphics's having demonstrated the patentability of those substitute claims.

Mentor Graphics contends that the proposed substitute independent claim, 35, "introduce[s] language to more explicitly recite the meaning of the term 'instrumentation signal'" and that the dependent claims are changed solely to change the dependency to the proposed substitute independent claim that corresponds to the dependent claim's respective independent base claim. Mot. to Amend 5. Proposed substitute independent claim 35 is reproduced below, with underlined text indicating material inserted relative to that claim:

[3] Mentor Graphics initially proposed substitute claim 37 replace original claim 2 without any contingency. Mot. to Amend 5. Subsequently, this request was withdrawn. Paper 39, 1.

> 35. A method of generating a gate level design, comprising the steps of:
>
> a) creating an instrumentation signal associated with at least one synthesizable statement contained in a register transfer level (RTL) synthesizable source code; and
>
> b) synthesizing the source code into a gate-level design having the instrumentation signal, the synthesizing comprising generating instrumentation logic to provide the instrumentation signal, the instrumentation logic comprising instrumentation logic circuitry that is additional to circuitry specified in the source code.

Proposed dependent claims 40 and 41 are identical to the claims they are to replace, claims 8 and 9, except that instead of depending from claim 5, proposed claims 40 and 41 would depend from proposed claim 35. Mot to Amend 4.

1. No Broadening of Scope

Proposed substitute claims may not enlarge the scope of original patent claims. 35 U.S.C. § 316(d)(3); 37 C.F.R. § 42.121(a)(2)(ii). Proposed substitute claims 35, 40, and 41 merely add features to the claims for which they substitute and do not remove any limitation therefrom. Accordingly, no issue exists with regard to the prohibition against broadening original patent claims.

2. Patentability over Prior Art

a. Anticipation by Gregory

Mentor Graphics asserts that the technique disclosed in Gregory prevents already synthesized circuit elements and signals from being altered structurally during optimization. Mot. to Amend 13 (citing Ex. 2027 ¶¶ 49-52). According to Mentor Graphics, in Gregory, "[n]o additional logic is added to the relabeled signals such that they are structurally changed in any

way to indicate that the signals have been instrumented." *Id.* at 13-14 (citing Ex. 2027 ¶¶ 63, 67-69).

Synopsys argues that Gregory's Figure 18 discloses the additional instrumentation logic circuitry limitation required by the proposed substitute claims. Opp. 4-6. Synopsys's expert, Dr. Brad Hutchings, testifies that the addition of logic gates to Figure 18 is apparent by comparison with Figure 14. Ex. 1013 ¶ 31. Figure 14 of Gregory, reproduced below, shows the circuit that results from optimizing the circuit shown in Figure 13, which in turn is the circuit resulting from translating the VHDL source code shown in Figure 12. Ex. 1007, col. 14, ll. 5-7.

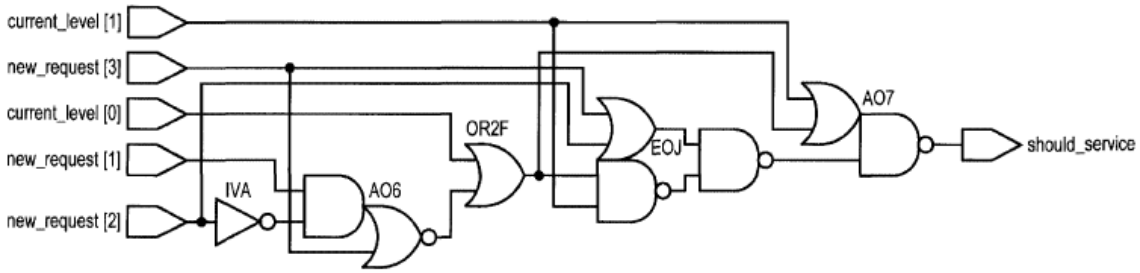


Figure 14, above, is a schematic for the circuit resulting from optimizing a circuit created by translating VHDL source code. *Id.* Figure 18, reproduced below, shows the circuit that results from optimizing the circuit shown in Figure 17, which in turn is the circuit resulting from translating the VHDL source code shown in Figure 16. *Id.* at col. 10, ll. 9-12.

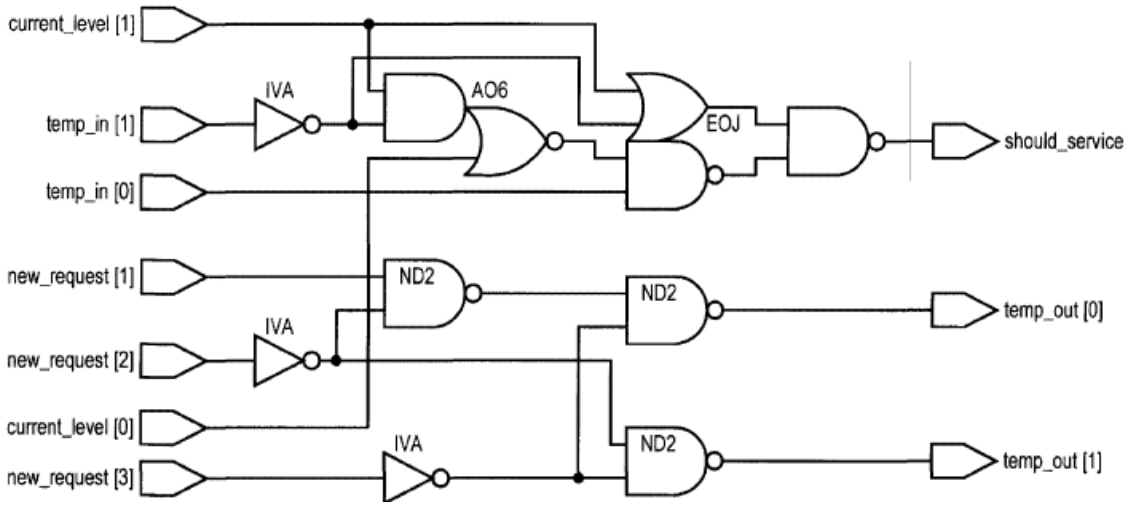


Figure 18, above, is a schematic for the circuit resulting from optimizing a circuit created by translating VHDL source code. *Id.* at col. 14, ll. 30-36. Because the VHDL source code in Figure 16 is the same as the VHDL source code in Figure 12 with block probes, or instrumentation, Figure 14 shows the circuit that results from translating uninstrumented source code, and Figure 18 shows the circuit that results from translating instrumented source code. Ex. 1013 ¶ 31; Ex. 1007, Fig. 12, 16; col. 9, ll. 64-65 ("Fig. 12. VHDL source without probes using two process blocks."); col. 10, l. 7 ("Fig. 16. VHDL source with two block probes installed.").

Dr. Hutchings testifies that the circuits of Figures 14 and 18 are "functionally identical but structurally different" and testifies that Figure 18 has a higher gate count than Figure 14. Ex. 1013 ¶ 32. Dr. Hutchings, however, does not testify affirmatively that the structural differences or the additional gate count are the result of the probes, as required by the proposed amendment, as opposed to the optimization process. *See id.* at ¶¶ 31-36.

Mentor Graphics responds that the differences in logic discussed by Dr. Hutchings come from the process of optimization, not additional logic resulting from probe statements. Paper 39, 2 ("Reply Mot. to Amend")

(citing Ex. 2027 ¶¶ 44, 51-53, 61-63). We are persuaded by Mentor Graphics's arguments and evidence that Gregory does not show "instrumentation logic comprising instrumentation logic circuitry that is additional to circuitry specified in the source code," as required by proposed substitute claims 35, 40, and 41.

b. Obviousness over Gregory

Mentor Graphics asserts that "one skilled in the art would not have been motivated to modify *Gregory* to include instrumentation logic circuitry that is additional to circuitry specified in the source code" because Gregory concerns software simulation and, therefore, eliminates the need for additional or generated instrumentation logic. Mot. to Amend 13-14 (citing Ex. 2027 ¶¶ 21, 27). Mentor Graphics asserts that "in view of the fundamental technical differences between Gregory and the claimed subject matter, any modification to Gregory such that the technique involved generating instrumentation logic circuitry that is additional to circuitry specified in the source code would change the principle of operation of *Gregory*." *Id.* at 14.

Synopsys argues that Mentor Graphics does not establish the nonobviousness of the proposed substitute claims over Gregory because it does not address the basic skill set possessed by a person of ordinary skill in the art and points to no evidence to support the assertion that one skilled in the art would not have been motivated to modify Gregory to include the additional logic circuitry limitation. Opp. 6. Dr. Hutchings testifies that "[n]umerous engineering texts and technical literature available to a person of ordinary skill in the art at the time of the invention taught inserting additional logic to debug circuits" and that an ordinary skilled artisan would

have known to use similar techniques when debugging synthesizable HDL. Ex. 1013 ¶¶ 37-38 (citing Ex. 1014-18). We give substantial weight to Dr. Hutchings's testimony on this issue, which is based on support from objective sources.

Mentor Graphics responds that Synopsys's "failure to present a strong showing of obviousness based on other references . . . render the alleged evidence insufficient to demonstrate obviousness." Reply Mot. to Amend 5. Mentor Graphics, however, misstates the burden required in this situation. It is Mentor Graphics who has the burden to show that it is entitled to the proposed substitute claims because they are patentable. Synopsys does not bear the burden to show that the claims are unpatentable.

We conclude, based on the record, that Mentor Graphics has not met its burden to show that independent claim 35 or claims 40 and 41, which depend from claim 35, would not have been obvious to a person of ordinary skill in the art based on the disclosure of Gregory.

c. Mentor Graphics's Burden

Moreover, distinguishing the proposed substitute claims only from the prior art references applied to the original patent claims is insufficient to demonstrate general patentability over prior art. As the moving party, a patent owner bears the burden to show entitlement to the relief requested. 37 C.F.R. § 42.20(c).

Mentor Graphics makes the conclusory statement, unsupported by evidence, that "the Patent Owner believes *Gregory* to be the closest known prior art and therefore believes the proposed substitute claims to be patentable over all known prior art." Mot. to Amend 14-15; *see also id.* at 11 ("Patent Owner believes *Gregory* to be the closest known prior art and is

not currently aware of any other prior art that would affect the patentability of the substitute claims.").

This statement is insufficient, without discussing the level of ordinary skill in the art, and what was previously known, with respect to each added feature, including the ordinary skill set possessed by such a hypothetical person. For each proposed claim, Mentor Graphics focuses on the added feature requiring additional instrumentation logic circuitry. However, Mentor Graphics reveals little, if anything, about the level of ordinary skill and what was previously known with respect to that feature.

In the context of the claim element added by Mentor Graphics, it is essential to know whether synthesizing source code, including additional instrumentation logic circuitry, pre-existed the claimed invention, in any context, and, if so, how it worked. Otherwise, Mentor Graphics is expected, reasonably, to explain such pre-existing art, and why it would not have been applicable to render the invention of the proposed substitute claims obvious to one with ordinary skill in the art. Mentor Graphics has failed to do either.

Without having discussed sufficiently, in its motion, the level of ordinary skill in the art and what was previously known regarding the features on which Mentor Graphics focuses for establishing patentability, Mentor Graphics has not, in its motion, set forth a prima facie case for the relief requested—that independent claim 35 and claims 40 and 41, are patentable—or satisfied its burden of proof.

3. Written Description Support

Because Mentor Graphics has not shown patentability of the proposed substitute claims over the prior art, we do not reach whether it has shown that the proposed substitute claims have written description support in the

'584 application as filed. We note that Mentor Graphics should have cited to the disclosure of the '584 application as filed rather than the disclosure of the '376 patent as issued.

Mentor Graphics's Motion to Amend Claims is *denied*.

F. Mentor Graphics's Motion to Exclude Evidence

Mentor Graphics filed a Motion to Exclude Evidence (Paper 42) seeking to exclude the Declaration testimony of Dr. Hutchings because it is not competent expert testimony. Mentor Graphics argues that Dr. Hutchings did not have an understanding of the claimed subject matter as a whole, including each limitation of the claim, and therefore his testimony fails to satisfy the criteria of Federal Rule of Evidence 702. Paper 42, 3-8. Mentor Graphics bases this assertion on Dr. Hutchings's testimony that he had not formed an opinion on the meaning of "execution status" or "instrumentation signal," but instead assumed that "the Board already ruled on anticipation, so I focused on the amended language" of the proposed substitute claims. *Id.* at 7-8 (quoting Ex. 2032, 97:3-11).

We agree with Synopsys that Dr. Hutchings's testimony should not be excluded. Mentor Graphics's objections to Dr. Hutchings's testimony go to the weight and sufficiency of his testimonial evidence, rather than its admissibility. *See Liquid Dynamics Corp. v. Vaughan Co.*, 449 F.3d 1209, 1221 (Fed. Cir. 2006) (citing *Quiet Tech. DC-8, Inc. v. Hurel-Dubois UK Ltd.*, 326 F.3d 1333, 1344-45 (11th Cir. 2003)); *In re TMI Litig.*, 193 F.3d 613, 692 (3d Cir. 1999) ("So long as the expert's testimony rests upon 'good grounds,' it should be tested by the adversary process—competing expert testimony and active cross-examination." (quoting *Ruiz–Troche v. Pepsi Cola of Puerto Rico Bottling Co.*, 161 F.3d 77, 85 (1st Cir.1998)));

Wilmington v. J.I. Case Co., 793 F.2d 909, 920 (8th Cir.1986) ("Virtually all the inadequacies in the expert's testimony urged here by [the defendant] were brought out forcefully at trial . . . . These matters go to the weight of the expert's testimony rather than to its admissibility."). Mentor Graphics had the opportunity to address any alleged deficiencies in Dr. Hutchings's testimony in the Reply in support of the Motion to Amend. *See* Reply Mot. to Amend 1, 3 (stating that Dr. Hutchings's testimony is "incompetent and entitled to no weight").

Nevertheless, we have reviewed the testimony in question and conclude that Dr. Hutchings has demonstrated appropriate credentials, adequate preparation, and sufficient understanding of the '376 patent. *See, e.g.*, Ex. 1013 ¶¶ 4-11, 19-22. Mentor Graphics does not point to any authority supporting its position. Here, Dr. Hutchings presumed the Board would adopt certain constructions for the terms in the claims and stated his opinions based on those constructions. This presumption was logical given that Dr. Hutchings opines only on proposed substitute claims that are contingent on a finding of anticipation. Nothing about this presumption indicates a lack of understanding of the claims.

Mentor Graphics's Motion to Exclude Evidence is *denied.*

G. Synopsys's Motion to Exclude Evidence

Synopsys filed a Motion to Exclude Evidence (Paper 44) seeking to exclude (1) all of Mentor Graphics's exhibits relating to assignor estoppel because they are not relevant; (2) all of Mentor Graphics's exhibits relating to the post-2006 relationship between EVE and Synopsys because they are not relevant; and (3) Exhibits 2030 and 2031 because they were not cited or explained in any paper, and Exhibit 2033 because it relates to conception

date of the '376 patent, which is not at issue in this proceeding.

We find it unnecessary to consider the specific objections to the admissibility of exhibits relating to assignor estoppel because Mentor Graphics has failed to demonstrate that assignor estoppel provides an exception to the statutory mandate, even assuming those exhibits to be admissible.

Similarly, we find it unnecessary to consider the specific objections to the admissibility of exhibits relating to the post-2006 relationship between EVE and Synopsys, because Mentor Graphics has failed to demonstrate that a real party-in-interest or privity relationship between EVE and Synopsis existed during the relevant time, even assuming those exhibits to be admissible.

Finally, we find it unnecessary to consider the objections to the admissibility of Exhibits 2030, 2031, and 2033. As pointed out by Synopsys, Exhibits 2030 and 2031 were not cited in any of the briefs. Mentor Graphics explains that the Exhibits are relevant to Dr. Hutchings's retraction of paragraph 33 of his deposition. Paper 47, 6. However, because Dr. Hutchings retracted paragraph 33, we did not rely on this portion of his testimony in making our decision. Thus, we also have not relied on Exhibits 2030 and 2031. We similarly have not relied on Exhibit 2033, a declaration submitted by Mentor Graphics to swear behind the Boubezari reference (*Id.* at 7) because we did not reach that issue in deciding this case.

The motion is dismissed as moot, because even considering the evidence that Synopsys seeks to exclude, we either have not reached the issue to which the evidence relates or we have decided the issue in Synopsys's favor.

III. CONCLUSION

Synopsys has not shown by a preponderance of the evidence that claims 1-4, 6, 7, 11, 28, and 29 of the '376 patent are unpatentable under 35 U.S.C. § 102(e) over Gregory.

Synopsys has shown by a preponderance of the evidence that claims 5, 8, and 9 of the '376 patent are unpatentable under 35 U.S.C. § 102(e) over Gregory.

Mentor Graphics has not shown that its proposed substitute claims 34-36 and 38-43 are patentable over the prior art.

Accordingly, it is

ORDERED that claims 5, 8, and 9 of the '376 patent are CANCELLED;

FURTHER ORDERED that Mentor Graphics's Motion to Amend Claims is *denied*;

FURTHER ORDERED that Mentor Graphics's Motion to Exclude Evidence is *denied*;

FURTHER ORDERED that Synopsys's Motion to Exclude Evidence is *dismissed.*

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