

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MENTOR GRAPHICS CORPORATION,
Petitioner,

v.

SYNOPSIS, INC.,
Patent Owner.

Case IPR2014-00287
Patent 6,836,420 B1

Before JENNIFER S. BISK, SCOTT A. DANIELS, and
PHILIP J. HOFFMANN, *Administrative Patent Judges*.

DANIELS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. *Background*

Mentor Graphics Corporation (“Petitioner”) filed a Petition to institute an *inter partes* review of claims 1–3, 10–13, and 20 of U.S. Patent No. 6,836,420 B1 (“the ’420 patent”). Paper 6 (“Pet.”).¹ We instituted trial for claims 1–3, 10–13, and 20 of the ’420 patent on certain grounds of unpatentability alleged in the Petition. Paper 9 (“Decision to Institute” or “Inst. Dec.”).

After institution of trial, on September 17, 2014, Patent Owner, Synopsys, Inc., (“Patent Owner”), filed a Patent Owner Response (“PO Resp.”), along with a Declaration by Patent Owner’s Declarant, Dr. Brad Hutchings (“Hutchings Declaration”). Subsequently, Petitioner filed a Reply (“Reply”) on December 12, 2014 and a Declaration in support of the Reply by Petitioner’s Declarant, Mr. Edward Detjens (“Reply Declaration”). Paper 22.

A hearing for IPR2014-00287 was held on March 10, 2015. The transcript of the hearing has been entered into the record. Paper 30 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a).

Petitioner has shown by a preponderance of the evidence that claims 1–3, 10–13, and 20 of the ’420 patent are unpatentable based on the combination of Vander Zanden and Shand. Petitioner has not shown that the challenged claims are unpatentable over any of the other proposed grounds.

¹ We refer to the corrected Petition filed January 15, 2014.

B. The '420 Patent

The '420 patent (Ex. 1001) generally relates to memory circuit design and specifically, a method and corresponding digital circuit design for resettable memory. Ex. 1001, 1:7–10. The '420 patent states, as a matter of background, that the circuitry for a conventional resettable memory unit is complicated and expensive because “each n wide storage cell is implemented with resettable flip-flops that are individually accessed via complicated multiplexing and control circuitry.” *Id.* at 1:65–67. According to the patent, such a resettable memory unit is relatively slow and consumes more silicon surface area than a non-resettable memory unit. *Id.* at 2:3–6.

A solution to these challenges, proposed by the '420 patent, is designing resettable memory 220 as a combination of memory unit without reset 201, and memory unit with reset 205. *Id.* at 1:61–2:2, Fig. 2A. Figure 2A of the '420 patent, illustrating resettable memory 220, is reproduced below.

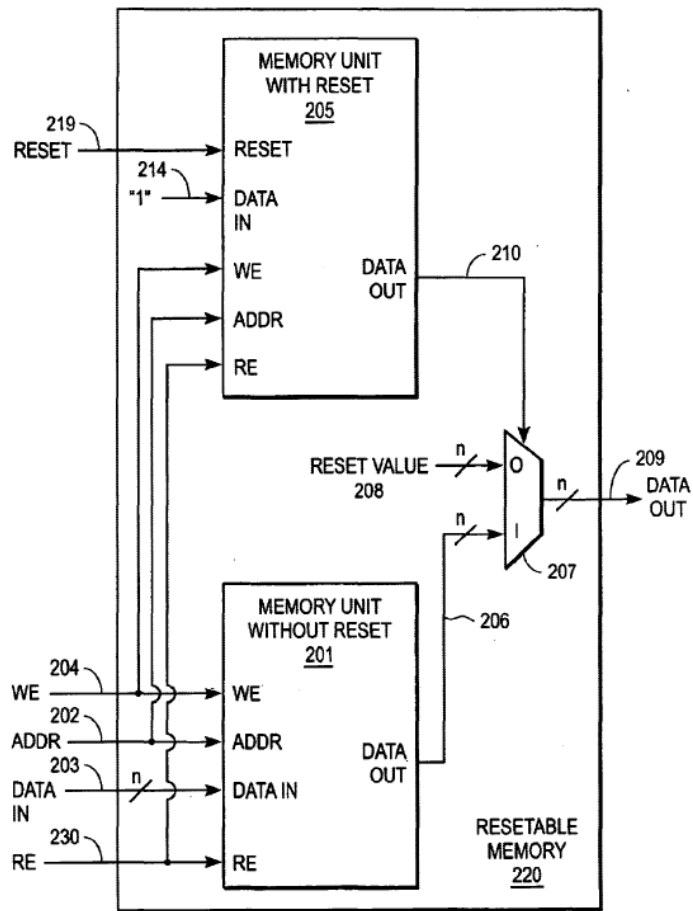


FIG. 2A

As depicted by Figure 2A, above, both memory unit without reset 201 and memory unit with reset 205 are connected to data out line 209 via multiplexor 207. Memory unit without reset 201 is larger in that it has a greater data width than memory unit with reset 205. *Id.* at 3:3–10. The '420 patent describes the smaller resettable memory having a cell word size less than the cell word size of the non-resettable memory. For example, the cell word size of the resettable memory is only one bit wide, so that the memory output from a cell is either a “1” or “0.” *Id.* at 3:8–10. As explained below, the purpose of the combination is that the smaller memory with reset 205

“cost effectively disguises the inability of the larger memory 201 to reset its cells.” *Id.* at 3:12–13.

Resettable memory 220 operates generally as follows: data is provided through data in line 203 to memory without reset 201, and is stored in a particular cell within the memory. *See id.* at Fig. 2A. The ’420 patent refers to data called from memory without reset 201 as “actual memory unit data output 206.” *Id.* at 3:26–30. Memory unit with reset 205 has a corresponding cell, in which a “1” from data in 214 is stored whenever write enable (WE) 204 of resettable memory 220 is activated. *Id.* at 4:1–3. The “1” from the memory unit with reset 205 instructs multiplexer 207 to output the actual memory unit data output 206 from memory 201 to data out line 209. *Id.* at 4:30–35. If memory unit with reset 205 is reset, a reset value, for example “0,” is stored in memory unit 205, output to data out 210, and received by Multiplexer 207. In this circumstance, reset value 208 is output to data out line 209. *Id.* at 3:51–54. If no new data has been written to the particular cell in memory unit without reset 201 since its last reset, the multiplexer will continue to output the reset value “0,”² which remains in its storage cell until WE 204 line is activated again. *Id.* at 4:1–3. Accordingly, when a new value is written to the particular cell in memory unit without reset 201, the “0” will be over written with a “1” and the new value will be output by multiplexer 207 to data out line 209. *Id.* at 4:30–35. The ’420 patent explains that “[i]n this manner, the circuit of FIG. 2[A] emulates the

² The reset may be a value besides “0,” for instance FIG. 2B discloses an embodiment in which “a reset value function circuit 230 may be inserted between (and coupled to) the reset value 208 input of the multiplexer 207 and the address input 202 of the resettable memory 220.” Ex. 1001, 4:67–5:3.

behavior of a memory unit having the storage capacity of memory unit 201 but also having reset capability.” *Id.* at 4:46–48.

In other words, the memory unit with reset 205 effectively replicates the behavior of a resettable memory by providing “0” or another reset value, if there has been a reset of a corresponding cell in memory unit with reset 205, unless and until new data is written to memory 201. *See id.* at 4:46–54.

In addition to the resettable memory circuit embodiment of Figure 2A discussed above, the ’420 patent describes a circuit design methodology inferring the use of a resettable memory from the behavioral level, or RTL (register-transfer level) description of the memory. *Id.* at 5:32–34. Rather than describe the specific circuit hardware, RTL level description describes the memory circuit in terms of its function, or operational flow, including the characteristic of the memory that it is resettable. *Id.* at 5:36–44. A software design tool, by way of example, which facilitates circuit design, infers from the RTL level description that a reset condition is being applied to at least one specific variable, and the software design tool can incorporate a resettable memory into the designer’s circuit design.³ *Id.* at 6:27–29; *see* Fig. 4.

C. Illustrative Claims

Of the challenged claims, the independent claims are 1 and 11. Each of dependent claims 2, 3, and 10 depends directly from claim 1. Each of

³ The ’420 patent states that “[t]he automatic inference can be accomplished, for example, by configuring the design tool to recognize from the operational flow of the circuit that: 1) some type of reset is being applied to the stored data values within the circuit; and 2) the stored data values are being changed to some type of reset value in response.” Ex. 1001, 6:22–27.

dependent claims 12, 13, and 20 depends directly from claim 11. Claims 1 and 11 illustrate the claimed subject matter and are reproduced below:

1. A method, comprising:
 - a) inferring the existence of a resetable memory from a behavioral or RTL level description of a semiconductor circuit; and
 - b) incorporating a resetable memory design into a design for said semiconductor circuit.

11. A machine readable medium having stored thereon a sequence of instructions which, when executed by a digital processing system, cause said system to perform a method, said method, comprising:
 - a) inferring the existence of a resetable memory from a behavioral or RTL level description of a semiconductor circuit; and
 - b) incorporating a resetable memory design into a design for said semiconductor circuit.

D. The Prior Art References Supporting Alleged Unpatentability

Petitioner relies upon the following prior art references:

Shand, U.S. Patent No. 6,192,447 B1 (issued Feb. 20, 2001)
("Shand '447," Ex. 1006).

Runaldue, U.S. Patent No. 5,067,110 (issued Nov. 19, 1991)
("Runaldue '110," Ex. 1007).

Nels Vander Zanden, *Synthesis of Memories From Behavioral HDLs*, IEEE (1994) ("Vander Zanden," Ex. 1003).

Peter Wohl & John Waicukauski, *Using Verilog Simulation Libraries For ATPG*, IEEE (1999) ("Wohl," Ex. 1004).

XILINX SYNTHESIS TECHNOLOGY (XST) USER GUIDE, VERSION 3.1I, Xilinx, Inc. (2000) ("XST," Ex. 1005).

E. The Pending Grounds of Unpatentability

Reference(s)	Basis	Claims challenged
Vander Zanden (Ex. 1003)	§ 102	1, 2, 10–12, and 20
Wohl (Ex. 1004)	§ 102	1, 2, 10–12, and 20
Vander Zanden and Shand (Ex. 1006)	§ 103	1–3, 10–13, and 20
Vander Zanden and Runaldue (Ex. 1007)	§ 103	1–3, 10–13, and 20

Petitioner supports its challenge with a Declaration by Mr. Ewald Detjens A.B., M.S. (“Detjens Decl.,” Ex. 1002).

II. CLAIM CONSTRUCTION

A. Legal Standard

Consistent with the statute and the legislative history of the Leahy-Smith America Invents Act (“AIA”), Public Law 112-29, 125 Stat. 284 (September 16, 2011), the Board will interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012); 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claims are to be given their broadest reasonable interpretation consistent with the specification, and the claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004), *see In re Cuozzo Speed Techs., LLC*, 778 F.3d 1271, 1279–83 (Fed. Cir. 2015). Also, we must be careful not to read a particular embodiment appearing in the written description into the claim, if the claim language is broader than the embodiment. *See In re Van Geuns*,

988 F.2d 1181, 1184 (Fed. Cir. 1993) (“[L]imitations are not to be read into the claims from the specification.”).

B. Overview of the Parties’ Positions

1. Inferring and Incorporating

In the Decision to Institute, we provided an interpretation for “inferring” in accordance with its plain meaning, including: concluding, deciding, deducing, deriving, extrapolating, gathering, judging, making out, reasoning, understanding, and recognizing. Inst. Dec. 9–10. We did not provide a construction for any other terms.

Patent Owner’s position is that the word “deducing” comes closer to the meaning of “inferring” than the words “recognizing” or “identifying” as proposed by Petitioner. PO Resp. 24, *see also* Pet. 14. Our construction includes from its plain meaning, a variety of words (including: deducing recognizing, and identifying) that, depending on context, provide additional understanding of the word “inferring.” Inst. Dec. 9–10. A plain meaning of the word “incorporating” is “to unite or work into something already existent so as to form an indistinguishable whole.” *Incorporate*, Merriam-Webster Online Dictionary, <http://www.merriam-webster.com/dictionary/incorporate> (last visited May 28, 2015).

For these words, we do not consider the proffered constructions to provide any clarity over the term itself. Consequently, we simply are not persuaded by either of the parties contentions and interpretations that under the broadest reasonable interpretation, in the context of the Specification and claims, that these words should be construed with respect to only the particular definitions or meanings ascribed to them by either party.

2. *Memory*

Based on the parties' positions and arguments in the Petition, Patent Owner's Response, Petitioner's Reply, as well as at the oral hearing, with respect to Vander Zanden, the base reference in each ground, we determine that the word "memory" should be construed explicitly.

Neither party provides a construction for "memory," however, the '420 patent describes a "memory unit" in the Background section of the Specification as,

having a plurality of storage cells (or simply, "cells"). Associated with each cell is a unique address that provides access to the location of a particular storage cell. Each storage cell has the capacity to store "n" bits (where n is an integer greater than or equal to one). The n bits may be collectively referred to as a word of data.

Ex. 1001, 1:15–20. The '420 patent explains that for a memory, from an input perspective, a word of data (i.e. "n" bits of data) is written to a specific cell address in the memory unit, and from an output perspective, the word of data is retrieved from a provided cell address and "the word of data is presented at the data output bus." *Id.* at 21–38. Thus, the '420 patent provides certain structural and functional characteristics that provide a basis for defining "memory." Moreover, a person of ordinary skill in the art at the time of the invention would have understood based on these characteristics that a memory unit in the '420 patent either presents a word of data from a specified address at the output in a "read" command, or overwrites old data with a new word of data at a specified address in a "write" command. Hutchings Decl. ¶ 21. ("One or more inputs control whether the current contents of a memory word should be presented at the output (referred to as

a ‘read’) or whether the current contents should be overwritten and updated to contain a new value (referred to as a ‘write’).”) Based on the Specification and evidence before us, we construe “memory” as a device for storing data having a plurality of cells, each cell having a unique address for storing data, where data is written to a cell during a write function, and, during a read function data is retrieved from a cell and presented at a memory output.

3. *Resettable Memory*

Petitioner provides contentions regarding the broadest reasonable construction of “resettable memory.” Pet. 10–14. Specifically, Petitioner contends that because the ’420 patent describes that the memory unit’s cells are not actually reset, but only appear to be reset to downstream components, “resettable memory” is “a memory unit whose *output value(s)* can be cleared to a reset value, e.g., ‘0’, the memory unit comprising one or more storage cells.” *Id.* at 11 (emphasis added). Patent Owner argues that Petitioner’s construction is overly broad, and that the Specification of the ’420 patent repeatedly describes that a “resettable memory” “must output a reset value for a given memory cell (following a reset) *until new data is written into that cell.*” PO Resp. 12–13 (emphasis added). Petitioner counters that the construction of this term should not be conditioned on future data writes. Reply 6–7.

A claim construction analysis begins with, and is centered on, the claim language itself. *See Interactive Gift Express, Inc. v. Compuserve, Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001). Nevertheless, claims must be read in view of the specification of which they are a part. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007), *Phillips v. AWH Corp.*, 415 F.3d

1303, 1315, (Fed.Cir. 2005) (en banc). The specification is the single best guide to the meaning of a disputed term. *Id.* Turning to the language of claim 1, the claimed method includes two steps “inferring the existence of a resettable memory,” and “incorporating a resettable memory design,” but the claim language does not, in any detail, explicate what the “resettable memory” itself, is, or does. Ex. 1001, claim 1.

The Specification of the ’420 patent states from a structural standpoint that “a resettable memory is described that includes a memory without reset capability.” Ex. 1001, 2:51–52. The purpose of including a “memory without reset” in the overall resettable memory, the Specification explains, is to be less expensive and less complex than an actual “memory with reset” because “often, the integration of circuitry for resetting the cell word values of the memory unit **101** is too expensive and/or complicated to implement . . . having noticeably slower performance (and that consumes more silicon surface area).” *Id.* at 1:61–2:6. The “memory without reset” portion of the overall resettable memory is smaller and more efficient, but unable to reset its memory cells. *Id.* at 3:12–13.

As discussed in further detail below, we are not apprised of a sufficient reason to read “memory without reset” into the claims. Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim. *Superguide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004). Nevertheless, as described explicitly in the ’420 Specification, when reset, the overall “resettable memory” must be able to output a reset value, despite retention of what is

essentially stored, old data in a particular memory cell of the resettable memory. *See* Ex. 1001, 3:11–23.

Patent Owner alleges that the Specification consistently discloses that “a ‘resettable memory’ must output a reset value for a given memory cell (following a reset) until new data is written into that cell.” PO Resp. 13–17 (citing Ex. 1001, 3:40–58, 4:17–21, 47–54, 7:12–31, Figs. 2A, 2B, 3, 5, 6; Hutchings Decl. ¶¶ 31, 36–40). Dr. Hutchings testifies that a person of ordinary skill in the art reading the ’420 patent “would understand that one defining characteristic of a resettable memory is that, following a reset, it must output a reset value for a given memory cell until new data is written into that cell.” Hutchings Decl. ¶ 31. It is further stated by Dr. Hutchings that in observing the operating flow of the invention from Figure 3 of the ’420 patent, the implementation of the described invention relies explicitly on the methodology that “*a reset is asserted 301. This causes the reset value 208 (in FIGS. 2A and 2B) to be provided 302 as the effective memory cell output-until the cell is written to.*” *Id.* ¶ 35 (citing Ex. 1001, 4:56–61).

Our review of the Specification indicates that the “resettable memory” is consistently defined as “reset” in each embodiment to output the reset value (as opposed to the stored, old, data in the memory without reset) until a new data value is written in a particular memory cell. Ex. 1001, 3:50–56 (“That is, after the resettable memory **220** has been ‘reset’, any attempt to read a data word from a particular cell within the memory unit without reset **201** will produce the reset value **208** at the memory unit data output **209**. This functional behavior continues for each cell until a particular cell is written to.”) We are mindful that we should not ordinarily rely on the preferred embodiments alone as representing the entire scope of the claimed

invention. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1370 (Fed. Cir. 2002); *see also Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1344 (Fed. Cir. 2001) (emphasizing that the scope of a claim term often covers more than the embodiments disclosed in the specification and that a patent applicant need not describe “in the specification every conceivable and possible future embodiment of his invention”). However, Patent Owner’s evidence from the ’420 patent unambiguously describes how all the embodiments include this functionality. To construe this term as Petitioner proposes as simply “a memory unit whose output value(s) can be cleared to a reset value, e.g., ‘0’,” ignores the explicit behavior and the methodology of a “resettable memory” as described in the Specification. Pet. 11. Moreover, Petitioner’s proposed construction relies in part on a statement from the Background of the ’420 patent explaining that in the context of known resettable memories “[a] reset function effectively ‘clears’ the memory unit’s cell word values to some ‘reset’ value.” *Id.* (citing Ex. 1001, 1:59–60.) This statement, however, relates to conventionally clearing the memory unit’s cell value, not the “effective” output discussed in context of the inventive resettable memory described later in the detailed description. *See* Ex. 1001, 3:24–26.

Petitioner’s apparent position that the word “effectively” ties this phrase discussing known circuitry for resetting cell word values in a memory unit, to the “‘effective’ memory unit output as observed by the downstream circuitry,” discussed later in the Specification is not persuasive. *Id.* at 3:32–34. Indeed, supported as it is by the Background of the invention, Petitioner’s incorrect construction would encompass the example described in the Background section of the Specification, i.e. the known method using

a resettable flip-flop for clearing each storage cell in the memory. *See id.* at 1:63–2:6. This is not a reasonable interpretation owing to the detailed description and more specific characterization of the described “resettable memory,” contrasted against the known resettable memory described in the Background section of the ’420 patent. Thus, we are persuaded that one of ordinary skill in the art, would understand from the Specification of the ’420 patent that a “resettable memory,” as claimed, is a memory, as construed above, that outputs a reset value until new data is written into the memory.

4. *Resettable Memory Design*

Claims 1 and 11, in paragraphs b), both recite a “resettable memory design.” In the context of both the method recited in claim 1, and the machine readable medium recited in claim 11, paragraph b) reads:

- b) incorporating a resettable memory design into a design for said semiconductor circuit.

On its face, the predicate in this clause uses the word “design” in the context of a circuit, i.e. a semiconductor circuit design. Reviewing the Specification, the term “design” is similarly used in almost every instance to refer to a circuit or semiconductor circuit. For example, the Specification explains the benefits of implementing the resettable memory in a circuit design, where:

[a] further utility of the approaches discussed above is the ease at which a memory having reset may be incorporated into a *designer’s circuit design* . . . [f]or example, *semiconductor circuits* are typically designed with a particular semiconductor manufacturing process (i.e., a “foundry”) in mind. Usually, the foundry supplies models of basic building blocks (e.g., logic gates, memory units, etc.) from which a *semiconductor chip design* can be constructed.

Ex. 1001, 5:9–18 (emphasis added).

From the plain meaning of the claims and the Specification, we understand that the word “design” in the context of “resetable memory” essentially means a circuit design. Moreover, understanding that paragraph b) in claims 1 and 11 is the implementation step relative to the preceding “inferring” step in paragraph a), this implementation step explains *how* the “resetable memory” is to be used in a semiconductor circuit. Accordingly, the broadest reasonable interpretation of “resetable memory design” in light of the Specification is a resetable memory as defined previously, implemented in a circuit design.

III. ANALYSIS

A. Alleged Anticipation of Claims 1–2, 10–12, and 20 by Vander Zanden

For the reasons given below, despite the arguments provided in the Petition, and the evidence cited therein, Petitioner has not shown, by a preponderance of the evidence, that each of claims 1–2, 10–12, and 20 are unpatentable as anticipated by Vander Zanden.

1. Vander Zanden

Vander Zanden discloses a method of creating descriptions of small memory designs “such as multi-port register files” for use in computer emulation—synthesis—that differs from conventional techniques. Ex. 1003, 71. The method synthesizes a description of a memory, specifically a two-dimensional array *regFile*, apart from other logic and datapath elements as a behavioral description. *Id.* at 72. “This allows the designer to include the behavioral description of the memory with the rest of the HDL [Hardware Description Language] code, yet offers multiple architectural

implementations for the memory without additional effort for the designer.”

Id. at 71. Figure 3 of Vander Zanden is reproduced below:

```
architecture regfilesyn_A of regfilesyn is
begin
process(clk,rst)
subtype addrType is integer range 0 to 15;
type regFileType is array (addrType) of integer;
variable regFile: regFileType;
begin
if rst='1' then
out1 <= (others => '0');
elsif clk'event and clk='1' then
if s2='1' then
out1 <= regFile(addr1) + regFile(addr2);
else
out1 <= regFile(addr3);
end if;
if s1='1' then
regFile(writeAddr) := dataIn;
end if;
end if;
end process;
end regfilesyn_A;
```

Figure 3: VHDL Description

Figure 3 of Vander Zanden illustrates an HDL model for a memory having an if-else statement that includes on one hand a data out, “out1” result of “0,” and on the other hand, a data out result of cell addresses, “addr1, 2, 3.” Ex. 1003, 73.

Figure 4 of Vander Zanden, reproduced below, discloses a particular datapath circuit design based on the HDL description of Figure 3 including two registers, an adder (ADD1), and a multiplexor leading flip-flop DFF 6 to the data out line OUT1. *Id.*

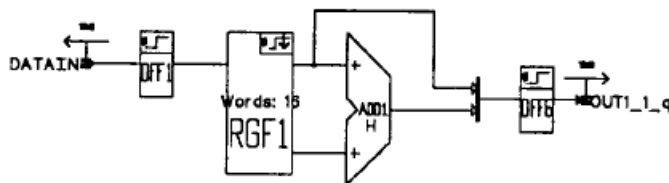


Figure 4: Datapath Design Containing Register File Cell

Figure 4 of Vander Zanden illustrates a datapath design containing register file cell.

According to Vander Zanden, the use of such a memory synthesis technique and datapath design reduces the size of the circuit design as well as operational delay. *Id.* at 74.

2. Discussion

i. Claims 1–2, and 10

Petitioner argues that Vander Zanden anticipates claim 1, a method claim, because it discloses not only “inferring a resettable memory” but also “incorporating a resettable memory design into a design for said semiconductor circuit.” Pet. 15–16. Petitioner states that “[a] POSA would understand the synthesis process described by Vander Zanden to teach inferring the existence of a memory by the presence of a ‘two-dimensional array’ within the behavioral description.” *Id.* at 16 (citing Detjens Decl. ¶ 36(a)). Petitioner asserts that a two-dimensional array of bits, such as *regFile* disclosed by the VHDL model in Vander Zanden’s Figure 3, constitutes a memory, and that resettable flip-flop DFF6 on the data out line as shown in the circuit design at Figure 4 makes the memory resettable. *Id.* (citing Ex. 1003, 72).

Patent Owner argues that Vander Zanden does not disclose “a resettable memory design” as claimed “because, from the perspective of the downstream circuitry, the circuit shown in Vander Zanden Figure 4 is not a memory. This is due to the presence of an adder in the circuit.” PO Resp. 26. In support, Patent Owner cites to Petitioner’s Declarant, Mr. Detjens’, deposition testimony:

Q. Would the average engineer understand [the circuit with an adder] to be a memory?

...

THE WITNESS: The average engineer would not expect an adder to be at that place in a memory.

Id. (citing Ex. 2010, 41:3–16). Patent Owner alleges that Mr. Detjens, as well as Patent Owner’s Declarant, Dr. Hutchings, agree that the downstream circuitry from Vander Zanden’s output flip-flop DFF6 would, at times, see the sum of two memory locations due to adder ADD1, and not an actual memory value from the memory locations in RGF1. *Id.* at 28. Patent Owner contends that because of this a designer of ordinary skill in the art “could not (and would not) use the Vander Zanden Figure 4 circuit as a memory because in one state the circuit would output values [from ADD1] completely different from either a reset value or a value stored in the register file RGF1. *Id.* at 29.

Petitioner’s Declarant, Mr. Detjens testifies that at the time of the filing of the patent, those of ordinary skill in the art would have understood Vander Zanden to disclose a memory, specifically by the steps of:

[a]nalyzing the extracted logic equations to determine the characteristics, i.e., requirements, of the memory described in the behavioral description, e.g., whether the memory is written synchronously or asynchronously and how many read and write ports are required for the memory. (*Id.*, Step 4.) A POSA would have understood another characteristic to be whether the memory is resettable.

Ex. 1002 ¶ 36.e. Mr. Detjens states that one of ordinary skill in the art would consider Figures 3 and 4 in Vander Zanden to disclose a memory, even though there is an adder on one of the outputs of the circuit because the

“ADDER only affects the output of the circuit in one mode of the circuit, when the multiplexer selects the ADDER path.” Ex. 1024 ¶¶ 23–24 (citing Ex. 1003, 74, Fig. 4). In a mode of the circuit where the multiplexer does not select the ADDER, Mr. Detjens alleges that “a POSA would have understood the circuit of Fig. 4 to operate as memory, with the output value of RGF1 appearing on the output, unless the reset signal, ‘rst,’ has been applied.” *Id.* at 24. Thus, Mr. Detjens alleges that on one hand the circuit discloses a memory with a reset function, and on the other hand it discloses a memory output operated upon by ADDER.

Petitioner’s evidence is persuasive that a person of ordinary skill in the art would consider the circuit shown in Vander Zanden’s Figure 4 to operate as a memory, as we have construed the term, with a reset capability. We construed “memory” as a device for storing data having a plurality of cells, each cell having a unique address for storing data, where data is written to a cell during a write function, and, during a read function data is retrieved from a cell and presented at a memory output. *See* section II.B.2. Although the additional circuitry of the ADDER is provided to perform an operation on values output from RGF1, in the mode where the ADDER is not selected, OUT1 will output a value from a register in RGF1, unless a reset signal is applied, as a memory would in accordance with our claim construction. At least in one state downstream circuitry would recognize the circuit of Figure 4 as a memory, thus “inferring” the circuit to be a memory with reset capability. Patent Owner’s argument that this does not occur when the ADDER mode is in effect, does not explain why the portion of the circuit without the ADDER circuitry does not operate and would not be recognized, as a memory having a reset function.

Patent Owner further asserts that Vander Zanden does not anticipate the claimed subject matter because it does not disclose a “resettable memory,” as properly construed, because Vander Zanden does not keep, i.e. remember, that the memory has been reset. PO Resp. 29–33. Patent Owner contends that the code in Vander Zanden’s Figure 3 includes well known “if then” statements which show that only when the reset signal is high, e.g. $rst=1$, is OUT1 a reset value “0.” Otherwise, when the signal goes low, “the output of the circuit (out1) is assigned the value stored in a particular memory address (see line 14) or the sum of two values stored in different memory addresses (*see* line 12).” PO Resp. 32 (citing Ex. 2011 ¶ 59).

Based on our claim construction, we are persuaded that Vander Zanden does not disclose a “resettable memory” as recited in independent claim 1. We determined that a “resettable memory” means a memory that outputs a reset value until new data is written into the memory. *See* section II.B.3. Vander Zanden’s “if then” statement in the code shown in Figure 3 outputs a reset value “0” only when the reset signal is high, in all other modes it outputs either a value from RGF1 or added values from RGF1. *See* Ex. 1003, Fig. 3; *see also* PO Resp. 32. In other words OUT1 does not keep, or remember, the reset value until new data is written to RGF1. We find Patent Owner’s position persuasive that the resettable flip-flop DFF6 on the output line of the circuit as described in Vander Zanden’s Figure 3, and shown in Figure 4, does not render the registers at RGF1 a “resettable memory” as properly construed because it fails to maintain OUT1 at a reset value until new data is written to a cell.

Petitioner’s argument that no temporal limitation should be read into the claim is unpersuasive because, as discussed above in section II.B.3, the

'420 patent expressly differentiates the “reset” functionality of the described “resettable memory” from known resettable memories where the described, and claimed methodology in each embodiment, “causes the reset value **208** to be provided **302** as the effective memory cell output—until the cell has been written to.” Ex. 1001, 4:56–58.

Vander Zanden does not disclose a “resettable memory design” for similar reasons as set forth above with respect to “resettable memory.” We are persuaded that the resettable flip-flop DFF 6 on the output line as shown in Figure 4 does not disclose a “restable memory design” as called for in the claims because Petitioner does not explain how the circuit design in Figure 4 implements the retention of a reset value until new data is written to the cell, where it only toggles between the reset mode, ADDER mode and mode which returns a value from RGF1.

For the reasons provided above, Petitioner has not established by a preponderance of the evidence, the unpatentability of claim 1 as anticipated by Vander Zanden under 35 U.S.C. § 102(b) because each and every element as set forth in the claim is not found, either expressly or inherently described, in Vander Zanden in as complete detail as is contained in claim 1. *Scripps Clinic & Research Found. v. Genentech, Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991) (“There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention.”).

Because the remaining dependent claims 2 and 10 depend directly from claim 1, and necessarily include all the limitations of claim 1, these claims also are not anticipated by Vander Zanden.

ii. Claims 11–12, and 20

Independent claim 11 is for a “machine readable medium” with instructions to carry out the method with exactly the same limitations in paragraphs a) and b) as discussed above with respect to claim 1. For the same reasons as set forth above, claim 11 and dependent claims 12 and 20 are also not anticipated by Vander Zanden.

B. Alleged Obviousness of Claims 1–3, 10–13, and 20 over Vander Zanden and Shand

For the reasons given below Petitioner has shown, by a preponderance of the evidence, that each of claims 1–3, 10–13, and 20 are unpatentable based on the combination of Vander Zanden and Shand.

1. Overview of Shand

Shand is directed to a method, and specific circuit designs, for resetting memories. Ex. 1006, 1:5–14. Figure 1, reproduced below, illustrates a circuit diagram for a resettable memory according to Shand.

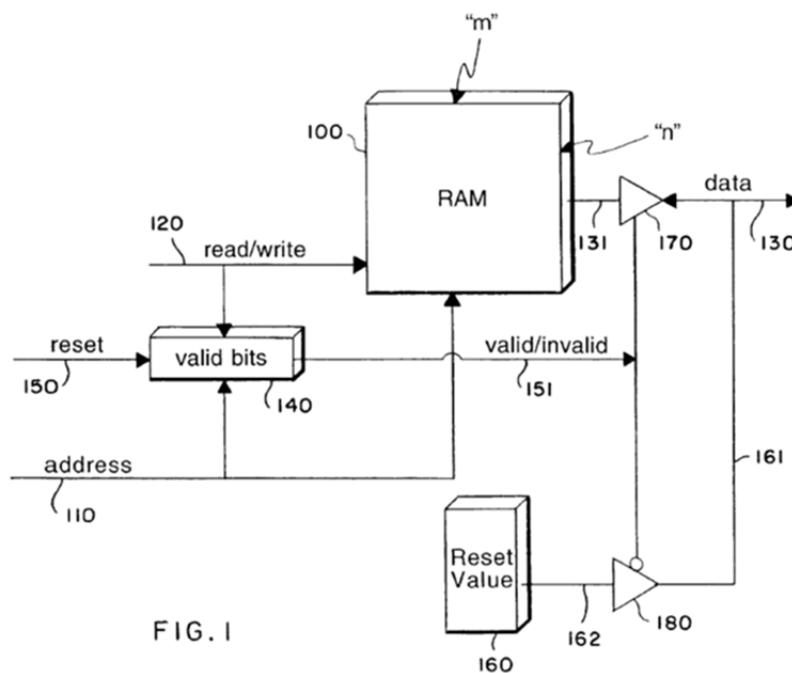


FIG. 1

Shand discloses, for example in Figure 1, above, non-resettable RAM 100 and reset register 140 with corresponding bits “m” to respective memory locations in RAM 100. *Id.* at 2:31–66. When a reset register bit value is valid for a particular memory location, “the reset value from register [160] is produced on line 130 via lines 162 and 161, instead of the actual data stored at the addresses memory location.” *Id.* at 2:64-66. In this way, Shand explains, a reset value is maintained until “[a] write to a particular memory location will set the corresponding bit of register 140 to, for example, a logical one, and the corresponding memory location after the write is now valid.” *Id.* at 43–46.

2. Discussion

Patent Owner argues that Shand does not remedy Vander Zanden’s failure to teach the step of “inferring the existence of a resettable memory” as recited in claims 1 and 13, and further, that one of ordinary skill in the art would not combine these references because Shand discloses a structurally and functionally different circuit from Vander Zanden. PO Resp. 53–57.

As discussed previously in section III.A.2.i, with respect to the anticipation challenge to Vander Zanden, we determined that Vander Zanden discloses inferring a “memory” in accordance with our claim construction, but not a “resettable memory.” This is because Vander Zanden’s Figure 4 discloses a memory circuit design including a reset function, however, the evidence does not show that the memory maintains, or remembers the reset value for output, OUT1, until new data is written to RGF1 as required by our claim construction. *See* Ex. 1003, Figs. 3–4.

In the case of obviousness, Petitioner relies upon Vander Zanden’s derivation of a memory circuit from Verilog behavioral description to

disclose the step of inferring the existence of a memory, and turns to Shand for disclosure of a “resetable memory” and a “resetable memory design” for incorporation into a semiconductor circuit. Pet. 31. Petitioner asserts that one of ordinary skill in the art would have combined Shand with Vander Zanden in order to reduce the size of the circuit design. *Id.* at 32 (citing Ex. 1002 ¶ 68).

Patent Owner argues specifically that Petitioner’s Declarant, Mr. Detjens, admitted that one of ordinary skill in the art would not replace the memory in Vander Zanden with the circuit described in Shand. PO Resp. 55. This argument mischaracterizes Mr. Detjens testimony as well as the question. The question asked Mr. Detjens if he could identify “what *memory* in Vander Zanden you would replace with the Shand memory?” Ex. 2010 84:2–3 (emphasis added). Read in context, Mr. Detjens’ initial answer “No” differentiates between replacing the “memory” and replacing the “resetable memory.” *See id.* at 84:1–20. Mr. Detjens continued on, and answered the question with further specificity, stating that “for a *resetable memory* that is created through the process given in the Vander Zanden paper, you would replace it with the memory in the Shand patent.” *Id.* at 84:18–20 (emphasis added). Thus, we do not find Patent Owner’s argument on this point to be persuasive.

Patent Owner further asserts that Shand’s resetable memory is functionally different and one of ordinary skill in the art would not utilize Shand’s resetable memory with Vander Zanden because it “would render the circuit inoperable (*i.e.*, the synthesized circuit in Vander Zanden Figure 4 would no longer match the HDL and it would not work as the designer intended).” PO Resp. 57 (citing *McGinley v. Franklin Sports, Inc.*, 262 F.3d

1339, 1354 (Fed. Cir. 2001)). Petitioner replies that “A POSA knew how to describe a resetable memory in behavioral or RTL level terms, and how to recognize a resetable memory in such a description.” Reply 2–3 (citing Ex. 1024 ¶¶ 10–15; Ex. 1020 at 17–18, 27–28, 75–77, 84–85, 91–98).

Petitioner’s position, and Dr. Detjens’ testimony, are persuasive. Neither Patent Owner’s argument that Shand fails to disclose the inferring step, nor the testimony provided in Dr. Hutchings’s Declaration alleging that Shand discloses only resetable memory circuits and not *inferring* a memory with reset, explains why it was not within the ordinary skill of one in the art to have modified the respective underlying HDL code, for example as shown in Vander Zanden’s Figure 3, to include code defining the respective resetable memory circuit such as disclosed in Shand. *See* PO Resp. 57, *see also* Ex. 2011 ¶¶ 85–88. As discussed above with respect to anticipation, we are persuaded that Vander Zanden discloses the “inferring” step for a memory as recited in independent claims 1 and 13, and that it would have been within the abilities of a person of ordinary skill in the art to combine Shand’s resetable memory circuit design with Vander Zanden and consequently modify the HDL code to address the functional changes imparted by the implementation of a different resetable memory in such a combination.

Patent Owner does not address the specific limitations of dependent claims 2, 3, 10, 12, 13, and 20 but relies, for each of claims 1–3, 10–13 and 20, upon its erroneous analysis with respect to the combination of Vander Zanden and Shand. *See* Prelim Resp. 47–49, *see also* PO Resp. 52–57. We therefore conclude that a preponderance of the evidence demonstrates that

claims 1–3, 10–13 and 20 are unpatentable based on the combination of Vander Zanden and Shand.

C. Alleged Obviousness of Claims 1–3, 10–13, and 20 over Vander Zanden and Runaldue

1. Overview of Runaldue

Runaldue discloses a memory circuit with a zero detect logic to determine if a row of a memory array is to be treated as reset to a zero state, or preserved in a non-zero state according to corresponding tag-memory cells. Ex. 1007, 2:1–16. Runaldue explains that, “[t]he tag-memory cells are resettable to a zero state to indicate that the associated row of the memory array is to be treated as all being in the zero state. This is to be done even though the actual contents of the memory are not all zeros.” *Id.* at 2:11–16.

2. Discussion

Patent Owner states that Petitioner’s obviousness arguments for the combination of Vander Zanden and Runaldue are based on the same “incorrect premise” as Vander Zanden and Shand and “are largely identical to those made with respect to Shand . . . and fail for the same reasons described above.” PO Resp. 58. Patent Owner’s argument that Vander Zanden does not infer a resettable memory is, as discussed above with respect to Shand, incorrect. However, because we construed the term “resettable memory” and “resettable memory design” differently than Petitioner proposed, the question remains whether Runaldue meets both these further claim limitations of a “resettable memory” and a “resettable memory design” as properly construed.

Runaldue discloses in the Background of the Invention, that a “global reset” function is understood as “a condition in which every memory

element is reset to a predefined logical zero state.” Ex. 1007, 1:19–21. In the Summary of the Invention, Runaldue explains that in a memory array, each row of memory cells will have a “tag-memory cell[]” that indicates whether the row has a non-zero, or a zero, state. *Id.* at 2:1–7. Runaldue further discloses that “[t]he tag-memory cells are resettable to a zero state to indicate that the associated row of the memory array is to be treated as all being in the zero state. This is to be done even though the actual contents of the memory are not all zeros.” *Id.* at 11–16. What we cannot determine from our review of Runaldue is that the tag-memory maintains a zero state until new data is written to the memory. Runaldue is silent as to such a requirement. We construed “resettable memory” as a memory that outputs a reset value until new data is written into the memory. Runaldue discloses a memory that outputs a reset value, for example a zero state, but there is no disclosure that the zero state is maintained, or “remembered” until new data is written to the memory. Therefore, even if combined with Vander Zanden, Runaldue fails to correct the underlying deficiency of Vander Zanden. Accordingly, Petitioner has failed to show by a preponderance of the evidence that the combination of Vander Zanden and Runaldue meets all the limitations of independent claims 1 and 11. Because the remaining dependent claims 2, 3, 10, 12, 13 and 20 depend directly from claim 1 or claim 11, and necessarily include all the limitations of their respective dependent claims, these claims also are not rendered obvious by Vander Zanden and Runaldue.

D. Alleged Anticipation of Claims 1–2, 10–12, and 20 by Wohl

For the reasons given below, despite the arguments provided in the Petition, and the evidence cited therein, Petitioner has not shown, by a

preponderance of the evidence, that each of claims 1–2, 10–12, and 20 are unpatentable as anticipated by Wohl.

1. Overview of Wohl

Wohl describes an improvement in integrated circuit design flow that more efficiently uses a single Verilog simulation library for both simulation and ATPG (“Automatic Test Pattern Generator”) model building. Ex. 1004, 1011. Wohl explains that using a single library in the netlist reader and model builder of an ATPG tool eliminates the necessity for coding and verifying a separate ATPG library, and additionally simplifies debugging test problems. *Id.*

Wohl specifically discloses an ATPG model builder for converting a behavioral Verilog description, for example of a RAM including a reset line and read/write ports, into a resulting ATPG model test pattern generator. *Id.* at 1017, Figs. 6–7. Wohl discusses a methodology which rewrites, or recodes, the Verilog RAM description into a simplified form that is sufficiently simple for automatic processing and displays the resulting ATPG RAM model in a schematic viewer. *Id.* By way of example, the RAM ATPG model shown in Wohl’s Figure 7 below, appears as a test pattern generator simulated by the behavioral Verilog description shown in Figure 6.

Figure 6 of Wohl, reproduced below, is a RAM described in behavioral Verilog having a reset line. Ex. 1004, 1017.

```

module withram(reset, r,w, a, d1,d2);
input reset, r,w;
input [3:0] a;
input [7:0] d1;
output [7:0] d2;
reg [7:0] mymem [15:0], d2;
integer i;
always @ reset if (reset)
for (i=0; i<16; i=i+1) mymem[i] <= 0;
always @ (posedge w) mymem[a] <= d1;
always @ r if (r) d2 <= mymem[a];
else d2 <= 0; // read_off is 0
endmodule

```

Figure 6. Simple RAM with reset, write and read port.

Wohl’s Verilog description, shown above in Figure 6, results in the “unambiguous ATPG model of Figure 7,” displayed in the block diagram reproduced below.

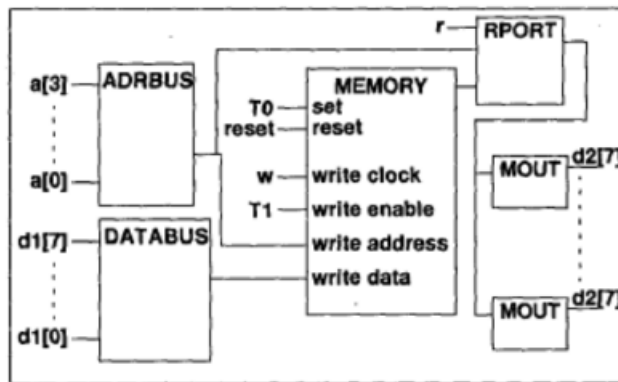


Figure 7. ATPG model of the RAM in Figure 6.

Wohl’s Figure 7, illustrated above, is described as “the ATPG model built as displayed by the schematic viewer.” *Id.*

2. Discussion

i. Claims 1–2 and 10

Petitioner argues that Wohl discloses each limitation of claim 1 including a method for converting a behavioral Verilog description of RAM with resettable memory into a gate-level description of an ATPG model of a circuit design including resettable memory. Pet. 19–20 (citing Ex. 1004,

1017, Figs 6–7). Petitioner specifically asserts that because Wohl teaches a behavioral description of a RAM with a reset line, and an ATPG model builder that converts the behavioral description into an ATPG model “[a] POSA would understand this conversion to require inferring, or recognizing, the existence of a resettable memory from the behavioral Verilog description” as called for in paragraph a) of claim 1. Pet. 20 (citing Ex. 1002 ¶¶ 46–47). Also Petitioner contends, Wohl’s ATPG model in Figure 7 would be understood by a person of ordinary skill in the art as a design for a semiconductor circuit having a resettable memory as recited in paragraph b) of claim 1. *Id.* at 20–21 (citing Ex. 1002 ¶ 48).

Patent Owner makes three arguments as to why Wohl does not anticipate the challenged claims. PO Resp. 40. First, Patent Owner argues that Wohl does not disclose a “resettable memory design” as claimed because Wohl discloses only a memory with intrinsic reset, i.e. a resettable memory. *Id.* at 40–43. Second, Patent Owner argues that the ATPG model in Figure 7 does not match the functionality shown in the code in Figure 6, and third, that Wohl does not disclose a semiconductor design. *Id.* at 44–49.

With respect to whether Wohl’s ATPG model in Figure 7 discloses a “resettable memory design” in accordance with the proper claim construction, we determine that it does not. Wohl explains that the ATPG model is part of the development and “typical design flow of integrated circuits,” but provides no explanation of how to derive a memory circuit design, that could be incorporated into a semiconductor circuit, from the design flow. Ex. 1004, 1011. Clearly, an ATPG test model is a schematic representation of the behavioral Verilog description, however, it is not clear from Wohl that one of ordinary skill in the art would understand the ATPG

model to be representative of a circuit design implementing, for example, the memory function described by the behavioral Verilog in Wohl.

Petitioner states in its Reply that the '420 patent does not limit “‘semiconductor circuit’ designs to final designs that can be used, without alteration or optimization, to directly manufacture semiconductor circuits in silicon chips.” Reply 10. Petitioner argues, essentially, that a gate-level ATPG model, is sufficient to disclose a memory circuit design as claimed. *Id.* This argument misses the mark however, because it is unsupported by reliance on any credible evidence, and does not explain where, or how, Wohl’s gate level ATPG model discloses a “resetable memory circuit design,” as properly construed, that can be incorporated into a semiconductor circuit. *See id.* To establish anticipation, every element and limitation of the claimed invention must be found in a single prior art reference, arranged as in the claim. *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001).

Petitioner relies upon Mr. Detjens’ testimony alleging that a person of ordinary skill in the art would understand that Wohl teaches “incorporating a resetable memory design into a semiconductor circuit design.” Pet. 21 (citing Ex. 1002 ¶ 48.) Mr. Detjens alleges that “the inference of the memory described in Figure 6’s behavioral Verilog leads to the incorporation of a resettable memory into a gate-level ATPG model description of the circuit, as clearly illustrated in Figure 7.” Ex. 1002 ¶ 48. Mr. Detjens’ Declaration, however, is similarly deficient with respect to any explanation or opinion regarding the understanding of a person of ordinary skill as to how or why the memory block shown in Wohl’s Figure 7 is representative of a circuit. *Id.* The Declaration concludes that “A POSA

would have understood Figure 6 of Wohl as describing the operational flow of a particular circuit” without explaining how the operational flow shown in Figure 7 and code statements from Figures 6 details any circuit structure that could be incorporated into a semiconductor circuit. *Id.* ¶ 49. Indeed, when asked during his deposition to explain what it means to be an ATPG model of a memory, Mr. Detjens testified that “[t]he ATPG model is used to create the test vectors that are part of the design of the semiconductor device.” Ex. 2010, 64. Mr. Detjens’ testimony indicates that test vectors are a functional description necessary in the circuit design process, but, when questioned on this point, Mr. Detjens did not specify that the ATPG model in Figure 7 alone was sufficient to indicate to one of skill in the art a particular circuit or circuit design structure:

A: When you walk up to a foundry and say make this chip, you don’t hand them just a netlist of library elements and say manufacture this. You have to hand them a set of test vectors at the same time that corresponds to that. If you don’t, they won’t manufacture it for you.

Q: So are you telling me that the test vectors, in part, define the circuitry that goes onto the chip?

A: It defines the functionality of the circuitry on the chip.

Id.

We are not persuaded that Petitioner has shown by a preponderance of the evidence that the ATPG test model, as a representation of a “resetable memory,” without more, would be understood by one of ordinary skill in the art to disclose a “resetable memory circuit design” as properly construed, for incorporation into a semiconductor circuit, such that claim 1 is anticipated by Wohl under 35 U.S.C. § 102(b).

Because the remaining dependent claims 2 and 10 depend directly from claim 1, and necessarily include all the limitations of claim 1, these claims also are not anticipated by Wohl.

ii. Claims 11, 12, and 20

Independent claim 11 contains exactly the same limitations in paragraphs a) and b) as discussed above with respect to claim 1. For the same reasons as set forth above, claim 11 and dependent claims 12 and 20 are also not anticipated by Wohl.

E. Motion to Exclude

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 21), along with the Declaration of Dr. Hutchings (Ex. 2011). Petitioner then filed a Petitioner's Reply (Paper 22) as well as a Reply Declaration by Mr. Detjens (Ex. 1024). Subsequently, Patent Owner filed a Motion to Exclude Evidence ("Mot. to Exclude") (Paper 25) arguing, among other things, that the Board should exclude, in their entirety, Petitioner's Reply and Mr. Detjens' Reply Declaration.

*1. Petitioner's Reply and Mr. Detjens' Reply Declaration
(Ex. 1024)*

Patent Owner contends that Petitioner's Reply attempts to advance a new theory that Vander Zanden's output flip-flop DFF6, "*is itself* the resetable memory" along with a corresponding new claim construction that would read flip-flop DFF6 as a "resetable memory." Mot. to Exclude 5. We do not understand Petitioner's Reply as a new theory or claim construction because Petitioner's Reply essentially reiterated their initial proposed construction that a "resetable memory" should include a "memory unit comprising one or more storage cells." *Compare* Pet. 11, *and* Reply 5. In

any event, we determined that on this record, and in accordance with the Specification of the '420 patent, that “resetable memory” should be construed as a memory “that outputs a reset value until new data is written into the memory.” *See* Section II.B.3. Indeed, our claim construction is essentially that urged by Patent Owner in this proceeding.

Patent Owner also complains that Petitioner raised a new single-reference obviousness theory, relying on Vander Zanden, in the Reply. Mot. to Exclude 6. We understand the Petition, and the Reply, to rely upon Vander Zanden to disclose the “inferring” step recited in each of the independent claims 1 and 11. As discussed above in section III.A.2.i, denying anticipation over Vander Zanden, we found that Vander Zanden discloses the step of “inferring” the existence of a memory with reset capability, but not a “resetable memory,” as would be understood by one of ordinary skill in the art in the context of the '420 patent. To the extent Petitioner alleges that the “inferring” step was obvious in view of Vander Zanden in the Reply, we determined that Vander Zanden disclosed this step in our anticipation analysis, and that the elements missing from Vander Zanden, are properly found in Shand, as discussed above in section III.C.2.

Patent Owner next argues that Petitioner presents a “new position” in the Reply that “Vander Zanden’s tool expressly synthesized writes and control signals . . . and the conditions under which each write operation will take place.” Mot. to Exclude 7 (*citing* Reply 3). We do not understand this to be a new position or theory, but a description of memory functions in general. In the context of Vander Zanden’s disclosure of a memory Petitioner’s description is consistent with our claim construction for “memory” as set forth above in Section II.B.2. Petitioner’s reliance in the

Reply upon Figure 8 in Wohl is also not a new theory as Patent Owner asserts because Patent Owner raised the timing issue in its Response based on the parallel executed always statements in Wohl's Figure 6 as being "fatal" to anticipation. *See* PO Resp. 44. Petitioner's Reply merely points out that Figure 8 in Wohl, and the related description, is a further example of behavioral Verilog code that expressly addresses, and corrects, the timing issue from Figure 6. This response, to an issue raised by Patent Owner, that does not go outside the evidence and prior art of record, does not rise to the level of a new argument.

We have reviewed Mr. Detjens' Declaration in Support of Petitioner's Reply, (Ex. 1024) and find the Declaration, as a whole, complies with our rule, 37 C.F.R. § 42.23(b), that a reply may only respond to arguments raised in patent owner's response. For example, Mr. Detjens explains in the Reply Declaration that his testimony is specifically in response to Patent Owner's argument that Vander Zanden does not disclose inferring resettable memories. Ex. 1024 ¶ 5 (citing PO Resp. 29–30). Within the context of Vander Zanden and his previous testimony, Mr. Detjens' Reply Declaration provides appropriate elucidating evidence with respect to the level of ordinary skill in the art in addition to that in his original Declaration. *Compare id.* ¶¶ 6–11, *with* Ex. 1002 ¶¶ 35–43. The Reply Declaration does, in several paragraphs, refer to certain evidence such as Exhibits 1022 and 1023 not filed with the Petition, but overall, relies substantially upon the prior art and evidence submitted with the Petition. Patent Owner's Motion does not apprise us that the Reply or Reply Declaration is raising a new issue or injecting improper new evidence into the proceeding. Our review of the Reply Declaration indicates that overall Mr. Detjens' testimony is proper

rebuttal evidence, timely submitted, in reply to Patent Owner's Response. Therefore, the request to exclude Petitioner's Reply and Mr. Detjens' Reply Declaration (Ex. 1024) is denied.

2. *Exhibits 1005, 1017–1019, 1021–1023, and 1025–1034*

Patent Owner moves to exclude Exhibits 1005, 1017, 1018, and 1019 as irrelevant. Mot. to Exclude 2–3. Patent Owner moves to exclude Exhibits 1022 and 1023 which embody material it argues Petitioner should have addressed in the Petition. *Id.* at 8–10. Patent Owner further moves to exclude Exhibits 1021–1023 and 1025–1034 as irrelevant or related to other exhibits Patent Owner asserts should be excluded. *Id.* at 12–13. Patent Owner moves also to exclude Exhibit 1022 under F.R.E. 901, and Exhibits 1022, 1026–1030, and 1032 as hearsay. *Id.* at 14–15. Exhibits 1026–1032 and 1034 are not of record in this proceeding. We do not rely on any of the remaining exhibits 1005, 1017–1019, 1021–1023, 1025 and 1033. Accordingly, Patent Owner's Motion is dismissed as moot as to these exhibits.

IV. CONCLUSION

We conclude that Petitioner has demonstrated by a preponderance of the evidence that (1) claims 1–3, 10–13, and 20 of the '420 patent are unpatentable as obvious over the combination of Vander Zanden and Shand.

This is a final written decision of the Board under 35 U.S.C. § 318(a). Parties to the proceeding seeking judicial review of this decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

V. ORDER

For the reasons given, it is

ORDERED that claims 1–3, 10–13, and 20 of U.S. Patent No. 6,836,420 B1 are determined by a preponderance of the evidence to be unpatentable;

FURTHER ORDERED Patent Owner’s Motion to exclude Exhibits 1021–1034 is denied-in-part and dismissed-in-part;

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

Case IPR2014-00287

Patent 6,836,420

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