Trials@uspto.gov
571-272-7822

Paper 31
Date Entered: April 18, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,
Petitioner,

v.

PLL TECHNOLOGIES, INC.,
Patent Owner.

Case IPR2015-00148
Patent 6,356,122 B2

Before DAVID C. MCKONE, BEVERLY M. BUNTING, and KEVIN W. CHERRY, *Administrative Patent Judges*.

CHERRY, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6(c). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, we determine that

Petitioner has shown by a preponderance of the evidence that claims 1–10, 12–14, and 16–20 of U.S. Patent No. 6,356,122 B2 (Ex. 1001, "the '122 patent") are *unpatentable*.

A. Procedural History

Petitioner, Xilinx, Inc., filed a Petition requesting an *inter partes* review of claims 1–20 of the '122 patent. Paper 1 ("Petition" or "Pet."). Patent Owner, PLL Technologies, Inc., filed a Preliminary Response. Paper 6 ("Prelim. Resp."). In a Decision to Institute (Paper 8, "Dec. Inst.") issued April 28, 2015, we instituted an *inter partes* review of claims 1–10, 12–14, and 16–20 on the following grounds of unpatentability:

1. Claims 1, 7–10, and 14 as anticipated under 35 U.S.C. § 102(b) by Nienaber[1];
2. Claims 1–3, 7–10, 14, and 17 as obvious under 35 U.S.C. § 103(a) over Nienaber and Young[2];
3. Claims 4, 12, 16, and 18 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, and Taketoshi[3];
4. Claim 5 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, and Kang[4];
5. Claim 6 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, Kang, and Sutardja[5];

[1] Nienaber, US 4,611,230, iss. Sept. 9, 1986 (Ex. 1003).
[2] Young, US 5,446,867, iss. Aug. 29, 1995 (Ex. 1004).
[3] Taketoshi, US 5,389,898, iss. Feb. 14, 1995 (Ex. 1005).
[4] Kang, US 5,999,024, iss. Dec. 7, 1999, filed Dec. 23, 1997 (Ex. 1006).
[5] Sutardja, US 5,576,647, iss. Nov. 19, 1996 (Ex. 1007).

6. Claims 4 and 13 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, and Ferraiolo[6];
7. Claim 19 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, Taketoshi, and Kang; and
8. Claim 20 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, Taketoshi, Kang, and Sutardja.

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 14, "PO Resp.") and Petitioner filed a Reply (Paper 23, "Pet. Reply"). Oral hearing was held on January 26, 2016.[7]

Petitioner submitted the Declaration of Donald Alpert, Ph.D. (Ex. 1010, "Alpert Declaration") and the Declaration of Donald Alpert, Ph.D. in Support of Petitioner's Reply to Patent Owner's Response (Ex. 1014, "Alpert Reply Declaration").

Patent Owner submitted the Declaration of John Hayes, Ph.D., dated August 31, 2015 (Ex. 2002, "Hayes Declaration").

B. The '122 Patent

The '122 patent relates generally to a phase locked loop ("PLL")-based clock synthesizer. Ex. 1001, 1:11–16, Fig. 2. A PLL-clock circuit consists of an oscillator, a reference path, and a feedback path. *Id.* at 1:56–57. The oscillator, which can be a voltage-controlled oscillator ("VCO"), has a reference input receiving a reference signal, a feedback input receiving a feedback signal, and an output. *Id.* at 1:57–59. The reference path

[6] Ferraiolo, US 5,838,205, iss. Nov. 17, 1998, filed Feb. 18, 1997 (Ex. 1008).
[7] A transcript of the oral hearing ("Tr.") is entered as Paper 30.

provides the reference signal from the reference clock input. *Id.* at 1:59–61. The feedback path provides a feedback signal from the oscillator loop output. *Id.* at 1:61–62. The reference input and the feedback input enter a Phase/Frequency Detector ("PFD"), which measures the phase difference between the reference and feedback signals and provides a control signal for the VCO based on this difference. *Id.* at 3:30–39, 3:64–4:4.

Figure 2 is reproduced below.

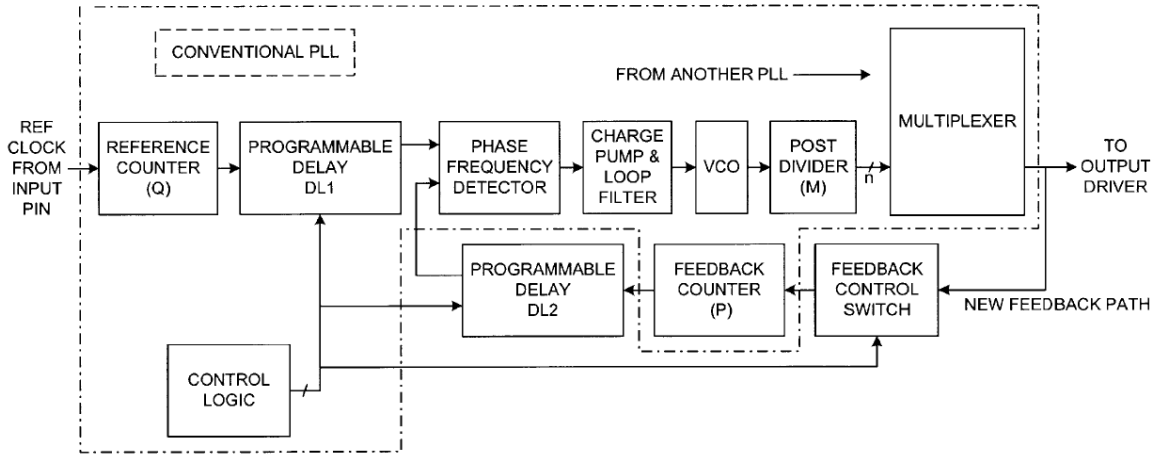

FIG. 2

Figure 2 illustrates a block diagram of a preferred embodiment of the invention of the '122 patent. *Id.* 2:13–14.

The circuit of Figure 2, in addition to the general elements of PLL-clock circuits discussed above, includes a feedback delay block ("DL2") that causes the feedback input to the PFD to lag behind a reference input. *Id.* at 3:64–66. This lag causes the PLL to compensate for the resulting phase difference by making the output of the VCO lead the reference input. *Id.* at 3:67–4:1. In this manner, programming a pre-determined delay value into the feedback delay can eliminate the delays caused by logic components elsewhere in the circuit. *Id.* at 4:1–4. The circuit of Figure 2 also includes a

reference delay block ("DL1") that acts as a "fine-tuning knob" providing a secondary level of control over output delay. *Id.* at 4:5–10. The reference delay has the opposite effect of feedback delay. *Id.* at 4:10–12. Therefore, if the time increments of delay in the programmable feedback delay circuit are not fine enough, the reference delay can be used to compensate for the feedback delay. *Id.* at 4:12–17. The delays for either or both blocks may be fixed or configurable by the user. *Id.* at 4:17–27.

Delay generation may be done through conventional delay lines or through resistor/capacitor ("RC") circuits. *Id.* at 3:25–28. The programmable delay circuit may be conventional, and may comprise a plurality of parallel gates, switches, or transistors. *Id.* at 3:40–48.

C. Illustrative Claims

Claims 1 and 7, apparatus claims, and claim 8, a method claim, are the independent claims of the '122 patent. Claims 2–6, 10, 12, and 13 depend, either directly or indirectly, from claim 1. Claims 9, 14, and 16–20 depend, either directly or indirectly, from claim 8. Claim 1 is illustrative of the subject matter in this proceeding, and is reproduced below.

> 1. A clock circuit, comprising:
>
> an oscillator, having a reference input receiving a reference signal, a feedback input receiving a feedback signal, and an output;
>
> a reference path providing said reference signal from a reference clock input; and
>
> a feedback path providing said feedback signal from the oscillator output;
>
> wherein each of the reference path and the feedback path comprises a programmable delay circuit.

Id. at 5:24–35.

II. ANALYSIS

A. Claim Interpretation

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 (Fed. Cir. 2015), *cert. granted sub nom. Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 890 (mem.) (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *See In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

"clock"

In our Decision to Institute, we agreed with Petitioner's declarant that the broadest reasonable construction of the term "clock" is a "periodic timing control signal." Dec. Inst. 8–9 (citing Ex. 1010 ¶ 77). We found that our construction was consistent with the Specification. Dec. Inst. 9 (citing Ex. 1001, 1:19–35 (discussing clock synthesizer as generating an output frequency based on a reference clock input and the cyclic relationship of the signals), 2:45–3:20 (discussing clock signals as periodic signals)).

Patent Owner submits that we should construe "clock" as a "periodic signal used for synchronization in a digital system." PO Resp. 16. In support of this construction, Patent Owner relies heavily on extrinsic evidence. *See id.* at 12–19. Patent Owner argues that we should not rely on

Petitioner's declarant's "unsubstantiated, litigation-induced definition of the term 'clock,'" and should instead "adopt an interpretation that is based on reliable, unbiased authority." *Id.* at 12.

Patent Owner identifies the *IEEE Dictionary* as such an "authoritative source," and asserts that, based on the definitions contained in the *IEEE Dictionary*, the broadest definition is "a periodic signal used for synchronization." *Id.* at 12–13 (citing Ex. 2007 (IEEE STANDARD DICTIONARY OF ELECTRICAL & ELECTRONICS TERMS 163 (6th ed. 1996)); Ex. 2002 ¶ 40). Patent Owner contends that "although that definition appears to be facially not limited to digital systems, it is in fact applicable only in the context of computer or other synchronous digital systems, and, thus, invalid for non-digital systems." *Id.* at 13 (citing Ex. 2002 ¶ 41). Patent Owner bases this contention, in part, on its interpretation of the *IEEE Dictionary*. *Id.* at 13–16.

In its analysis of the *IEEE Dictionary*, Patent Owner focuses on the "category codes" used in the dictionary. *Id.* at 14. Patent Owner explains that the "category code" that follows each definition "establish[es] the context in which the definition applies" and explains the standards that are the sources of the definitions. *Id.* at 14–15. Patent Owner submits that the term "clock" or "clock signal" are in the "C" category that signifies "computer." *Id.* at 15 (citing Ex. 2007, v, 163–64). Patent Owner argues that the IEEE standards that are the sources of the definitions "are all computer- or digital-based standards." *Id.* Thus, Patent Owner concludes that "[s]tating that context explicitly in the interpretation of the term 'clock' in this case leads to [Patent Owner's construction]"—"Periodic signal used for synchronization in a digital system." *Id.* at 16 (citing Ex. 2007 ¶ 42).

We are not persuaded by Patent Owner that the claims of the '122 patent should be limited to digital systems. We begin our analysis with the intrinsic evidence from the '122 patent. *See In re Translogic Tech.*, 504 F.3d at 1257. First, the language of the claims provides no basis, and Patent Owner directs us to none, for limiting the claims to uses in a digital system. Indeed, as Patent Owner conceded, the structural components of the circuit that are recited in the independent claims, i.e., the reference path, the feedback path, the oscillator, and the delay circuits, are not limited to digital applications. Tr. 42:21–44:9.

As for the Specification, Patent Owner does not direct us to any criticism of non-digital systems or specific statements in the Specification that Patent Owner contends explicitly or implicitly limit a clock or the invention to digital systems. Instead, Patent Owner states that "the '122 Patent does not describe or contemplate non-digital applications of its 'clock.'" PO Resp. 20 (citing Ex. 2002 ¶ 46). However, the only support cited for this contention, i.e., Paragraph 46 of Dr. Hayes's Declaration, states, without any citation: "The '122 Patent does not describe or contemplate non-digital applications of its 'clock' and thus fully supports the fact that a 'clock' signal is for a digital system." Ex. 2002 ¶ 46. We do not find this conclusory testimony, without any citation or explanation, to be entitled to any weight. *See* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."); *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 294 (Fed. Cir. 1985) (stating a lack of objective support for an expert opinion "may render the testimony of little probative value in [a patentability] determination").

Patent Owner also asserts that Dr. Alpert recognizes that the '122 patent does not describe or contemplate non-digital applications of its clock. PO Resp. 20 (citing Ex. 1010 ¶¶ 27–29). However, we do not understand Dr. Alpert's testimony as stating such a conclusion. Dr. Alpert describes certain problems in personal computers, and concludes that "[t]he '122 patent aims to provide a solution to problems like that described above for controlling timing to transfer data between components." Ex. 1010 ¶ 29. This testimony establishes one problem that the '122 patent seeks to solve, but does not support Patent Owner's conclusion that the '122 patent does not contemplate any non-digital applications for its circuit.

We have reviewed the '122 patent and have been unable to locate any mention of the term "digital" or reference that the circuit is limited to only certain particular uses. The '122 patent describes clocks broadly as periodic signals used for timing control. *See, e.g.*, Ex. 1001, 1:19–35 (describing a clock synthesizer as generating an output clock based on an input clock, where both input and output clocks are periodic signals having "cycles"), 2:45–3:20 (discussing clock signals as periodic signals). Indeed, the Specification broadly states that "[t]he present invention enjoys particular advantages in applications where a predictable input-output phase relationship is desired, particularly where the output frequency is an integral or one-half an integral multiple of the input frequency." *Id.* at 1:48–53. Thus, the Specification describes its potential uses very broadly. Such a broad discussion of potential uses supports Petitioner's construction.

Even if the '122 patent only describes a digital embodiment, that alone is not enough to limit the claims to the preferred embodiment. Ex. 1001, 5:20. We note that:

> A patent that discloses only one embodiment is not necessarily limited to that embodiment. *Saunders Grp., Inc. v. Comfortrac, Inc.*, 492 F.3d 1326, 1332 (Fed. Cir. 2007). "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel–Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

GE Lighting Sols., LLC v. AgiLight, Inc., 750 F.3d 1304, 1309 (Fed. Cir. 2014) (alteration in original). Patent Owner identifies no such clear indication here.

Patent Owner also directs our attention to the prosecution history. PO Resp. 20–21. In particular, Patent Owner submits that nearly all of the references cited by the Examiner during the prosecution involved digital systems. *Id.* at 20. Thus, Patent Owner concludes that the Examiner's "consistent citation of references having 'clocks' in computer systems, show implicitly that the Examiner understood that a 'clock' in the '122 Patent is a synchronous digital system clock." *Id.* at 20–21. However, Patent Owner does not identify anywhere the applicant or Examiner stated that the claims were limited to digital systems, or where either made any explicit finding or contention in this regard. We decline to draw any inferences from the Examiner's search strategy when the Examiner was silent regarding the meaning of the term "clock." *See DeMarini Sports, Inc. v. Worth, Inc.*, 239 F.3d 1314, 1326 (Fed. Cir. 2001) ("Drawing inferences of the meaning of claim terms from an examiner's silence is not a proper basis on which to construe a patent claim.").

As for the extrinsic evidence, we find that this evidence does not support limiting "clock" in the context of the '122 patent to use only in digital systems. Although extrinsic evidence can be a useful tool, we weigh

all such evidence together and we discuss it below only to the extent that it helps us understand the intrinsic evidence. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1317–19 (Fed. Cir. 2005) (en banc).

We note that Patent Owner criticizes Dr. Alpert's definition of "clock" as "litigation motivated," but we do not discern any substantive difference between Dr. Alpert's definition and the definition provided by the *IEEE Dictionary* of "a periodic signal for synchronization." *See* PO Resp. 12–13 (quoting Ex. 2007). Patent Owner argues that a field of use (computers and digital technology) is "inherent" in the dictionary definition. Although we agree with Patent Owner that the category codes and corresponding standards can provide useful context, we are not persuaded that the "category codes" and the standards to which they correspond necessarily limit the definitions provided in the *IEEE Dictionary*. Moreover, as Petitioner demonstrates and Patent Owner's declarant concedes, the "C" category code is not limited exclusively to "digital" systems. Pet. Reply 3–6 (citing Ex. 1014 ¶¶ 7–13); Ex. 1019, 31:20–32:10 (conceding the "C" code is not limited to digital systems).

As for Dr. Hayes's testimony that "clock" has an established meaning in synchronous digital systems and does not have a recognized meaning in analog systems, we do not find that testimony persuasive. PO Resp. 16–18 (citing Ex. 2002 ¶¶ 43–45). Dr. Alpert has offered examples of analog or hybrid analog/digital systems that use a "clock" signal. *See* Ex. 1014 ¶¶ 14–16, 23–40; Ex. 1020; Ex. 1021. Petitioner and Dr. Alpert have provided other extrinsic evidence that supports Dr. Alpert's testimony and counsels against Patent Owner's interpretation of the extrinsic evidence. This evidence suggests that clock signals can be analog as well as digital.

Finally, Patent Owner submits that both parties' definitions of a person of ordinary skill in the art require experience in digital systems. PO Resp. 18–19. Based on this experience, Patent Owner argues that a person of ordinary skill would "naturally" think of the term as being limited to a digital system. *Id.* at 19. We do not agree. The fact that "clock" might be used widely in digital systems does not serve as a basis for limiting this invention to use only in digital systems. As Patent Owner admitted, PLL circuits are widely used in both analog and digital applications, Tr. 26:3–25, and a person of ordinary skill would have been aware of those applications and of art discussing "analog clocks" that Petitioner identified, Tr. 39:22–40:12. Thus, we do not find the particular experience of a person of ordinary skill to be a basis for limiting the ordinary meaning of the claim term in this case.

Weighing the extrinsic evidence together, we do not agree with Patent Owner that the extrinsic evidence supports its construction of "clock." Instead, we find Dr. Alpert's testimony and evidence persuasive that the ordinary meaning of "clock" is not limited to digital systems.

Accordingly, we conclude that the term "clock," as used in the '122 patent is simply "a periodic signal for timing control (or synchronization)."[8]

"clock circuit"

Patent Owner also proposes a construction for "clock circuit" recited in claim 1 of "a circuit that generates a periodic signal used for

[8] Petitioner and Patent Owner acknowledged there was no meaningful difference between the terms "timing control" or "synchronization." Tr. 7:14–21, 41:13–23. We see no meaningful distinction in this case between the terms "synchronization" or "timing control."

synchronization in a digital system." PO Resp. 21. Patent Owner's proposed construction is based, in part, on Patent Owner's proposed construction for the term "clock." *Id.* We decline to adopt Patent Owner's construction. As discussed above, we determined that "clock" is not limited to a "digital system" as Patent Owner contends.

"*a programmable delay circuit*"

Petitioner argues that the broadest reasonable interpretation of "a programmable delay circuit" is a delay circuit that can be programmed, configured, or adjusted to vary its delay time. Pet. 10–11; Pet. Reply 8–11.

In our Decision to Institute, we agreed with Petitioner. Dec. Inst. 8. Now, having the benefit of the full record developed during trial, we consider again the parties' proposed construction of the claim term "programmable."

In its Patent Owner Response, Patent Owner argues that "programmable" should be construed as "capable of storing in memory data and/or instructions to alter the delay." PO Resp. 22. Patent Owner raises four main points. PO Resp. 22–29. First, Patent Owner addresses our construction from the Decision to Institute. *Id.* at 22–24. Patent Owner argues that "programmable" is a "special case of the generic terms 'configurable' and 'adjustable.'" *Id.* at 22. Patent Owner asserts that "adjustable" is "generic as to the manner of adjustment," *id.* at 22–23, and "configurable" implies "adjustment by means of configuration," *id.* at 23. Patent Owner submits that "configurable" is narrower than "adjustable," but that both are broader than the term "programmable," because "programmable" connotes "adjustment by one particular technique — by means of programming." *Id.* Thus, according to Patent Owner, although

something that is "programmable" is "adjustable" and "configurable," something that is "adjustable" or "configurable" is not necessarily "programmable." *Id.* 23–24.

Second, Patent Owner identifies two definitions from the *IEEE Dictionary*, which it contends can be distilled down to a single definition of "capable of accepting data and/or instructions to alter a device's state to perform specific task(s) or to alter its basic function." PO Resp. 24–25 (citing Ex. 2007, 826 (IEEE STANDARD DICTIONARY OF ELECTRICAL & ELECTRONICS TERMS 826 (6th ed. 1996)).

Third, Patent Owner argues, much as it did with respect to "clock," that although the *IEEE Dictionary* definitions do not refer explicitly to a memory, a memory is "inherently necessary to accept data and/or instructions." *Id.* at 25–26 (citing Ex. 2002 ¶ 49).

Finally, Patent Owner argues that its construction is consistent with the intrinsic evidence. *Id.* at 26–29. In particular, Patent Owner argues that the Specification never uses "configurable" or "adjustable" to refer to anything broader than "configurable" or "adjustable" through "programming." *Id.* at 26–27 (citing Ex. 2002 ¶¶ 50, 51; Ex. 1001, 4:17–18, 4:39–42, 4:66–5:4). Patent Owner also asserts that the Specification makes "extensive reference to memory, which is required for programmable delays to function as recited in the '122 patent." *Id.* at 27. Patent Owner also identifies description in the Specification of use of memory to store programming information. *Id.* at 28 (citing Ex. 1001, 2:24–36, 2:45–47). Patent Owner further argues that the references applied by the Examiner during prosecution support its construction because "[a]ll of the references

applied by the Examiner, except Young, disclose programming using data and/or instructions stored in memory." *Id.* at 29.

We agree with Patent Owner that we should modify our preliminary construction, at least to the extent that, as used in the Specification, the term "programmable" is not interchangeable with "adjustable" or "configurable." Instead, we agree with Patent Owner that the Specification only refers to "programming" as a more limited example of "adjustable" or "configurable." *See, e.g.*, Ex. 1001, 2:18–27 ("The present invention concerns applications which use a programmable delay circuit (or other, similarly configurable PLL-based clock generator, such as a serially configurable device) where the input-output phase relationship is dependent on the values of the internal counters and the multiplexers in the output path, which in turn are dependent on the specific configuration of the device. Program and/or configuration information may be stored in a conventional nonvolatile or volatile memory. . . ."), 4:17–20 ("[I]f these delay blocks are configurable through serial programming of configuration bits, then the user can dynamically fine-tune the PLL for their particular application."), 4:45–49 ("If the delay blocks . . . are controllable through serially downloadable data words, then the user may have some adjustability and/or configurability in fine-tuning a system . . . containing the present clock circuit.").

We also agree with Patent Owner that the *IEEE Dictionary* provides an example of the ordinary and customary meaning of the term. We further agree that based on the definitions of term in the *IEEE Dictionary* that the ordinary and customary meaning of the term "programmable" is "capable of accepting data and/or instructions to alter a device's state to perform specific

task(s) or to alter its basic function." *See* PO Resp. 25. This is consistent with the description in the Specification, detailed above.

We do not see any support, however, for Patent Owner's argument that the construction must also include a memory. Patent Owner argues that a memory is "inherent" in the capability of accepting data or instruction, citing to testimony by Dr. Hayes. *See id.* at 25–26 (citing Ex. 2002 ¶ 49). Dr. Hayes's testimony, however, is conclusory and cites to no evidence that supports his contention. Ex. 2002 ¶ 49. Thus, we give it minimal weight. *See* 37 C.F.R. § 42.65(a).

As for Patent Owner's arguments that the intrinsic evidence supports the requirement that there must be a memory, we do not agree. To begin with, the claims recite nothing about a memory. As for the Specification, all of the discussions regarding the use of memory make clear that the memory is an optional component and is not required. *See* Ex. 1001, 2:24–33 ("Program and/or configuration information *may be* stored in a conventional nonvolatile or volatile memory. . . ."), 2:45–48 ("If the reference clock input is an electrical clock signal, the input-output phase relationship can be made user-programmable, through programmable memory, Serial Interface, *or* hardware inputs. . . ."), 4:66–5:4 ("Configuration bits *may be* stored in flash memory, random access memory (RAM, which may be static or dynamic), or a plurality of registers. *When the configuration bits are stored in flash memory*, EPROM or EEPROM, they may be reprogrammed while the clock circuit is in place in the system or board."). This permissive, rather than restrictive, language indicates that the invention is not meant to be limited to programming that requires information to be stored in a memory. *See Prolitec, Inc. v. Scentair Techs., Inc.*, 807 F.3d 1353, 1358 (Fed. Cir. 2015)

("[T]he use of 'may' signifies that the inventors did not intend to limit [the claim] . . . .").

In addition, the Specification discloses:

> A logic block may be configured to control the delay blocks and configure the feedback path (e.g., select its input or source). *The logic circuitry and configuration bits in the logic block can be one-time programmable (e.g., using EPROM, ROM, fuses, or metal-masks)*, or serially programmable through IC input pins or programming hardware input pins. In the first case, the delay may not [be] controlled by the user unless one builds field programming capability into the part.

Ex. 1001, 4:37–45 (emphasis added). The Specification expressly contemplates that programming may be done without a memory using fuses or metal masks. Ex. 1014 ¶¶ 17–19; Ex. 1010 ¶¶ 33, 43. Thus, we agree with Petitioner that the Specification does not require that a memory be included in order for the delay to be programmable. *See* Pet. Reply 9–10.

As for Patent Owner's prosecution history arguments, we do not find them persuasive. PO Resp. 29. Patent Owner seeks to read inferences into the Examiner's citation of certain references, but the Examiner never took any express position on the claim construction of this term. As we explained above, the Examiner's silence on a topic is not a proper basis for claim construction. *See DeMarini Sports*, 239 F.3d at 1326. Moreover, Patent Owner's argument that the references cited suggest a memory is required is refuted by the Examiner's reliance on Young (which Petitioner also relies on below), which teaches programming the delay without a memory.

Accordingly, we determine that the broadest reasonable construction of "programmable delay circuit" is a delay circuit that is "capable of accepting data or instructions, or both, to alter the delay."

Means-Plus-Function Limitations

Independent claim 7 recites several limitations that Petitioner contends should be interpreted as means-plus-function limitations subject to 35 U.S.C. § 112 ¶ 6.[9] Pet. 11–13. In our Decision to Institute, we found certain functions and corresponding structure for those limitations. Dec. Inst. 9–10. Neither party disputes this determination. Based on a full record, we see no reason to alter our preliminary construction for these elements and adopt them for purposes of this Final Written Decision. *Id.*

B. Claims 1, 7–10, and 14: Anticipation by Nienaber

Petitioner contends that claims 1, 7–10, and 14 are unpatentable under 35 U.S.C. § 102(b) as anticipated by Nienaber. To support its contention, Petitioner provides a detailed showing mapping limitations of claims 1, 7–10, and 14 to structures described by Nienaber. Pet. 14–24. Petitioner also cites the Alpert Declaration for support. *See* Ex. 1010 ¶¶ 74–116.

Nienaber (Ex. 1003)

Nienaber, titled, "Vertical Video Centering Control System," discloses a phase shifting means for altering the phase relationship between a vertical sync signal and video information in a video display environment. Ex. 1003, Abstract.

Figure 1 of Nienaber is reproduced below.

[9] Section 4(c) of the Leahy-Smith America Invents Act ("AIA") re-designated 35 U.S.C. § 112 ¶ 6 as 35 U.S.C. § 112(f). Pub. L. No. 112-29, 125 Stat. 284, 296–07 (2011). Because the '122 patent has a filing date before September 16, 2012 (effective date of § 4(c)), we refer to the pre-AIA version of 35 U.S.C. § 112, in this Decision.

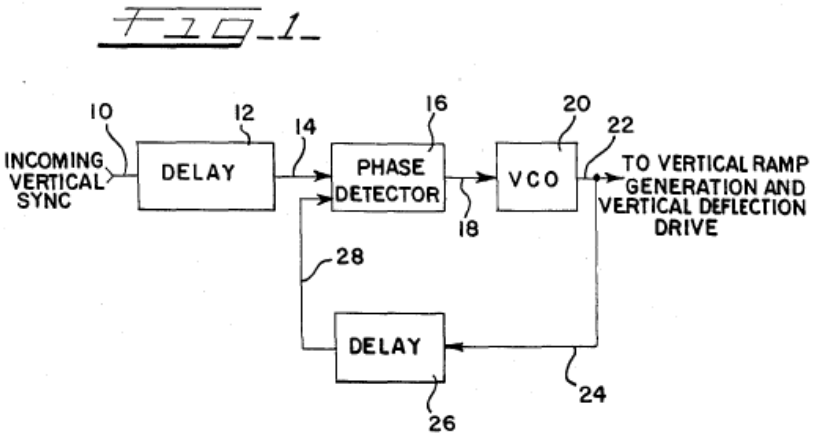

Figure 1 is a schematic block diagram showing a preferred embodiment of the loop circuit system of Nienaber. *Id.* at 2:45–47.

In particular, Figure 1 depicts an incoming vertical sync signal that is received on line 10 by first delay circuit 12. *Id.* at 3:10–11. Delay circuit 12 communicates its output signal via line 14 to phase detector circuit 16, which communicates via line 18 with VCO 20. *Id.* at 3:11–15. The output of VCO 20 on line 22 then is provided to a vertical ramp generation and vertical deflection drive circuitry (not shown) to accomplish the necessary vertical timing for a video display raster. *Id.* at 3:15–18. The output of VCO 20, which is on line 22, is supplied further via line 24 to second delay circuit 26. *Id.* at 3:18–20. The output of delay circuit 26 is provided via line 28 as a second input into phase detector circuit 16. *Id.* at 3:20–22.

Phase detector circuit 16 generates an output on line 18 as a representation of the phase difference between the signals received on lines 14 and 28. *Id.* at 3:23–26. The output on line 18 then will cause the VCO 20 to alter appropriately its output on line 22 and correspondingly on line 24. *Id.* at 3:26–29. The loop serves to correct any phase difference that may exist between the vertical sync signal received on line 14 and signal on line 28. *Id.* at 3:29–33.

Delay circuits 12 and 26 may comprise typical resistor/capacitor (RC) networks for delaying the signals presented at their respective inputs. *Id.* at 3:43–46. Either or both of delay circuits 12 and 26 may be adjustable. *Id.* at 3:47–48.

Analysis

In support of this asserted ground of unpatentability, Petitioner provides explanations as to how the subject matter of claims 1, 7–10, and 14 is disclosed by Nienaber. Pet. 14–24. For example, with respect to independent claim 1, Petitioner contends that Nienaber discloses "a clock circuit" through its disclosure of a phase shifting circuit that includes a PLL for altering the relationship (timing) between a vertical sync signal and a vertical retrace on a video display. *See* Pet. 14; Ex. 1003, Fig. 1 (showing PLL circuit), Abstract ("Phase shifting means for altering the phase relationship between a vertical sync signal, the resulting vertical retrace, and video information in a video display environment.").

Petitioner further contends that Nienaber discloses an oscillator, having a reference input receiving a reference signal, a feedback input receiving a feedback signal, and an output," and "a feedback path providing said feedback signal from the oscillator output" through its disclosure of a PLL circuit with a voltage controlled oscillator, phase detector, input path, and feedback path. *See* Pet. 14–20; Ex. 1003, Figure 1 (showing circuit containing these elements), 3:8–33 (describing circuit of Figure 1); Ex. 1010 ¶¶ 54, 55, 76–86.

Petitioner further explains how Nienaber, through its description of adjustable delay circuits, discloses programmable delay circuits in both the input and feedback paths, as recited in claim 1. Pet. 16, 19–20; Ex. 1003,

Abstract ("Either or both of the first and second delay circuits may be adjustable to vary the amount of phase shift introduced between the original vertical sync signal and the output vertical sync signal."), 3:43–62 (discussing delay circuits in detail and describing them as "adjustable"), 3:66–67 (terming delay "adjusted"), 4:14–15 (discussing adjusting the delay), 6:18–20 (claim directed to adjustable delay means in both paths); Ex. 1010 ¶¶ 85, 86.

Finally, Petitioner contends that Nienaber discloses a "reference signal from a reference clock input," as recited in claim 1, through its disclosure of an incoming vertical sync signal. Pet. 15, 18–19; Ex. 1003, 3:10–15 (discussing incoming vertical sync signal), Fig. 1 (showing including signal), Fig. 2 (showing exemplary waveforms of vertical sync signal); Ex. 1010 ¶¶ 81, 82.

Patent Owner argues that Nienaber does not disclose a "programmable delay circuit" and a "reference clock input," "a clock output," and a "clock circuit," as recited in claim 1. PO Resp. 29–37. Patent Owner does not dispute that Nienaber discloses the other limitations of claim 1. *See id.* Based on the full record after trial and the construction of "programmable delay circuit" discussed above, Petitioner's evidence and arguments do not persuade us that Nienaber discloses each of the disputed limitations of claim 1 of the '122 patent.

With respect to "programmable delay circuit," as we have construed it, Petitioner admits that Nienaber does not disclose a delay circuit that is "capable of accepting data or instructions, or both, to alter the delay." Tr. 14:3–25. Although Nienaber discloses "adjustable" delay circuits, it does not disclose delay circuits that can accept data or instructions, or both,

to alter the delay, based on the correct construction of "programmable delay circuit." *Id.* Thus, we determine that Petitioner has not shown by a preponderance of the evidence that Nienaber anticipates claim 1.

Petitioner's contentions that Nienaber anticipates claims 7–10 and 14 rely on the Nienaber's disclosure of adjustable delay circuits that we found inadequate with respect to claim 1. Pet. 20–27. Thus, we are persuaded Petitioner has not shown by a preponderance of the evidence that claims 1, 7–10, and 14 of the '122 patent are anticipated by Nienaber.

C. Claims 1–3, 7–10, and 14: Obviousness over Nienaber and Young

Petitioner contends that claims 1–3, 7–10, and 14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Nienaber and Young. To support its contention, Petitioner provides a detailed showing mapping limitations of claims 1–3, 7–10, and 14 to the disclosure of Nienaber and Young. Pet. 24-29. Petitioner also cites the Alpert Declaration for support. *See* Ex. 1010 ¶¶ 54, 55, 76–144.

Young (Ex. 1004)

Young, titled, "Microprocessor PLL Clock Circuit with Selectable Delayed Feedback," discloses a clock generator circuit for a microprocessor that generates a clock used internally to the microprocessor using an external clock input. Ex. 1004, Abstract.

Figure 1 of Young is reproduced below.

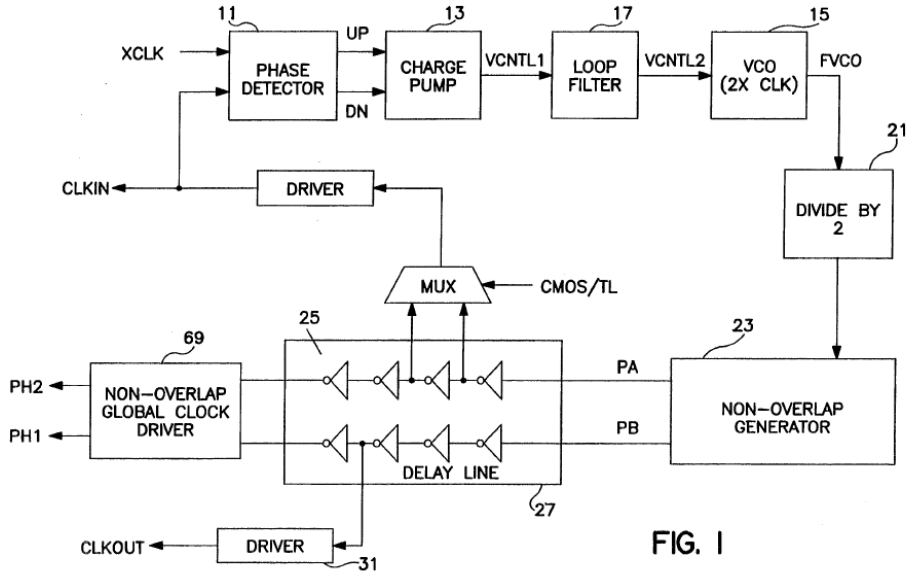

Figure 1 is a block diagram of the clock circuit of Young. *Id.* at 2:37–39.

The circuit includes phase detector 11, charge pump 13, loop filter 17, and VCO 15. *Id.* at 2:53–55. In the feedback path, Young includes delay line 27 with a programmable delay. *Id.* at 3:51–52. Delay line 27 comprises a set of identical delay elements and support logic circuitry. *Id.* at 3:52–53. The logic circuit can control the length of the delay based on a mode selected by the user. *Id.* at 4:45–60.

Analysis

In support of this asserted ground of unpatentability, Petitioner provides explanations as to how the subject matter of claims 1–3, 7–10, and 14 is accounted for by Nienaber and Young. Pet. 24–29. For example, with respect to independent claim 1, Petitioner contends, as discussed above in the anticipation discussion, that Nienaber discloses "a clock circuit," "an oscillator, having a reference input receiving a reference signal, a feedback input receiving a feedback signal, and an output," "a feedback path providing said feedback signal from the oscillator output," and a delay

circuit in both the reference path and feedback path. Pet. 14–20 (citing Ex. 1003, Abstract, 2:33–36, 3:8–33, 3:43–62, 3:66–67, 4:14–15, 6:18–20, Fig. 1; Ex. 1010 ¶¶ 54, 55, 76–85). Petitioner further argues that Young discloses a "programmable delay circuit," as recited in claim 1. Pet. 25–26 (citing Ex. 1004, 4:45–60, Fig. 1; Ex. 1010 ¶¶ 118–121).

Petitioner contends that a person of ordinary skill would have been motivated to combine the PLL circuit with adjustable delay circuits in the feedback and reference paths of Nienaber, and the programmable delay circuit found in Young, because both references have circuits that are structured similarly, and both references relate to similar subject matter of using delay circuits within a PLL clock circuit to adjust the amount of phase shift between the reference clock and the feedback signal. Pet. 25–26. In other words, Petitioner argues that a skilled artisan would have substituted a digital delay circuit, as taught by Young, in place of each of Nienaber's analog delay circuits. Petitioner further argues that substituting the "adjustable" delay circuits of Nienaber with the "programmable" delay circuits found in Young would have yielded the predictable result of having programmable delay elements in the reference and feedback paths. *Id.* at 26 (citing Ex. 1010 ¶¶ 117–121).

Patent Owner challenges Petitioner's assertions by arguing that (1) a person ordinary skill would not have combined Nienaber and Young because the combination would render Nienaber unsuitable for its intended use, and (2) the resulting combination would not teach the limitations of "programmable delay," a "reference clock input," "clock circuit," and "clock output." PO Resp. 29–42. Patent Owner does not dispute that Nienaber accounts the other limitations of claim 1. *See id.* at 29–42. Based on the full

record after trial, we find that the combination of Nienaber and Young, as described above with Petitioner's citations and arguments, accounts for each limitation of claim 1 of the '122 patent and Petitioner has provided articulated reasoning with some rational underpinning why a person of ordinary skill would have combined the references. We focus our discussion below on Patent Owner's counterarguments, which we find unpersuasive.

Patent Owner raises the same arguments for each of "reference clock input," "clock output," and "clock circuit," PO Resp. 29–36, so we consider these limitations together. First, although Patent Owner concedes that Nienaber's vertical sync signal is "somewhat periodic and used for synchronization," PO Resp. 30, Patent Owner argues that the vertical sync signal is not a clock signal because it is not used in a digital system. *Id.* at 30, 34–35. Second, Patent owner argues that "[a]nother difference between the vertical sync signal and a clock is that a vertical sync signal must be processed, whereas clock signals are not typically processed." *Id.* at 35 (citing Ex. 2002 ¶ 62). We are not persuaded by either of these arguments that Nienaber fails to teach or suggest a "clock."

As for the first argument, we have rejected Patent Owner's efforts to limit "clock" for use in a digital system. Our construction only requires "a periodic signal for synchronization." Both declarants effectively agree that Nienaber's vertical sync signal is a periodic signal for synchronization. Ex. 1010 ¶ 77; Ex. 2002 ¶ 61; *see also* PO Resp. 34–35 ("The fact that the incoming vertical sync signal is a periodic signal used for synchronization or timing control is insufficient to qualify it as a 'clock' signal."). Patent Owner's assertions about the precise use and purpose of the vertical sync signal (PO Resp. 29–35) do not reflect any structures or limitations recited in

the claims, so we do not consider them persuasive. *See In re Self*, 671 F.2d 1344, 1348 (CCPA 1982).[10]

Moreover, even if the "clock" was required to be digital, we are persuaded that Nienaber would still teach or suggest this limitation. Petitioner has presented evidence that Nienaber teaches or suggests a hybrid or mixed signal system that uses a digital clock signal for timing control to a person of ordinary skill in the art. Pet. Reply 13–16 (citing Ex. 1014 ¶¶ 23–47). As Dr. Alpert persuasively testifies some televisions in the mid-1980s, i.e., near the date of invention of Nienaber, were hybrid systems including both digital and analog components and techniques. Dr. Alpert supports his testimony with extensive citation to and explanation of Nienaber and various prior art references from that time, and thus, we find that his testimony is entitled to substantial weight. Ex. 1014 ¶¶ 25–45; Ex. 1025 (article from 1972 discussing use of digital techniques in televisions); Ex. 1003, 3:34–42 (Nienaber discussing using its circuit in video monitors and "non-standard television applications"); Ex. 1017, Fig. 3, 5:4–24, 6:28–57 (discussing use of digital vertical sync signals in television monitors); Ex. 1020 (hybrid system using "clock" signal); Ex. 1021 (hybrid system using "clock" signal); Ex. 1023 (hybrid circuit with digital clock).

These references establish that a person of ordinary skill would have understood that Nienaber suggested using a digital vertical sync signal. *In re*

[10] To the extent that Patent Owner now contends that the vertical sync signal is not a clock because it is only "approximately" or "not perfectly" periodic (Tr. 31:9–22), this argument does not appear to have been raised in its Patent Owner Response. We further note there is no requirement in our construction that the signal be "perfectly" periodic. Thus, we do not find this argument persuasive.

Preda, 401 F.2d 825, 826 (CCPA 1968) (citing *In re Shepard*, 319 F.2d 194 (CCPA 1963)) (noting that "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom"). Indeed, Dr. Hayes conceded at his deposition that the exemplary waveforms of the vertical sync signal shown in Figure 2 are digital, Ex. 1019, 42:8–16, and that vertical sync signals used in televisions and computer monitors at the time of Nienaber's invention were digital, *id.* at 43:7–9, 44:6–9. Thus, we find that even if the claims required a digital signal, Nienaber's vertical sync signal teaches or suggests such a signal.

As for Patent Owner's second argument that Nienaber's vertical sync signal cannot be a clock because it must be "processed," we do not find this argument persuasive. PO Resp. 35. As Patent Owner implicitly concedes, there is nothing that forbids a clock signal from being processed. *See id.* (stating "clock signals are not *typically* processed" (emphasis added)). Patent Owner points to no intrinsic evidence requiring that the clock signal recited in the claims to be unprocessed, and we decline to read such a requirement into the claim. Moreover, the only evidence Patent Owner cites is the testimony of Dr. Hayes (Ex. 2002 ¶ 61), but Dr. Hayes provides no support for his testimony. In contrast, Dr. Alpert testifies that there is no such requirement and cites to several examples of "gated" clocks. Ex. 1014 ¶ 47. We find Dr. Alpert's testimony supported by the evidence cited and give his testimony substantial weight. Thus, we find that Petitioner has shown that Nienaber's vertical sync signal is a "clock," as we have

construed that term for purposes of this Decision. *See* Pet. 15, 20; Ex. 1010 ¶ 77; Pet. Reply 11–16; Ex. 1014 ¶¶ 23–47.

Thus, we determine that the combination of Nienaber and Young accounts for the "clock" limitations of the independent claims.

With respect to Patent Owner's arguments that Young does not disclose a "programmable delay" (PO Resp. 41–42), we find that even under our construction of "programmable delay circuit," which requires a delay circuit accepting data or instructions, or both, to alter the delay, Young accounts for this element. We find that Young describes its delay lines as "programmable," Ex. 1004, Abstract, 4:45–60; Ex. 1010 ¶ 120, and that the type of programming is indistinguishable to that described by the '122 patent as "one-time programmable," Ex. 1001, 4:37–45; Ex. 1014 ¶¶ 49–51. As Patent Owner admits, Young teaches setting a value to either a logic 1 or 0. Tr. 52:19–25. We find this value is data that alters the delay, which meets the claim limitation. *See* Tr. 53:1–11. Thus, we determine that Petitioner has shown that the combination of Nienaber and Young accounts for the "programmable delay circuit." *See* Ex. 1014 ¶¶ 49–52.

We are not persuaded by Patent Owner's argument that a person of ordinary skill would not have been motivated to combine Nienaber and Young because the combination of Nienaber and Young would be inoperable. PO Resp. 38–41. Patent Owner argues that Nienaber is directed to a circuit that provides two vertical controls to adjust an analog television or video monitor picture both up and down. *Id.* at 38 (citing Ex. 1003, 3:43–62). Patent Owner submits that the delay circuit of Young only provides one of two possible delays—to allow operation with two possible clocks. *Id.* at 38–40 (citing Ex. 1004, 2:1–21). Patent Owner argues that "because of the

binary, two-choice nature of Young's delay elements (i.e., having just two possible delay values), one skilled in the art would not have made the substitution the Petition proposes, as the substitution would have resulted in insufficient granularity for vertically aligning a television or video monitor picture acceptably." *Id.* at 40 (citing Ex. 2002 ¶ 67). Patent Owner submits that, at best, the combination would have only four possible delays, and hence four possible vertical alignments, which would be insufficient to satisfactorily align the picture. *Id.* at 40–41. Thus, Patent Owner argues that the combination would render Nienaber unsatisfactory for its intended purpose. *Id.* at 41 (citing MPEP 2143.01(V)).

We do not agree with Patent Owner that the combination of Nienaber and Young would render Nienaber unsatisfactory for its intended purpose or that a person of ordinary skill would not have been motivated to combine Nienaber and Young.

To begin with, we find that Patent Owner's identification of the intended use of Nienaber is too narrow. We agree with Petitioner (Pet. Reply 22–23) that Nienaber discloses generally a "phase shifting means" for the purpose of "enabl[ing] video information to be shifted both up and down on a video display without undesirable side effects." Ex. 1003, Abstract. Thus, we agree with Petitioner's reasoning that, even incorporating Young without any of the modifications a person of ordinary skill would naturally make (discussed below), the combination would still be sufficient to accomplish Nienaber's purpose. *See In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012) ("[J]ust because better alternatives exist in the prior art does not mean that an inferior combination is inapt for obviousness purposes.").

In addition, we determine that Patent Owner's argument appears to be premised, at least in part, on an erroneous assumption that the delay elements of Young would be bodily incorporated into the circuit of Nienaber. However, "[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284, 1294 (Fed. Cir. 2015) (quoting *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)); *see also In re Mouttet*, 686 F.3d at 1332 ("It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." (collecting cases)). Thus, we find Young's teaching of "programmable" delay circuits is sufficient to suggest to a person of ordinary skill that "programmable" delay circuits could be substituted, not just the precise circuit disclosed in Young. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1076 (Fed. Cir. 2015) (noting that "[a] reference must be considered for everything it teaches by way of technology and is not limited to the particular invention it is describing and attempting to protect" (quoting *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985) (emphases omitted)).

This finding rests on fundamental obviousness principles. In an obviousness analysis, we do not ignore the modifications that one skill in the art would make to a device borrowed from the prior art. *See In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1382 (Fed. Cir. 2007) (citing *Optivus*

Tech, Inc. v. Ion Beam Applications, S.A., 469 F.3d 978, 989–90 (Fed. Cir. 2006)). The evidence submitted by Patent Owner to support its construction of "programmable" and the admitted prior art in the '122 patent demonstrates not only that Young's teachings would suggest more to a person ordinary skill than Patent Owner contends, but also that it was well within the level of skill of a person of ordinary skill in this art to make any modifications necessary. *See, e.g.*, Ex. 2003 (teaching programmable delay circuit); Ex. 2004 (same); Ex. 2006 (same). Indeed, the '122 patent labels a PLL with a "programmable delay" as "conventional," (Ex. 1001, Fig. 2), and describes the "programmable delay circuit" as "conventional" (*Id.* at 3:40–41). Even though this art is not part of the combination, this art "can legitimately serve to document the knowledge that skilled artisans would bring to bear in reading the prior art identified as producing obviousness." *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015).

At bottom, Petitioner's argument is that Nienaber teaches the basic technique claimed in claim 1, albeit using analog components, and that a skilled artisan would have updated those analog components using more modern digital components, as taught in Young. The Federal Circuit routinely has found such updating to be obvious. *See Muniauction, Inc. v. Thomson Corp.*, 532 F.3d 1318, 1326–27 (Fed. Cir. 2008) ("The record in this case demonstrates that adapting existing electronic processes to incorporate modern internet and web browser technology was . . . commonplace at the time the [challenged] patent application was filed."); *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161–62 (Fed. Cir. 2007) (Obvious to combine an electro-mechanical toy with a "more

modern" toy made with electronic components "to update it using modern electronic components in order to gain the commonly understood benefits of such adaptation, such as decreased size, increased reliability, simplified operation, and reduced cost."); *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) ("[W]e have repeatedly held that an implicit motivation to combine exists . . . when the 'improvement' is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller more durable, or more efficient.").

Accepting Patent Owner's inoperability argument as proof of non-obviousness would require the type of rigid approach to determining obviousness that has been rejected repeatedly. *See Randall Mfg. Co. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013). We decline Patent Owner's invitation to ignore the full scope of teachings in Young, the prior art admitted in Patent Owner's own patent, and the background art that Patent Owner submitted showing that the replacement of one type of delay circuit for another would have been obvious to a person of ordinary skill in the art. Instead, the evidence demonstrates that the replacement of adjustable delays with programmable delays is precisely the type of upgrade based on new technology that is routine. *See Western Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1370 (Fed. Cir. 2010) ("unpatentable improvement" to replace fax machine with electronic transaction machine when "such a transition was commonplace in the art").

We conclude that a person of ordinary skill would have been motivated to combine the references. As Dr. Alpert testifies, the substitution

of programmable delay circuits such as Young's would allow the desired delay to be configured or programmed by bonding pads or serially loaded from input pads in a manner that is commonly used for a variety of features (e.g., speed selection, functional assignment of I/O pins) during integrated circuit packing assembly or initialization within a functioning system. Ex. 1010 ¶ 121. We find this articulated reasoning has rational underpinning sufficient to show that a person of ordinary skill would have been motivated to make the combination of Nienaber and Young. In sum, when viewed in the context of all the evidence—the background references, the testimony of the experts, and the admitted prior art, the evidence strongly supports the notion that the circuit Patent Owner claimed was nothing more than the "combination of familiar elements according to known methods," "each performing the same function it had been known to perform," "yield[ing] predictable results." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416–17 (2007) (quoting *Sakraida v. Ag Pro, Inc.*, 425 U.S. 273, 282 (1976)).

Thus, we find that Petitioner has established by a preponderance of the evidence that Nienaber and Young render obvious claim 1 of the '122 patent.

We also have reviewed Petitioner's contentions of obviousness under § 103(a) over Nienaber and Young against claims 2, 3, 7–10, and 14. We agree with them and base our determination on Petitioner's evidence. Therefore, we are persuaded that Petitioner has established by a preponderance of the evidence that claims 1–3, 7–10, and 14 are unpatentable as obvious over the combination of Nienaber and Young.

D. Claims 4, 12, 16, and 18: Obviousness over Nienaber, Young, and Taketoshi

Petitioner contends that claims 4, 12, 16, and 18 are unpatentable under 35 U.S.C. § 103(a) as obvious over Nienaber, Young, and Taketoshi. To support its contention, Petitioner provides a detailed showing mapping limitations of claims 4, 12, 16, and 18 to structures described by Nienaber, Young, and Taketoshi. Pet. 29–31. Petitioner also cites the Alpert Declaration for support. *See* Ex. 1010 ¶¶ 145–164.

Taketoshi (Ex. 1005)

Taketoshi, titled, "Phase Locked Loop Having Plural Selectable Voltage Controlled Oscillators," discloses a PLL-based clock generator circuit composed of a phase detector, a filter, three VCOs, a multiplexer, and a frequency divider. Ex. 1005, Abstract.

Analysis

Petitioner contends that Taketoshi discloses "a second oscillator configured to provide a second output; and a multiplexer configured to select one of the oscillator outputs as a clock output," as recited in claims 4 and 18. Pet. 30–31 (citing Ex. 1005, 4:20–24, 4:45–47, Fig. 1; Ex. 1010 ¶¶ 145–152, 161–164). Petitioner further argues that Taketoshi discloses the limitation "wherein said oscillator comprises a ring oscillator," as recited in claims 12 and 16. Pet. 31 (citing Ex. 1005, 7:36–53, Fig. 8; Ex. 1010 ¶¶ 145–147, 153–160). Petitioner further contends that Nienaber and Young disclose the remaining limitations of claims 4, 12, 16, and 18, as we determined above with respect to claims 1, 8, and 17. *Id.* at 24–29.

Petitioner argues that a person of ordinary skill would have been motivated to combine Nienaber, Young, and Taketoshi, because they relate

to similar subject matter of using delay circuits within a PLL clock circuit to adjust the amount of phase shift between the reference clock and the feedback signal. Pet. 30. Petitioner further contends that by having multiple VCOs, the "total PLL frequency variable-range is expanded" and there is "reduction of pull-time of each VCO." Pet. 30–31 (citing Ex. 1005, 1:61, 2:1–31). Petitioner further argues that modifying Nienaber with Taketoshi would have resulted in the predictable outcome of having multiple VCOs provide multiple outputs and a multiplexer that could select from multiple outputs. *Id.* at 31 (citing Ex. 1010 ¶¶ 145–152, 161–164).

Patent Owner's Response does not address claims 4, 12, 16, or 18, apart from the arguments discussed above with respect to Nienaber and Young. PO Resp. 42. We have reviewed Petitioner's contentions. We agree with them and base our determination on Petitioner's evidence. Therefore, we determine, based on the evidence and argument provided, that Petitioner has established the unpatentability of claims 4, 12, 16, and 18 as obvious over the combination of Nienaber, Young, and Taketoshi, by a preponderance of the evidence.

E. Claim 5: Obviousness over Nienaber, Young, and Kang

Petitioner contends that claim 5 is unpatentable under 35 U.S.C. § 103(a) as obvious over Nienaber, Young, and Kang. To support its contention, Petitioner provides a detailed showing mapping limitations of claim 5 to structures described by Nienaber, Young, and Kang. Pet. 31–33. Petitioner also cites the Alpert Declaration for support. *See* Ex. 1010 ¶¶ 165–169.

Kang (Ex. 1006)

Kang, titled, "Wide Band Phase Locked Loop Circuit Using Narrow Band Voltage Controlled Oscillator," discloses a wide-band frequency PLL using from a narrow band VCO. Ex. 1006, Abstract. Kang further discloses using a variable frequency divider to generate a reference signal by dividing the signal generated from the VCO. *Id.*

Analysis

Petitioner contends that Kang discloses a circuit "wherein the logic circuit is further configured to select an input for the feedback path from at least two of the oscillator output, the divider output, and the clock output," as recited in claim 5. Pet. 31–33 (citing Ex. 1006, 3:5–11, 4:3–26, Figs. 2, 4; Ex. 1010 ¶¶ 165–169). Petitioner further contends that Nienaber and Young disclose the remaining limitations of claim 5, as we determined above with respect to claims 1 and 3. Pet. 24–29. Petitioner argues that a person of ordinary skill would have been motivated to combine Nienaber, Young, and Kang, because they relate to similar subject matter, and that adding the narrow-band VCO, divider, and multiplexer of Kang to the reference path of Nienaber would have yielded a predictable result that would have allowed a PLL circuit to support various duty cycles. Pet. 33 (citing Ex. 1010 ¶¶ 164–169).

Patent Owner's Response does not address claim 5, apart from the arguments discussed above with respect to Nienaber and Young. PO Resp. 42. We have reviewed Petitioner's contentions. We agree with them and base our determination on Petitioner's evidence. Therefore, we determine, based on the evidence and argument provided, that Petitioner has

established the unpatentability of claim 5 as obvious over the combination of Nienaber, Young, and Kang by a preponderance of the evidence.

F. Claim 6: Obviousness over Nienaber, Young, Kang, and Sutardja

Petitioner contends that claim 6 is unpatentable under 35 U.S.C. § 103(a) as obvious over Nienaber, Young, Kang, and Sutardja. To support its contention, Petitioner provides a detailed showing mapping limitations of claim 6 to structures described by Nienaber, Young, Kang, and Sutardja. Pet. 33–34. Petitioner also cites the Alpert Declaration for support. *See* Ex. 1010 ¶¶ 170–175.

Sutardja (Ex. 1007)

Sutardja, titled, "Charge Pump for Phase Lock Loop," describes a PLL circuit including a reference counter that receives a reference clock, and a feedback counter that receives the output oscillation signal of a VCO. Ex. 1007, 4:54–59.

Analysis

Petitioner contends that Sutardja discloses a circuit "wherein the reference path further comprises a reference counter receiving the reference clock input providing said reference signal therefrom, and the feedback path further comprises a feedback counter receiving the feedback path input providing said feedback signal therefrom," as recited in claim 6. Pet. 33–34 (citing Ex. 1007, 4:54–59, 5:9–11, Fig. 1; Ex. 1010 ¶¶ 170–175). Petitioner further contends that Nienaber, Young, and Kang disclose the remaining limitations of claim 6, as we determined above with respect to claim 5. Pet. 31–34. Petitioner argues that a person of ordinary skill would have been motivated to combine Nienaber, Young, Kang, and Sutardja because they

relate to similar subject matter, and modifying Nienaber to include the counter of Sutardja in the reference and feedback paths to divide the frequencies of the reference and feedback signals and would have yielded a predictable result. Pet. 34 (citing Ex. 1010 ¶¶ 170–175).

Patent Owner's Response does not address claim 6, apart from the arguments discussed above with respect to Nienaber and Young. PO Resp. 42. We have reviewed Petitioner's contentions. We agree with them and base our determination on Petitioner's evidence. Therefore, we determine, based on the evidence and argument provided, that Petitioner has established the unpatentability of claim 6 as obvious over the combination of Nienaber, Young, Kang, and Sutardja by a preponderance of the evidence.

G. Claims 4 and 13: Obviousness over Nienaber, Young, and Ferraiolo

Petitioner contends that claims 4 and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Nienaber, Young, and Ferraiolo. To support its contention, Petitioner provides a detailed showing mapping limitations of claims 4 and 13 to structures described by Nienaber, Young, and Ferraiolo. Pet. 35–36. Petitioner also cites the Alpert Declaration for support. *See* Ex. 1010 ¶¶ 177–182.

Ferraiolo (Ex. 1008)

Ferraiolo, titled, "Variable-Speed Phase-Locked Loop System with on-the-fly Switching and Method Therefor," describes a clock generation circuit that uses two PLLs to allow the circuit to switch the frequency of the output clock without the delay or disruption if only a single PLL were used. Ex. 1008, 1:61–2:4.

Analysis

Petitioner contends that Ferraiolo discloses "a second oscillator configured to provide a second output; and a multiplexer configured to select one of the oscillator output as a clock output," as recited in claim 4. Pet. 35–36 (citing Ex. 1008, 3:10–27, Fig. 2; Ex. 1010 ¶¶ 177–182). Petitioner asserts that Ferraiolo discloses "wherein said second oscillator further comprises a phase locked loop," as recited in claim 13. Pet. 35–36 (citing Ex. 1008, Fig. 2; Ex. 1010 ¶¶ 177–182). Petitioner further submits that Nienaber and Young disclose the remaining limitations of claims 4 and 13, as we determined above with respect to claim 1. Pet. 24–27. Petitioner argues that a person of ordinary skill would have been motivated to combine Nienaber, Young, and Ferraiolo because they relate to similar subject matter, and that modifying Nienaber to include an additional PLL, as shown in Ferraiolo, would obtain a predictable result of being able to select from an additional PLL and to change frequency instantly without disturbance. Pet. 36 (citing Ex. 1010 ¶¶ 177–182). This is also consistent with the disclosure in Figure 2 of the '122 patent that the "Conventional PLL" portion includes a multiplexer that receives a signal "FROM ANOTHER PLL." Ex. 1001, Fig. 2.

Patent Owner's Response does not address claims 4 or 13, apart from the arguments discussed above with respect to Nienaber and Young. PO Resp. 42. We have reviewed Petitioner's contentions. We agree with them and base our determination on Petitioner's evidence. Therefore, we determine, based on the evidence and argument provided, that Petitioner has established the unpatentability of claims 4 and 13 as obvious over the

combination of Nienaber, Young, and Ferraiolo by a preponderance of the evidence.

H. Claim 19: Obviousness over Nienaber, Young, Taketoshi, and Kang

Petitioner contends that claim 19 is unpatentable under 35 U.S.C. § 103(a) as obvious over Nienaber, Young, Taketoshi, and Kang. To support its contention, Petitioner provides a detailed showing mapping limitations of claim 19 to structures described by Nienaber, Young, Taketoshi, and Kang. Pet. 36–37. Petitioner also cites the Alpert Declaration for support. *See* Ex. 1010 ¶¶ 183–185.

Analysis

Claim 19 depends from claim 18. As discussed above, Petitioner has shown sufficiently that the combination of Nienaber, Young, and Taketoshi account for the limitations of claim 18. Pet. 30–31. In particular, Petitioner contends that Young discloses "selecting a characteristic or predetermined delay for the programmable amount of time," as recited in claim 19. Pet. 36, 27–28 (citing Ex. 1004, 3:67–4:51; Ex. 1010 ¶¶ 122–126). Petitioner also asserts that Kang discloses "selecting an input for a feedback path from at least two of (i) one of the oscillator outputs, (ii) the divided output, and (iii) the clock output," as recited in claim 19. Pet. 31–33, 37; Ex. 1006, 3:5–12, 4:3–26, Figs. 2, 4; Ex. 1010 ¶¶ 165–169, 183–185. Petitioner further contends that Nienaber, Young, and Taketoshi disclose the remaining limitations of claim 19, as we determined above with respect to claim 18. Pet. 29–31. Petitioner argues that a person of ordinary skill would have been motivated to combine Nienaber, Young, Taketoshi, and Kang because Taketoshi enables varied output frequencies, and Kang enables selection

from a divided version of the output. Pet. 37. The combination, thus, would allow the phase-lock controller to operate over a small frequency range as the output frequency is varied. *Id.* (citing Ex. 1010 ¶¶ 183–185).

Patent Owner's Response does not address claim 19, apart from the arguments discussed above with respect to Nienaber and Young. PO Resp. 42. We have reviewed Petitioner's contentions. We agree with them and base our determination on Petitioner's evidence. Therefore, we determine, based on the evidence and argument provided, that Petitioner has established the unpatentability of claim 19 as obvious over the combination of Nienaber, Young, Taketoshi, and Kang by a preponderance of the evidence.

I. Claim 20: Obviousness over Nienaber, Young, Taketoshi, Kang, and Sutardja

Petitioner contends that claim 20 is unpatentable under 35 U.S.C. § 103(a) as obvious over Nienaber, Young, Taketoshi, Kang, and Sutardja. To support its contention, Petitioner provides a detailed showing mapping limitations of claim 20 to structures described by Nienaber, Young, Taketoshi, Kang, and Sutardja. Pet. 37–38. Petitioner also cites the Alpert Declaration for support. *See* Ex. 1010 ¶¶ 187–189.

Analysis

Petitioner contends that, similar to the discussion with respect to claim 6, Sutardja discloses the limitation of "wherein said method further comprises the steps of: providing a reference signal generated by a reference counter receiving the reference input; and providing a feedback signal generated by a feedback counter receiving the feedback path input," as recited in claim 20. *Id.* at 33–34 (citing Ex. 1007, 4:54–59, 5:9–11,

Fig. 1; Ex. 1010 ¶¶ 170–175). Petitioner further submits that Nienaber, Young, Taketoshi, and Kang disclose the remaining limitations of claim 20, as we determined above with respect to claim 19. Pet. 36–37.

Petitioner contends that a person of ordinary skill would have been motivated to modify Nienaber to include the counter of Sutardja in the reference and feedback paths to divide the frequencies of the reference and feedback signals, and that such modification would have yielded a predictable result. Pet. 34 (citing Ex. 1010 ¶¶ 170–175).

Patent Owner's Response does not address claim 20, apart from the arguments discussed above with respect to Nienaber and Young. PO Resp. 42. We have reviewed Petitioner's contentions. We agree with them and base our determination on Petitioner's evidence. Therefore, we determine, based on the evidence and argument provided, that Petitioner has established the unpatentability of claim 20 as obvious over the combination of Nienaber, Young, Taketoshi, Kang, and Sutardja by a preponderance of the evidence.

III. CONCLUSION

We determine that Petitioner has shown by a preponderance of the evidence that claims 1–10, 12–14, and 16–20 of the '122 patent are unpatentable based on the following grounds:

1. Claims 1–3, 7–10, 14, and 17 as obvious under 35 U.S.C. § 103(a) over Nienaber and Young;
2. Claims 4, 12, 16, and 18 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, and Taketoshi;

3. Claim 5 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, and Kang;
4. Claim 6 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, Kang, and Sutardja;
5. Claims 4 and 13 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, and Ferraiolo;
6. Claim 19 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, Taketoshi, and Kang; and
7. Claim 20 as obvious under 35 U.S.C. § 103(a) over Nienaber, Young, Taketoshi, Kang, and Sutardja.

IV. ORDER

For the reasons given, it is:

ORDERED that claims 1–10, 12–14, and 16–20 of the ’122 patent have been shown to be *unpatentable*; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

For Petitioner:

David B. Cochran
Joseph M. Sauer
Joshua R. Nightingale
dcochran@jonesday.com
jmsauer@jonesday.com
jrnightingale@jonesday.com

For Patent Owner:

Matthew C. Phillips
Steve A. Wong
Himanshu S. Amin
matthew.phillips@renaissanceiplaw.com
swong@thepatentattorneys.com
hamin@thepatentattorneys.com