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Paper 32
Entered: April 14, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG SEMICONDUCTOR, INC., and
SAMSUNG AUSTIN SEMICONDUCTOR LLC,
Petitioner[1],

v.

HOME SEMICONDUCTOR CORPORATION,
Patent Owner.

Case IPR2015-00459
Patent 6,150,244

Before JONI Y. CHANG, JON B. TORNQUIST, and BETH Z. SHAW, *Administrative Patent Judges.*

CHANG, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

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[1] Samsung Telecommunications America LLC, originally a real party-in-interest at the time of filing the Petition, no longer exists as a separate corporate entity, because it has merged with and into Samsung Electronics America, Inc. Paper 9.

I. INTRODUCTION

Samsung Electronics Co. Ltd., Samsung Electronics America Inc., Samsung Semiconductor Inc., and Samsung Austin Semiconductor LLC (collectively "Samsung"), filed a Petition requesting an *inter partes* review of claims 1–20 of U.S. Patent No. 6,150,244 (Ex. 1001, "the '244 patent"). Paper 1 ("Pet."). Patent Owner, Home Semiconductor Corporation ("HSC"), did not file a Preliminary Response. Upon consideration of the Petition, we determined that there was a reasonable likelihood that Samsung would prevail with respect to at least 1 of the challenged claims. Pursuant to 35 U.S.C. § 314(a), we instituted this trial as to claims 1–20 of the '244 patent. Paper 11 ("Dec.").

After institution, HSC filed a Patent Owner Response (Paper 18, "PO Resp."), and Samsung filed a Reply to the Patent Owner Response (Paper 21, "Reply"). An oral hearing was held on February 25, 2016.[2]

We have jurisdiction under 35 U.S.C. § 6(c). This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). For the reasons set forth below, we conclude that Samsung has demonstrated by a preponderance of the evidence that claims 1–20 of the '244 patent are unpatentable.

[2] The oral hearings for this trial and the following cases were consolidated: Cases IPR2015-00460, IPR2015-00466, and IPR2015-00467. Paper 30. A transcript of the hearing has been entered into the record as Paper 31 ("Tr.").

A. Related Matter

Samsung indicates that the ’244 patent is asserted in *Home Semiconductor Corp. v. Samsung Electronics Co. Ltd.*, No. 1:13-cv-02033-RGA (D. Del.). Pet. 1.

B. The ’244 Patent

The ’244 patent discloses a method for fabricating a metal-oxide semiconductor (MOS) transistor. Ex. 1001, 3:56–67. According to the ’244 patent, the MOS transistor has a gate electrode and raised source and drain electrodes. *Id*. The gate electrode is formed before the raised source and drain electrodes, and the definition of the raised source and drain does not rely on the use of a single lithographic step. *Id*. Figure 7 of the ’244 patent, reproduced below, illustrates a cross-sectional view of a MOS transistor.

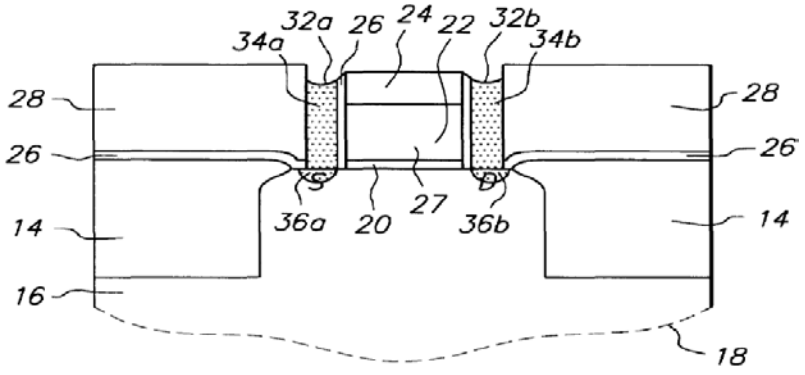

FIG. 7

As show in Figure 7, a transistor is formed on a semiconductor substrate in lightly doped well region 16 having profile 18, which is located between isolation regions 14. *Id*. at 4:1–6:26. The transistor has: (1) gate electrode 27 having first dielectric layer 20, first conductor layer 22, second

dielectric layer 24, and third dielectric layer 26; (2) raised source and drain electrodes 34a and 34b; and (3) raised source 36a and drain 36b. *Id*.

C. Illustrative Claim

Claims 1, 14, and 16 are independent. Claims 2–13 depend ultimately from claim 1; claim 15 depends directly from claim 14; and claims 17–20 depend, directly or indirectly, from claim 16. Claim 1 reads as follows:

> 1. A process of fabricating on a substrate a semiconductor device *having a raised source, a raised drain* and a gate electrode structure, comprising the steps of:
>
> forming a plurality of isolation regions on said substrate to isolate a plurality of active regions;
>
> forming sequentially a first dielectric layer, a first conductor layer and a second dielectric layer on said substrate;
>
> forming on one of said active regions a patterned first resist layer to mask a portion of said second dielectric layer and the underlying first conductor layer and first dielectric layer;
>
> removing said second dielectric layer, said first conductor layer and said first dielectric layer other than said portion masked by said first resist layer to form said gate electrode structure;
>
> depositing sequentially a third dielectric layer and a fourth dielectric layer on said substrate and said gate electrode structure;
>
> removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure;
>
> forming on the substrate a patterned second resist layer to mask portions of the fourth dielectric layer;
>
> removing said fourth dielectric layer other than said portions masked by said second resist layer to form a plurality of trenches

> adjacent to said gate electrode structure, wherein portions of the substrate are exposed, and *wherein spacers are formed on sidewalls of the gate electrode structure at the same time*;
>
> filling said plurality of trenches with a second conductor layer, doping said second conductor layer in the trenches with dopants; and
>
> driving said dopants into the substrate underneath said trenches to form said raised source and said raised drain.

Ex. 1001, 6:28–65 (emphases added).

D. Prior Art Relied Upon

Samsung relies upon the following prior art references:

Shunji Nakamura, U.S. Patent No. 6,312,994 B1, issued on November 6, 2001 (Ex. 1004, "Nakamura").

A. MUKHERJEE, INTRODUCTION TO nMOS AND CMOS VLSI SYSTEMS DESIGN 11, 12, 119–39, 341 (Prentice Hall 1986) (Ex. 1005, "Mukherjee").[3]

R.S. MULLER AND T.I. KAMINS, DEVICE ELECTRONICS FOR INTEGRATED CIRCUITS 66, 67, 74–79, 257–62 (John Wiley & Sons, 2d ed. 1986) (Ex. 1006, "Muller").

R.F. PIERRET, SEMICONDUCTOR DEVICE FUNDAMENTALS 146–73, 608–39 (Addison-Wesley Publishing Company 1996) (Ex. 1007, "Pierret").

S. WOLF AND R.N. TAUBER, SILICON PROCESSING FOR THE VLSI ERA, VOLUME 1 – PROCESS TECHNOLOGY 307–08 (Lattice Press 1986) (Ex. 1008, "Wolf").

S.K. GHANDHI, VLSI FABRICATION PRINCIPLES – SILICON AND GALLIUM ARSENIDE 427–29 (John Wiley & Sons, Inc. 1983) (Ex. 1012, "Ghandhi").

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[3] All references to the page numbers of Exhibits 1005–1008 and 1012 refer to the original page numbers of the Exhibit on either the upper left or right corner, and not the exhibit page number on the bottom center of the page.

E. Instituted Grounds of Unpatentability

We instituted the instant trial based on the following grounds of unpatentability (Dec. 20):

Challenged Claim(s)	Basis	References
1, 9, 11, 12, 14–16, 19, and 20	§ 103(a)	Nakamura and Muller
2–4, 6–8, 17, and 18	§ 103(a)	Nakamura, Muller, and Mukherjee
5	§ 103(a)	Nakamura, Muller, and Wolf
10	§ 103(a)	Nakamura, Muller, and Ghandhi
13	§ 103(a)	Nakamura, Muller, and Pierret

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). In that regard, the terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the Specification. *In re Translogic Tech., Inc*., 504 F.3d 1249, 1257 (Fed. Cir. 2007). Further, "limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

In this proceeding, the parties propose constructions for the following: "raised source," "raised drain," "removing a top portion," "at the same time," and order of method steps.

"raised source" and "raised drain"

Claim 1 recites "fabricating on a substrate a semiconductor device having *a raised source, a raised drain* and a gate electrode structure." Ex. 1001, 6:28–30 (emphasis added). Samsung proposes to construe the claim terms "raised source" and "raised drain" to encompass "a source and drain formed, at least in part, by diffusing dopant ions into a substrate surface via doped material formed at the surface regions of a substrate where the source and the drain are to be formed." Pet. 6.

In the Decision on Institution, we adopted Samsung's proposed constructions in light of the Specification, as they are consistent with the broadest reasonable construction. Dec. 8; Pet. 5–6 (citing Ex. 1001, 1:39–49; 5:63–6:10). Subsequent to institution, HSC does not challenge any aspect of the claim constructions as to these terms. PO Resp. 9–29. Upon review of the present record, we discern no reason to change our claim constructions for these terms for purposes of this Final Written Decision.

"removing a top portion"

Claim 1 recites "removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure." Ex. 1001, 6:48–50. Claim 14 recites a similar limitation. *Id*. at 7:47–49. Samsung interprets this limitation to require no more than *making*

a hole through a top portion of the fourth dielectric layer to expose a portion of the underlying third dielectric layer covering the gate electrode structure. Pet. 28–29. HSC disagrees and proposes essentially to construe "removing a top portion" to require *planarizing* the entire top surface of the fourth dielectric layer across the wafer, in addition to *making a hole* through the fourth dielectric layer to expose a portion of the third dielectric layer. PO Resp. 10–14. As support, HSC cites to the following portion of the Specification:

> The top portion of the fourth dielectric layer 28 is then *planarized by a planarization process*, e.g., chemical mechanical polishing (CMP), until the third dielectric layer 26 covering the top of the gate electrode structure is exposed as shown in FIG. 4.

Ex. 1001, 5:6–10 (emphasis added).

HSC's proposed construction, however, would import improperly a limitation—"planarized by a planarization process"—from a preferred embodiment disclosed in the Specification into claims 1 and 14. *See Superguide Corp. v. DirecTV Enters., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) ("Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim."); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (expressly rejecting "the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment").

HSC does not allege, nor do we discern, that there is a definition set forth in the Specification to give the disputed term a special meaning. *See In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (stating that an inventor may rebut the presumption that claim terms are given their ordinary and customer meaning by providing a definition of the term in the specification with reasonable clarity, deliberateness, and precision). Significantly, the Specification uses the term "removing" in a broader description of the claimed process—"removing the top portion of the second dielectric layer to expose the portion of the first dielectric layer that covers the gate electrode structure." Ex. 1001, Abs. As Samsung also notes, the Specification uses the words "removing" and "portion" to refer to the removal of only a portion of material and not the removal of the top surface across the entire wafer. Reply 4–5; Ex. 1001, 5:28–30 ("This anisotropic process also removes the portion of the third dielectric layer 26 on top of the gate electrode structure."). Therefore, the Specification does not support HSC's proposed claim construction that imports a "planarizing" limitation from a preferred embodiment into claims 1 and 14.

Nor does the plain meaning of the claim language support HSC's position. Claims 1 and 14 use "removing," whereas claim 16 uses "planarizing" for the same limitation—"*planarizing* a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure," Ex. 1001, 8:26–28 (emphasis added). There is an inference that "two different terms used in a patent have different meanings." *Comaper Corp. v. Antec, Inc.*, 596 F.3d 1343, 1348 (Fed. Cir.

2010). Indeed, the plain meaning of the term "removing" does not necessarily mean "planarizing." As HSC and its expert acknowledge, "planarizing" or "planarization" is a special type of etching process—chemical mechanical polishing—that flattens or smooths the entire surface of the wafer. PO Resp. 11–12; Ex. 2002 ¶¶ 37, 38. Nothing in the language of claims 1 and 14 requires the entire top surface of the dielectric layer to be flattened or smoothed. Interpreting "removing" as "planarizing" would exclude other well-known etching processes, such as isotropic and anisotropic etches. Moreover, HSC does not construe other claim limitations that use the term "removing" as "planarizing"—e.g., "removing said fourth dielectric layer other than said portions masked by said second resist layer to form a plurality of trenches" (Ex. 1001, 6:52–55, 7:47–49). Thus, HSC's proposed claim construction for "removing a top portion" is inconsistent with other claim limitations.

We also are not persuaded by HSC's argument that the phrase "top portion" refers to the entire top portion of the dielectric layer across the wafer, and the removal of this portion occurs wafer-wide. PO Resp. 10. As Samsung notes, the plain meaning of the term "portion" is "a part of a whole." Reply 4; Ex. 1015, 1412. Moreover, HSC's interpretation of "top portion" still would not require the dielectric layer be flattened or smoothed.

In that light, we find that the plain meanings of the claim terms do not require us to interpret "removing" as "planarizing," or interpret "a top portion" as the *entire* top portion of the dielectric layer *across* the

semiconductor wafer, as alleged by HSC. In short, HSC's construction is not consistent with the plain meanings of the claim terms.

We also are not persuaded by HSC's argument and expert testimony that "[i]f only a portion of the top surface were removed, the process would not result in a functioning device," as they are predicated on the notion that a resist layer cannot be formed on a non-planarized surface, and that the deposition of the fourth dielectric layer produces an uneven surface. PO Resp. 14; Ex. 2002 ¶ 41. HSC, however, fails to provide credible evidence to show that forming a resist layer on a non-planarized surface would not produce a functional device. Although Mr. Maltiel's testimony discusses the benefits of forming a resist layer on a planarized surface, as shown in the preferred embodiment, nothing in the "Description of the Prior Art" Section of the Specification indicates that the prior art devices were defective and non-functional devices. Ex. 1001, 1:11–2:9. Nor does Mr. Maltiel provide data or other objective evidence to support his assertion that forming a resist layer on a non-planarized surface would produce "a defective and non-functional device." Ex. 2002 ¶ 41. Moreover, neither HSC nor Mr. Maltiel explains sufficiently why it is necessary to planarize the surface during the "removing" step. As evidenced by Nakamura, one of ordinary skill in the art would recognize that the fourth dielectric layer may be deposited by spin on glass, which produces a planarized surface. *See* Ex. 1004, 10:6–9, Fig. 1C. Mr. Maltiel's testimony is entitled little, if any, weight, as it is inconsistent with the prior art of record. *See* 37 C.F.R. § 42.65(a) ("Expert testimony

that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

We further note that patent claims have a presumption of validity in a district court proceeding. In contrast, there is no presumption of validity here in an *inter partes* review, and, therefore, we do not apply a rule of construction with an aim to preserve the validity of claims. HSC essentially asks us to rewrite the claims to add a planarization step. Our reviewing court "repeatedly and consistently has recognized that courts may not redraft claims, whether to make them operable or to sustain their validity." *Rembrandt Data Techs., LP v. AOL, LLC*, 641 F.3d 1331, 1339 (Fed. Cir. 2011) (citing *Chef Am., Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004)). We recognize that courts sometimes can correct "a patent if (1) the correction is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims." *Id*. (citing *Novo Industries, L.P. v. Micro Molds Corp.*, 350 F.3d 1348, 1357 (Fed. Cir. 2003)). Here, the correction suggested by HSC is not minor, obvious, free from reasonable debate or evident from the prosecution history. As such, we decline to rewrite the claims to add a planarization step.

In view of the foregoing, we decline to adopt HSC's proposed claim construction. Rather, in light of the Specification, we agree with Samsung that the aforementioned "removing" limitations recited in claims 1 and 14 require no more than *making a hole* through a top portion of the fourth

dielectric layer to expose a portion of the third dielectric layer covering the gate electrode structure. Pet. 28–29.

"*at the same time*"

Claims 1 and 16 recite:

> [1] *removing said fourth dielectric layer* other than said portions masked by said second resist layer to form a plurality of trenches adjacent to said gate electrode structure, [2] *wherein* portions of the substrate are exposed, and [3] *wherein* spacers are formed on sidewalls of the gate electrode structure *at the same time*;

Ex. 1001, 6:53–58, 8:32–37 (emphases and bracketed numbers added). Claim 14 requires similar steps. *Id*. at 7:47–52. In this regard, the parties' dispute centers on whether all three steps must occur at the same time. Pet. 6–12; PO Resp. 14–21; Reply 5–10. In the Decision on Institution, we determined that, in light of the Specification, they do not. Dec. 9.

After institution, HSC argues that the "wherein" clauses describe additional results that occur during the recited step for "removing said fourth dielectric layer." PO Resp. 16. In particular, HSC contends that the limitation requires a *single process step*, in which, using a patterned resist layer as a mask, the unmasked portions of the fourth dielectric layer are removed, while the masked portions are not removed, during which all of the following results must occur *at the same time*: (1) forming the *trenches* that extend down to the substrate surface, adjacent the gate electrode structure; (2) exposing portions of the *substrate*; and (3) forming *spacers* on the sidewalls of the gate electrode. *Id*. at 16–17, 43. As support, HSC directs our attention to Mr. Maltiel's testimony. Ex. 2002 ¶¶ 47–52.

HSC's proposed claim construction, however, would import a number of extraneous limitations into the claims. "It is improper for a court to add 'extraneous' limitations to a claim, that is, limitations added 'wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim.'" *Hoganas AB v. Dresser Indus., Inc.*, 9 F.3d 948, 950 (Fed. Cir. 1993) (citing *E.I. Du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988)). Neither the claim language nor the Specification supports HSC's proposed claim construction.

It is unquestionable that the recited "removing" step only removes the fourth dielectric layer, and *not* the third dielectric layer. Prior to the "removing" step, each independent claim recites "depositing sequentially a third dielectric layer and a fourth dielectric layer on said substrate and said gate electrode structure." *See, e.g.*, Ex. 1001, 6:44–47. Therefore, exposing portions of the substrate and forming spacers are not the results of removing the fourth dielectric layer. Rather, they are the results of removing the third dielectric layer, which is *not* recited in the claims. Without removing the portions of the third dielectric layer that are directly on the substrate, none of the following results identified by HSC would occur: (1) exposing portions of the substrate; (2) forming trenches that extend down to the substrate; and (3) forming spacers on the sidewalls of the gate electrode. Ex. 1001, 4:62–5:9, Fig. 4. Also, nothing in the claims requires the trenches to extend down to the substrate, as suggested by HSC. PO Resp. 43.

Even if we were to interpret the claims to require a step of removing the third dielectric layer to expose portions of the substrate and forms

spacers, such a step would occur *subsequent* to, not at the same time as, the step for removing the fourth dielectric layer. Ex. 1001, 4:62–5:44, Fig. 4. That is because the portions of the third dielectric layer that are directly on the substrate are underneath the fourth dielectric layer, and the step for removing the fourth dielectric layer is anisotropic for forming the trenches. *Id*. Those portions of the third dielectric layer cannot be removed until the fourth dielectric layer over the contact regions is removed. *Id*. As such, we are not persuaded by HSC's arguments that all three results identified by HSC must occur at the same time during a single process step for etching the fourth dielectric layer.

HSC also relies on Mr. Maltiel's testimony that HSC's construction is consistent with the Specification, and that the Specification "makes clear that this same etching step also etches the third dielectric layer." Ex. 2002 ¶¶ 47–52. Mr. Maltiel's testimony, however, conflates different portions of the third dielectric layer, and conflates "process" with "step." *Id*.

Figure 4 of the '244 patent is reproduced below with our highlights and Samsung's annotations in red added:

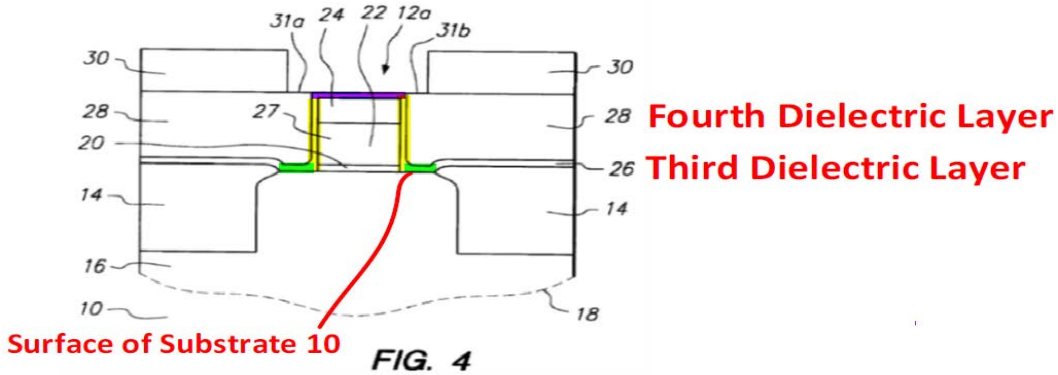


FIG. 4

As shown by annotated Figure 4 above, third dielectric layer 26 has the following portions in the device area: green portions which are directly on *substrate* 10; yellow portions which are directly on the *sidewalls of gate* electrode 27; and a purple portion which is on the *top of gate* electrode 27. Ex. 1001, 4:62–5:10. Fourth dielectric layer 28 is on the green and yellow portions, but *not* on the purple portion, of third dielectric layer 26. *Id*. Patterned resist layer 30 exposes region 12a, including portions of fourth dielectric layer 28 over the contact regions, and the purple portion of third dielectric layer 26. *Id*. at 5:11–24.

The passage of the Specification relied on by Mr. Maltiel's testimony is directed to the portion of the third dielectric layer that is on the top of the *gate electrode structure* (shown as purple in the annotated Figure 4 above), and *not* the portions of the third dielectric layer that are directly on *the substrate* (shown as green in the annotated Figure 4 above). Ex. 2002 ¶¶ 47–52 (citing Ex. 1001, 5:28–30 ("This anisotropic *process* also removes the portion of the third dielectric layer 26 on top of the *gate electrode structure 27*." (emphases added))). As shown in annotated Figure 4 above, the green portions of third dielectric layer 26 are underneath fourth dielectric layer 28, and therefore, the green portions of third dielectric layer 26 would not be exposed to the etchant until the portions of fourth dielectric layer 28 over the contact regions are removed. *Id*. at 5:25–44, Fig. 4.

Further, according to the Specification, the third dielectric layer is "an etch-stop layer." *Id*. at 4:66–5:1. Other than Figure 5 that shows the third dielectric layer is no longer on the substrate in the contact regions, the

Specification is silent as to removing the portions of the third dielectric layer that are directly on the substrate. *Id*. Even in the Abstract and Summary of the Invention section, the Specification does not disclose removing those portions of the third dielectric layer. *Id*. at Abs., 2:12–64. Nor does the Specification explain when or how those portions of the third dielectric layer are removed, let alone removing them in the same etching *step* for removing the fourth dielectric layer. *Id*. In fact, the Specification describes that the structure shown in Figure 5 is "a result of an anisotropic etching *process*." Ex. 1001, 5:25–36 (emphasis added). Nothing in the Specification indicates *a single step* for removing both the third and fourth dielectric layers over the contact regions, as asserted by Mr. Maltiel and HSC. *Id*.

In light of the foregoing, Mr. Maltiel's testimony (Ex. 2002 ¶¶ 47–52) is not supported by the Specification. As a result, we give little, if any, weight to Mr. Maltiel's testimony. *See* 37 C.F.R. § 42.65(a); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (en banc) ("We have viewed extrinsic evidence in general as less reliable than the patent and its prosecution history in determining how to read claim terms . . . . Third, extrinsic evidence consisting of expert reports and testimony is generated at the time of and for the purpose of litigation and thus can suffer from bias that is not present in intrinsic evidence.").

HSC's reliance on *Griffin v. Bertina* is misplaced. 285 F.3d 1029, 1033 (Fed. Cir. 2002) (finding that the "wherein clauses . . . relate back to and clarify what is required by the [claim element]"). As Samsung points out, in *Griffin*, the claim language within the "wherein" clauses referred

back to the claim element recited in that previous step. Reply 8. For instance, in *Griffin*, the claim recites "*assaying* for the presence of a *point mutation*," and the "wherein" clauses each explicitly referred back to the recited point mutation—"*wherein said point mutation correlates . . .* " and "*wherein the presence of said point mutation* in said test nucleic acid indicates . . . ." *Griffin*, 285 F.3d at 1031 (emphases in the original). Thus, in *Griffin*, the wherein clauses explicitly related back to a previously recited claim element. Here, there is no such antecedent reference tying the "wherein" clauses back to the "removing" step. Importantly, as discussed above, exposing the substrate and forming spacers are not the result of the recited "removing" step, which only removes the fourth dielectric layer. Rather, they are the result of an additional step that is *not* recited in the claims—removing the portions of the third dielectric layer.

The claim term "at the same time" is recited only in "wherein *spacers* are formed on sidewalls of the gate electrode structure *at the same time*." Figure 5 of the '244 patent is reproduced below with annotations and highlights added by Samsung, Pet. 11.

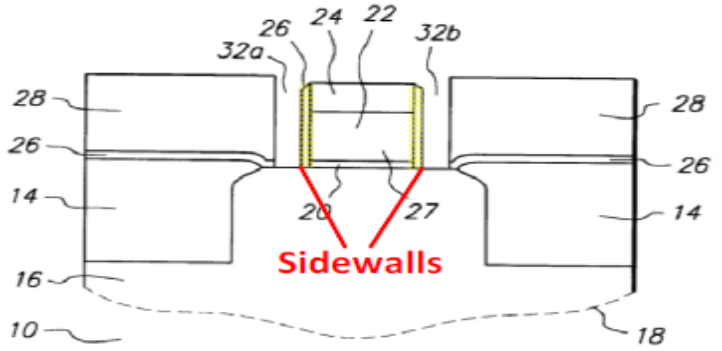


FIG. 5

As depicted in annotated Figure 5 of the ’244 patent above, spacers (shown in yellow highlights) on the sidewalls of gate electrode structure 27 are formed by: (1) depositing third dielectric layer 26, (2) removing portions of fourth dielectric layer 28 at the contact regions, and (3) removing portions of third dielectric layer 26 in the device area that are not on the sidewall of the gate electrode (the green and purple portions of third dielectric layer 26 shown in annotated Figure 4 reproduced previously). Ex. 1001, 5:25–36. Therefore, the step of forming the spacers does not occur at the same time as the step for removing portions of the fourth dielectric layer, as alleged by HSC. The term “at the same time” simply applies to the formation of the multiple spacers in the last “wherein” clause.

In light of the claim language and Specification, we decline to adopt HSC’s proposed claim construction. Rather, we construe “at the same time” to require only that the spacers are formed at the same time as each other.

“order of the steps”

> Claim 1 recites the following method steps:
>
> [1] removing a top portion of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure; [and]
>
> [2] forming on the substrate a patterned second resist layer to mask portions of the fourth dielectric layer;

Ex. 1001, 6:48–52 (bracketed matters added). Claim 14 recites similar method steps. *Id.* at 7:41–45.

Samsung argues that the claims do not require Steps 1 and 2 (reproduced above) be performed in the order written. Pet. 12. In the

Decision on Institution, we adopted Samsung's proposed construction as our own, as we found that it was consistent with the broadest reasonable interpretation of the claims in light of the Specification. Dec. 10.

After institution, HSC argues that a relevant skilled artisan, reading the claims, would have understood that the limitations are arranged in a specific logical order and must be performed in sequence because, in part, the claims are directed to semiconductor fabrication. PO Resp. 22. HSC maintains that reversing the order of Steps 1 and 2 is "impossible from a practical standpoint" because the top portion of the fourth dielectric layer is removed by planarization process that creates a flat surface, and the photoresist is formed on that planarized flat surface. *Id*. at 25. HSC also alleges that our claim construction would exclude the preferred embodiment. *Id*. at 27. HSC further contends that reversing the order of Steps 1 and 2 would render one of the "removing" steps superfluous. *Id*. at 27–28.

There is no *per se* rule that method steps for fabricating a semiconductor device must be performed in the order written. *See Loral Fairchild Corp. v. Song Corp.*, 181 F.3d 1313, 1322 (Fed. Cir. 1999) (In deciding whether the claimed steps for fabricating a semiconductor device must be performed in the order as written, the court noted that "not every process claim is limited to the performance of its steps in the order written."). In fact, it is well settled that "[u]nless the steps of a method actually recite an order, the steps are not ordinarily construed to require one." *Interactive Gift Exp., Inc. v. Compuserve Inc*., 256 F.3d 1323, 1343 (Fed. Cir. 2001). We are mindful that "a claim requires an ordering of steps

when the claim language, as matter of logic or grammar, requires that the steps be performed in the order written, or the specification directly or implicitly requires an order of steps." *Mformation Techs., Inc. v. Research In Motion Ltd.*, 764 F.3d 1392, 1398–99 (Fed. Cir. 2014).

Here, nothing in the claims or Specification directly or implicitly requires a narrow construction, requiring Steps 1 and 2 to be performed in the order written. For instance, there is no claim language that imposes a temporal restriction on the steps. Step 2 does not reference something (e.g., a product or result of Step 1) indicating Step 1 had been performed.

HSC's proposed construction would import improperly a limitation from a preferred embodiment into the claims, imposing a specific order of steps. *See Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1370–71 (Fed. Cir. 2003) (holding that, although the specification discussed only a single embodiment, it was improper to read a specific order of steps into method claims where, as a matter of logic or grammar, the language of the method claims did not impose a specific order on the performance of the method steps, and the specification did not directly or implicitly require a particular order). As Samsung notes, the preferred embodiment cited by HSC includes language (e.g., "next" and "is then") requiring a specific order of steps, but the claims do *not* recite that language. *Compare* Ex. 1001, 4:62–5:27 ("The top portion of the fourth dielectric layer 28 *is then* planarized by a planarization process, e.g., chemical mechanical polishing . . . . *Next*, a second resist layer 30 is deposited on top of the fourth dielectric layer 28." (emphases added)), *with id*. at 6:48–52 (Steps 1 and 2 reproduced above);

PO Resp. 24–25. Similar to the claims, in the Abstract and Summary of the Invention section, the Specification describes the claimed process without any language that requires a specific order of performing Steps 1 and 2. Ex. 1001, Abs., 2:25–64; *see also id.* at 3:50–55 ("the present disclosure is not intended to limit the invention to the embodiment illustrated").

We are not persuaded by HSC's arguments and expert testimony that reversing Steps 1 and 2 is impossible from a practical standpoint. PO Resp. 25–26; Ex. 2002 ¶¶ 60–63. Those arguments and testimony are predicated on HSC's construction of "removing a top portion" to require *planarizing* the fourth dielectric layer. *See, e.g.*, PO Resp. 25 ("The top portion of the fourth dielectric is removed by planarization process (described as CMP in the preferred embodiment) that creates a flat surface"); Ex. 2002 ¶ 61 ("[A]ny attempt to planarize the top portion by CMP (as described in the specification) after the photoresist is in place would be frustrated because the CMP polishing pad would be blocked by the resist mask."). We have already determined not to adopt that proposed claim construction for the reasons discussed above in our claim construction analysis in regard to the claim term "removing a top portion."

Furthermore, the claim language of Step 2 does not require forming the resist layer on a *planarized* dielectric layer, let alone on a planarized dielectric layer that exposes a portion of the third dielectric layer covering the gate electrode structure. Once again, HSC attempts to import a limitation from a preferred embodiment into the claims, requiring Step 2 to form a resist layer on such a planarized layer. Our reviewing Court "has

repeatedly cautioned against limiting the claimed invention to preferred embodiments or specific examples in the specification." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1346–47 (Fed. Cir. 2015). "[I]t is the *claims*, not the written description, which define the scope of the patent right." *Id*. at 1346 (emphasis in the original).

HSC's argument that our claim construction excludes the preferred embodiment is misplaced, as such an argument rests on the incorrect assumption that our construction mandates the reversed order of Steps 1 and 2. PO Resp. 27. To the contrary, we merely decline to require a specific order for performing Steps 1 and 2. Dec. 10. Our claim construction encompasses a process that performs Step 1 before Step 2, as well as a process that performs Step 2 before Step 1.

Further, we are not persuaded by HSC's argument and expert testimony that our claim construction would render one of the claimed steps superfluous because, as Samsung notes, HSC does not account for all of the claim elements. PO Resp. 27; Ex. 2002 ¶ 63; Reply 11–12. Indeed, each of the steps removes different portions of the fourth dielectric layer and requires a different result. Ex. 1001, 6:48–50, 6:53–56. Step 1 recites "to expose a portion of said third dielectric layer covering said gate electrode structure," whereas the other "removing" step recites "to form a plurality of trenches adjacent to said gate electrode structure." *Id*.

In view of the foregoing, we decline to adopt HSC's construction, as it would import a limitation—an order of steps—from a preferred embodiment into claims 1 and 14. *See Altiris*, 318 F.3d at 1370–71. Rather, we

determine that Step 1 is not required to be performed before Step 2 in claims 1 and 14.

Claim 16 recites similar steps as those aforementioned steps recited in claim 1, except claim 16 recites "*planarizing* a top portion" instead of "removing a top portion." Ex. 1001, 8:26–31. As written, the "planarizing" step is recited before the "resist forming" step in claim 16, whereas the "removing" step is recited before the "resist forming" step in claims 1 and 14. Samsung relies upon Nakamura's third embodiment, and not Nakamura's first embodiment, to meet these two limitations recited in claim 16. Pet. 27–37. As to claims 1 and 14, Samsung relies upon Nakamura's first embodiment, and, alternatively, Nakamura's third embodiment, to meet the two aforementioned steps. *Id*.

HSC does not challenge Samsung's assertion that Nakamura's third embodiment discloses the aforementioned steps, recited in claims 1, 14, and 16. PO Resp. 42–49. As discussed in our obviousness analysis below, we agree with Samsung's showing and note that Nakamura's third embodiment indeed discloses these limitations recited in claims 1, 14, and 16, in the order written. *See* Pet. 27–37; Ex. 1004, 2:28–32, 9:62–64, 10:6–10, 13:23–47, Figs. 5B, 5C. Therefore, even if we were to construe those steps in claims 1, 14, and 16 to require them to be performed in the order written, it would not change our obviousness analysis based on Nakamura's third embodiment.

Therefore, it is not necessary for us to determine whether the "planarization" step must be performed before the "resist forming" step in claim 16. Only those terms which are in controversy need to be construed,

and only to the extent necessary to resolve the controversy. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In that regard, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418; *see also Translogic*, 504 F.3d at 1259. A prima facie case of obviousness is established when the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. *In re Rinehart*, 531 F.2d 1048, 1051 (CCPA 1976).

It is well-settled that the level of ordinary skill in the art may be reflected by the prior art of record, as here. *See Okajima v. Bourdeau*,

261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc*., 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

We analyze the instituted grounds of unpatentability in accordance with the above-stated principles.

C. Obviousness over Nakamura and Muller

Samsung asserts that claims 1, 9, 11, 12, 14–16, 19, and 20 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Nakamura and Muller. Pet. 16–39, 45–54. In support of this asserted ground of unpatentability, Samsung provides detailed explanations as to how the combination of prior art meets each claim limitation. *Id*. Samsung also relies upon a Declaration of Dr. Gary W. Rubloff. Ex. 1003.

HSC counters that the combination of Nakamura and Muller does not disclose the steps of removing the fourth dielectric layers, as recited in independent claims 1, 14, and 16. PO Resp. 35–50.

We begin our discussion with a brief summary of Nakamura and Muller, and then we address the parties' contentions.

Nakamura

Nakamura describes a method for fabricating a semiconductor device that includes a MOS transistor having raised source and drain electrodes. Ex. 1004, Abs., 20:1–8. Specifically, Nakamura discloses forming a gate electrode before the raised source and drain electrodes (*id*. at 9:37–44, 14:27–33, 15:27–41), as well as forming the contact holes for the source and drain by self-alignment with the gate electrode—free from restriction by

lithographical processing precision (*id*. at 14:47–50, 15:56–16:3). The raised source and drain electrodes are formed in the openings, and the source and drain are formed by diffusing dopants from the source and drain electrodes into the substrate. *Id*. at 15:32–55.

Muller

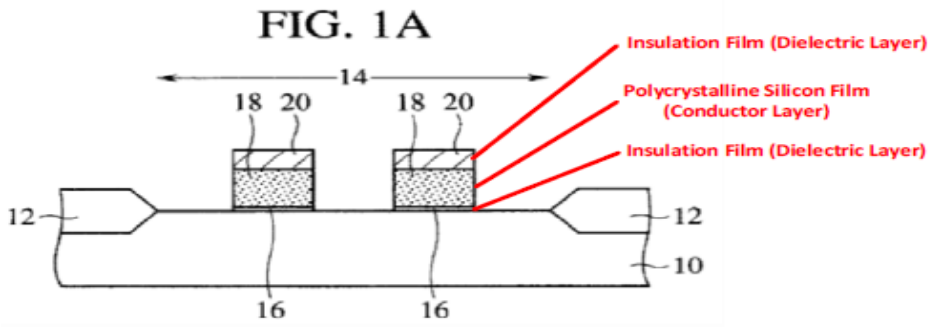
Muller is one of the five books cited by Samsung to show that certain basic semiconductor fabrication processing techniques were well-known in the art at the time of the invention. Ex. 1006. For instance, Samsung relies upon Muller to show that the process of lithography and etching involves the formation of a patterned resist layer to mask portions of the dielectric and conductive layers. Pet. 18–19, 25–27; Ex. 1006, 74–79. Samsung also relies upon Muller to show that the process of anisotropic etching dielectric or conductive layers produces nearly vertical sidewalls, and that a chemical vapor deposition is a well-known alternative to thermal oxidation for forming a silicon oxide layer. Pet. 43–46; Ex. 1006, 66–67, 77–79.

Forming a gate electrode

Samsung contends that the combination of Nakamura and Muller describes forming a gate electrode before the raised source and drain electrodes, as required by independent claims 1, 14, and 16. Pet. 16–27. HSC does not challenge this contention. *See generally* PO Resp.

Upon review of the Petition and prior art disclosures, we are persuaded by Samsung's contention. Notably, Samsung directs our attention

to Figure 1A of Nakamura, reproduced below (red annotations added by Samsung). Pet. at 17–18, 24.



Indeed, annotated Figure 1A of Nakamura above shows that gate electrodes 18 are formed on substrate 10 in active device region 14 before the raised source and drain electrodes. Ex. 1004, 9:31–44. As described by Nakamura, after forming field oxide regions 12 using the local oxidation of silicon (LOCOS) process, gate electrodes 18 are formed by: (1) depositing gate insulation film 16, a polycrystalline silicon film, and insulation film 20; and (2) etching selectively using a lithography process. *Id.*

Notwithstanding that Nakamura does not describe using a patterned resist layer for the selective etch, Samsung maintains that it would have been obvious to one with ordinary skill in the art that Nakamura's selective etch of the gate electrodes would have included forming a patterned resist layer, in light of Muller. Pet. 18–19, 25–27. Indeed, Muller describes a selective etching technique, using a patterned resist layer to mask portions of the deposited films, removing the deposited films other than the portion masked by the resist layer, and transferring the pattern onto the deposited films. Ex. 1006, 74–77. As noted by Samsung, Muller acknowledges that the techniques of forming a patterned resist layer and removing material other

than that masked by the patterned resist layer were the "usual" techniques used in the process of lithography and etching. Pet. 19; Ex. 1006, 74. Samsung's expert, Dr. Rubloff, testifies that it would have been obvious to a person having ordinary skill in the art that "Nakamura would utilize these techniques when it describes processing the gate insulation film 16, doped polycrystalline silicon film, and insulation film of silicon oxide 'by lithography and etching.'" Ex. 1003 ¶ B-4.

Furthermore, although Nakamura does not disclose that gate oxide insulation film 16 is formed by chemical vapor deposition, as required by dependent claim 9, depositing a silicon oxide layer using chemical vapor deposition was known in the art at the time of the invention, as evidenced by Muller. Pet. 45–46 (citing Ex. 1004, 2:1–7, 9:35–36; Ex. 1006, 66–67). Samsung has articulated an adequate rationale to combine the prior art disclosures, which is supported by Dr. Rubloff's testimony. *Id*. Specifically, Dr. Rubloff testifies that, in light of Muller, it would have been obvious to one having ordinary skill in the art that Nakamura's gate oxide film is formed by chemical vapor deposition to produce a high quality gate oxide film, without growing the film through thermal oxidation of the substrate. Ex. 1003 ¶¶ B-9, B-10. We credit Dr. Rubloff's testimony as it is consistent with the prior art of record.

In light of the foregoing, we determine that Samsung has established sufficiently that the combination of Nakamura and Muller describes forming a gate electrode as recited in the claims at issue.

Nakamura's first embodiment

Claim 1 recites "*removing a top portion* of said fourth dielectric layer to expose a portion of said third dielectric layer covering said gate electrode structure." Ex. 1001, 6:48–50 (emphasis added). Claim 1 also recites:

> *removing said fourth dielectric layer* other than said portions masked by said second resist layer to form *a plurality of trenches* adjacent to said gate electrode structure, wherein *portions of the substrate are exposed*, and wherein *spacers are formed* on sidewalls of the gate electrode structure at the same time;

Ex. 1001, 6:53–58 (emphases added). Claim 14 recites similar limitations. *Id*. at 7:47–52.

Samsung takes the position that Nakamura's first and third embodiments disclose these limitations. Pet. 28–37. Samsung first directs our attention to Figures 1C and 2A of Nakamura (reproduced below with annotations and highlights added by Samsung, Pet. 29), which illustrate the first embodiment.

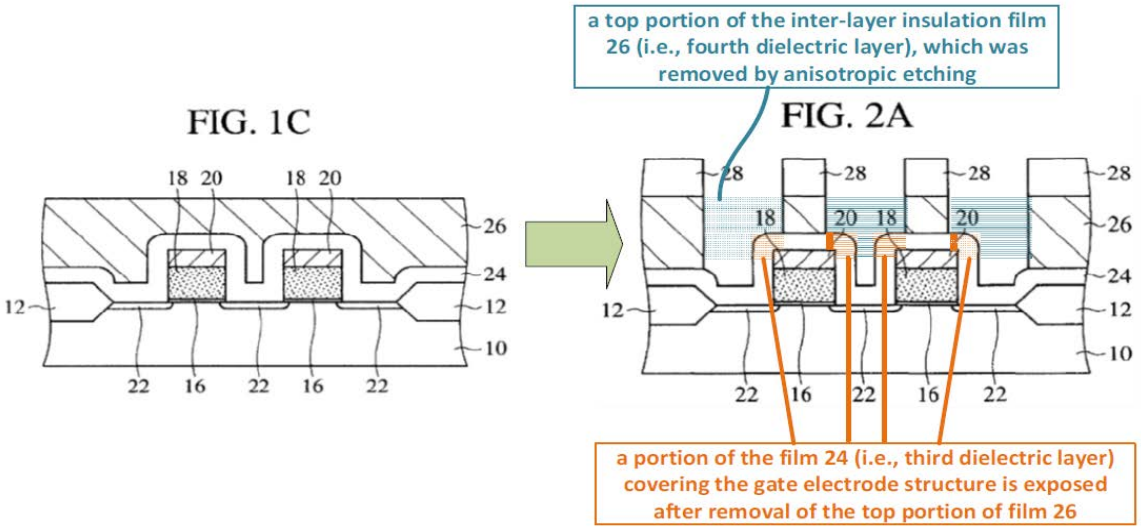
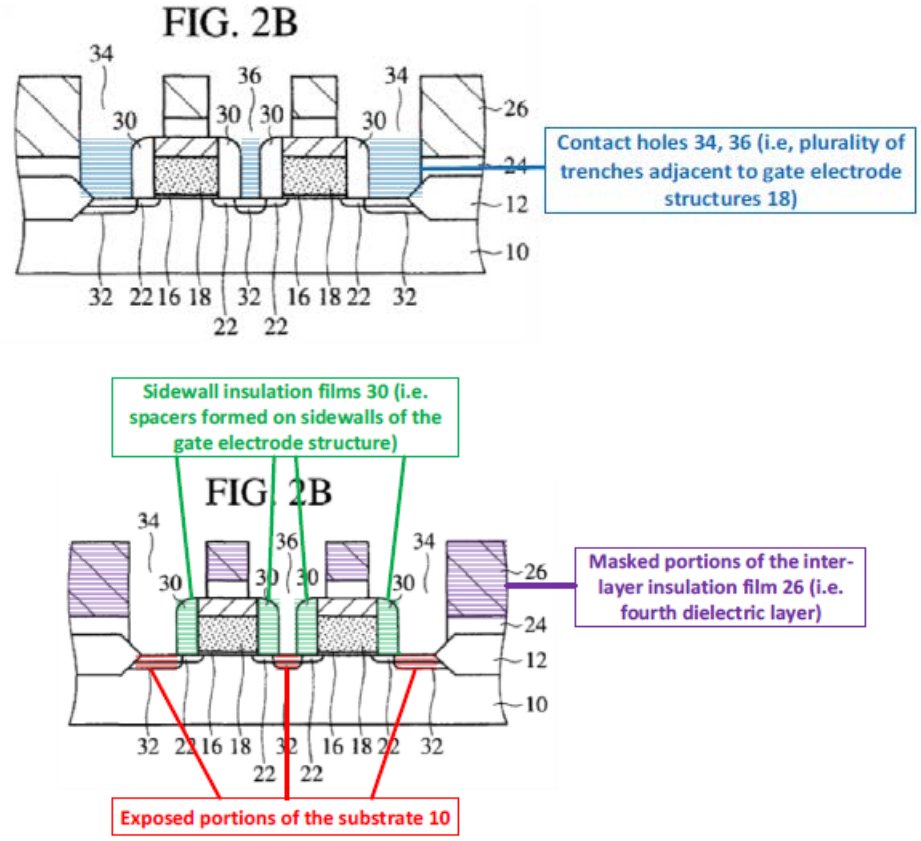


Figure 1C Nakamura depicts third dielectric layer 24 covering substrate 10 directly at regions 22 and gate electrode structure 18. Ex. 1004, 9:24–10:5. Fourth dielectric layer 26 is deposited on third dielectric layer 24. *Id*. at 10:6–17. As shown in annotated Figure 2A above, patterned resist layer 28 is formed on fourth dielectric layer 26, and Nakamura's anisotropic etch first removes a top portion of fourth dielectric layer 26 (in blue) to expose *a portion* of third dielectric layer 24 (in orange) covering gate electrode structure 18, as required by claims 1 and 14. *Id*. at 10:21–29.

Samsung also cites to Figure 2B of Nakamura (reproduced twice with annotations and highlights added by Samsung, Pet. 32–33), which illustrates the result of Nakamura's etch in its first embodiment.



As shown in annotated Figures 2B above, Nakamura's anisotropic etch removes portions of fourth dielectric layer 26, forming a plurality of trenches adjacent to gate electrode structure 18 (in blue), and forming spacers 30 (in green) on the sidewalls of gate electrode structure 18 at the same time. *See* Ex. 1004, 10:18–61. Nakamura also removes portions of third dielectric layer 24, exposing portions of substrate 10 (in red), as required by claims 1 and 14. *Id*.

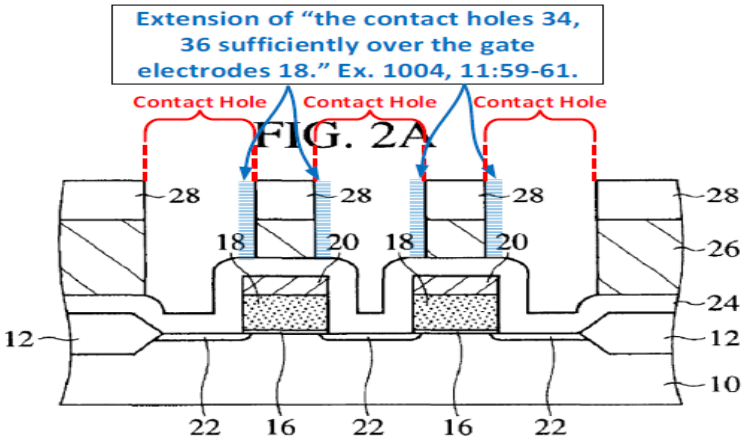
HSC counters that Nakamura does not disclose "removing a top portion" of the fourth dielectric layer, as construed under HSC's proposed construction, which requires: (1) *planarizing* or removing the *entire* top portion of the fourth dielectric layer *across* the wafer, and (2) performing the "removing" step *before* forming the resist layer to mask portions of the fourth dielectric layer. PO Resp. 35–42. According to HSC, Nakamura's etch does not expose a portion of the third dielectric layer *covering the gate electrode*, and any removal over the gate would be unintentional. *Id*. at 38–39. HSC also contends that Samsung relies on the same etch to satisfy both steps for removing portions of the fourth dielectric layers, rendering the "removing a top portion" limitation redundant. *Id*. at 40–42.

At the outset, we note that HSC's arguments and expert testimony are predicated on HSC's proposed claim construction, which imports limitations from a preferred embodiment into the claims. *Id*. at 35–42; Ex. 2002 ¶¶ 83–99. For the reasons stated above in our claim construction analysis, we decline to adopt HSC's proposed construction. Instead, we interpret the claim term "removing a top portion" to require no more than *making a hole*

through a top portion of the fourth dielectric layer to expose a portion of the third dielectric layer covering the gate electrode. We also decline to interpret "removing" as "planarizing" and to interpret "a top portion" as the entire top portion of the dielectric layer across the wafer, as urged by HSC. Nor do we require this "removing" step be performed *before* the resist forming step.

Applying the proper claim construction and based on the evidence before us, we agree with Samsung that Nakamura's first embodiment describes "removing a top portion" of the fourth dielectric layer to expose *a portion* of the third dielectric layer covering the gate electrode structure, as required by claims 1 and 14. Pet. 28–29. We also agree with Samsung that Nakamura's first embodiment describes removing portions of the fourth dielectric layer using a patterned resist layer to form a plurality of trenches, and removing portions of the third dielectric layer to expose the substrate and to form spacers, as required by claims 1 and 14. *Id*. at 29–34.

We are not persuaded by HSC's argument and expert testimony that Nakamura's etch only removes the fourth dielectric layer in the contact holes over the diffusion regions, and not over the gate electrode. PO Resp. 38–39; Ex. 2002 ¶¶ 93–95. The claim language does not require exposing the *entire* portion of the third dielectric layer covering the gate electrode structure, but rather only *a portion* of the third dielectric layer covering the gate electrode. Figure 2A of Nakamura is reproduced below with annotations added by Samsung (Reply, 16):



As shown in annotated Figure 2A of Nakamura above, the openings for the contact holes are extended over gate electrode structure 18 (highlighted in blue), and fourth dielectric layer 26 are removed to expose *a portion* of third dielectric layer 24 covering gate electrode structure 18.

Mr. Maltiel's testimony that "[a]ny removal of material over the gate dielectric would be unintentional" squarely contradicts Nakamura's written disclosure. Ex. 2002 ¶ 95. Nakamura explicitly teaches that to avoid the misalignment problem illustrated in Figures 3A–3B, it is necessary to extend the openings for the contact holes *sufficiently over the gate electrodes*, providing a margin for misalignment in the lithography step for opening the contact holds. Ex. 1004, 11:59–61. According to Nakamura, this is "an effective fabrication method because of its simple process." *Id*. at 11:65–67.

HSC's reliance on *Nystrom v. TREX Co.*, 424 F.3d 1136, 1148 (Fed. Cir. 2005), and *Krippelz v. Ford Motor Co.*, 667 F.3d 1261, 1268 (Fed. Cir. 2012), is misplaced. PO Resp. 39; *Nystrom*, 424 F.3d at 1148 ("[P]atent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent

on the issue."); *Krippelz*, 667 F.3d at 1268 ("This court has repeatedly cautioned against overreliance on drawings that are neither expressly to scale nor linked to quantitative values in the specification."). Neither case applies here because Samsung does not rely on Nakamura's drawings to define the precise proportions or quantitative dimensions of the elements. In fact, as discussed above, Nakamura's written disclosure expressly teaches that it is necessary to extend the openings for the contact holes *sufficiently over the gate electrodes*. Ex. 1004, 11:59–61. Both parties' experts confirm that this disclosure of Nakamura is directed to the first embodiment of Nakamura. Ex. 1016, 269:3–271:10; Ex. 1014 ¶¶ 2–4. More importantly, each of Figures 2A–2C, consistent with Nakamura's written disclosure, shows that the openings where the fourth dielectric layer are etched expose a portion of the third dielectric layer covering the gate electrode. Ex. 1004, Figs. 2A–2C. It is well settled that things patent drawings show clearly are not to be disregarded. *In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972).

HSC's argument that Samsung's reliance on Nakamura's etch renders the "removing a top portion" limitation redundant is inapposite. PO Resp. 40–42. As discussed above, Samsung's explanations have taken into account all of the claim elements in both "removing" limitations, including how Nakamura's etch removes a top portion of the fourth dielectric layer and removes portions of the fourth dielectric layer using a resist layer to form a plurality of trenches, as well as removes the third dielectric layer to expose the substrate and to form the spacers. Pet. 28–34; Ex. 1003 ¶¶ A-14 to A-19; Ex. 1004, 9:24–10:61, Figs. 1C, 2A, 2B.

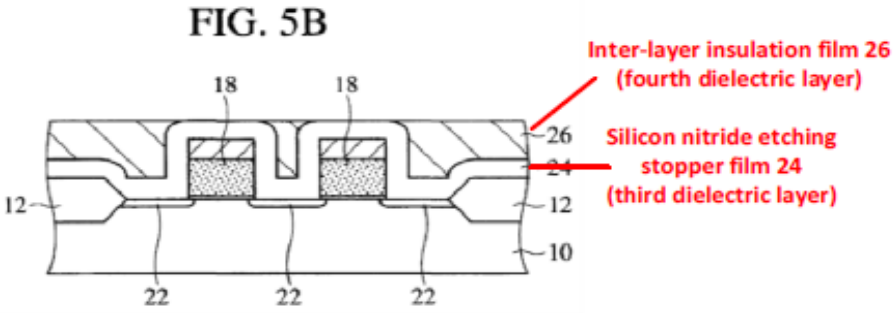
We also are not persuaded by HSC's argument and expert testimony that Nakamura's etch cannot satisfy both claim "removing" limitations. PO Resp. 40–42; Ex. 2002 ¶¶ 97–98. Nothing in the claim language requires each "removing" step to be performed independently or separately. The claims do not exclude a continuous process, in which the step for removing portions of the fourth dielectric layer to form a plurality of trenches adjacent to the gate electrode is initiated as soon as a top portion of the fourth dielectric layer is removed, exposing a portion of the third dielectric layer covering the gate electrode.

For the foregoing reasons, we conclude that Samsung has demonstrated sufficiently that Nakamura in combination with Muller discloses both "removing" limitations for removing portions of the fourth dielectric layer, as required by claims 1 and 14.

Nakamura's third embodiment

Samsung also asserts that Nakamura's third embodiment describes "removing a top portion" of the fourth dielectric layer to expose a portion of the third dielectric layer covering the gate electrode, as required by claims 1 and 14, as well as "planarizing a top portion" of the fourth dielectric layer, as recited in claim 16. Pet. 27–37. Samsung further takes the position that Nakamura's third embodiment describes "forming on the substrate a patterned second resist layer to mask portions of the fourth dielectric layer," as required by claims 1, 14, and 16. *Id*. HSC does not challenge those assertions. PO Resp. 42–49.

We are persuaded by Samsung's showing. Notably, Samsung directs our attention to Figure 5B of Nakamura, reproduced below (annotations added by Samsung, Pet. 30):



As shown in annotated Figure 5B of Nakamura above, third dielectric layer 24 and fourth dielectric layer 26 are deposited by chemical vapor deposition, on top of gate electrodes 18. Ex. 1004, 2:28–32, 9:62–64, 10:6–10, 13:23–35. Nakamura discloses that the entire top portion of fourth dielectric layer 26 across the wafer is planarized by chemical mechanical polishing, exposing a portion of third dielectric layer 24 covering gate electrodes 18. *Id*. As Samsung notes, Nakamura further describes that "a photoresist 28 having an opening spanning regions to be a source/drain diffused layer 38 and regions to be a source/drain diffused layer 40 is formed [subsequently] by the usual lithography." Pet. 31; Ex. 1004, 13:39–42.

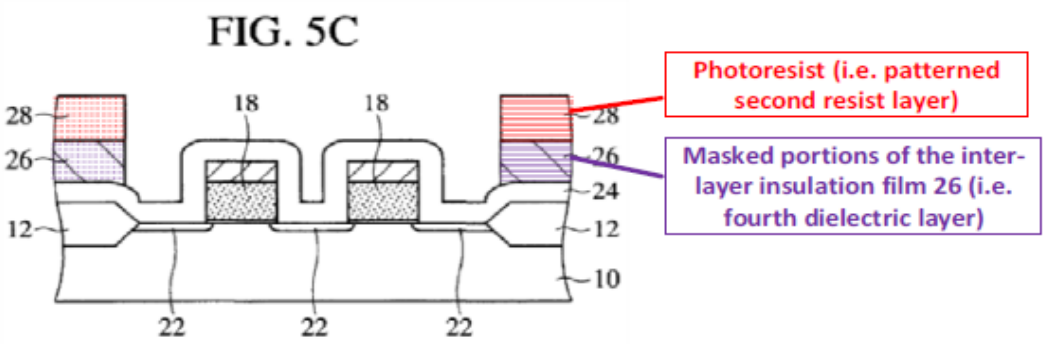
Based on the disclosure of Nakamura, we agree with Samsung that Nakamura's third embodiment describes a step for removing and planarizing a top portion of the fourth dielectric layer to expose a portion of the third dielectric layer covering the gate electrode, as well as a step for forming a patterned second resist layer, as recited in claims 1, 14, and 16, in the order written.

With regard to Nakamura's third embodiment, the parties' dispute centers on the limitation reproduced below. PO Resp. 42–49; Reply 18–25.

Claims 1 and 16 recite:

> [1] *removing said fourth dielectric layer* other than said portions masked by said second resist layer to form a plurality of trenches adjacent to said gate electrode structure, [2] *wherein* portions of the substrate are exposed, and [3] *wherein* spacers are formed on sidewalls of the gate electrode structure *at the same time*;

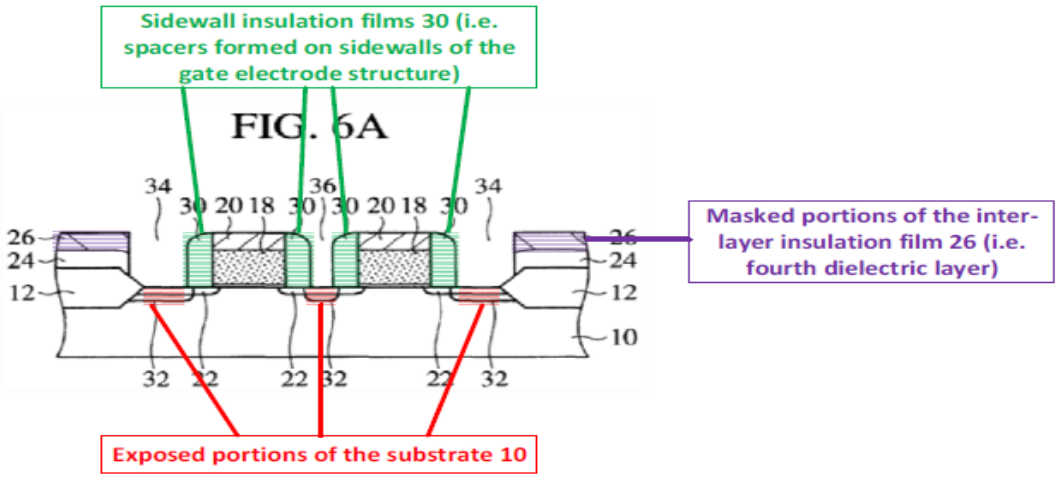
Ex. 1001, 6:53–58, 8:32–37 (emphases and bracketed numbers added). Claim 14 requires similar method steps. *Id*. at 7:47–52. Samsung takes the position that Nakamura's third embodiment also describes this limitation. Pet. 27–37. As support, Samsung cites to Figure 5C of Nakamura, reproduced below (annotations added by Samsung, Pet. 31):



As shown in annotated Figure 5C of Nakamura above, a plurality of trenches adjacent to gate electrodes are formed by depositing patterned photoresist 28 on the substrate and then removing the unmasked portions of fourth dielectric layer 26. Ex. 1004, 13:39–47. Based on that disclosure, we agree with Samsung that Nakamura's third embodiment describes "removing said fourth dielectric layer other than said portions masked by said second resist layer to form a plurality of trenches adjacent to said gate

electrode structure," as recited by claims 1 and 16, and similarly required by claim 14.

Samsung also cites to Figure 6A of Nakamura, reproduced below (annotations added by Samsung, Pet. 35).



As shown in annotated Figure 6A of Nakamura above, portions of third dielectric layer 24 are etched to expose portions of substrate 10 (highlighted in red). Ex. 1004, 13:56–64. Nakamura also discloses forming spacers 30 (highlighted in green) on the sidewalls of gate electrodes 18. *Id.*

Given the evidence before us, we also agree with Samsung that Nakamura's third embodiment describes removing portions of the third dielectric layer to expose portions of the substrate, and forming spacers at the same time.

HSC counters that Nakamura's third embodiment does not meet the disputed limitation for removing the portions of the fourth dielectric layer. PO Resp. 42–43. As support, HSC advances several arguments. *Id.*

First, HSC argues that, during Nakamura's process step where only the unmasked portions of the fourth dielectric layer are removed, the trenches are only partially formed, the substrate is not exposed, and the spacers are not yet formed. *Id*. at 42–43. HSC also alleges that the disputed claim limitation requires all three results identified by HSC to occur at the same time during the step of removing the fourth dielectric layer *with the resist mask in place*. *Id*. at 44–46.

As an initial matter, we note that HSC's arguments and expert testimony are predicated on HSC's proposed claim construction, which imports extraneous limitations into the claims, requiring that all three results identified by HSC occur at the same time. *Id*. at 42–46; Ex. 2002 ¶¶ 102–111. As discussed above in our claim construction analysis, we decline to adopt HSC's proposed claim construction. We note that the claim language merely requires removal of the fourth dielectric layer, and not the third dielectric layer. Without removing the portions of the third dielectric layer that are directly on the substrate, none of the following results identified by HSC would occur: (1) exposing portions of the substrate; (2) forming a plurality of trenches that extend down to the substrate; and (3) forming spacers on the sidewalls of the gate electrodes. Nothing in the claims requires that the trenches extend down to the substrate, let alone that the trenches extend down to the substrate as a result of only removing the fourth dielectric layer. HSC's arguments ignore the claim language "depositing sequentially a third dielectric layer and a fourth dielectric layer on said substrate and said gate electrode structure," which is recited before the

disputed limitation, and the fact that the claims do not recite a step for removing portions of the third dielectric layer that are directly on the substrate. Even if we construe the claims to require a step for removing the third dielectric layer to expose the substrate and to form spacers, such a step would occur *subsequent* to, not at the same time as, the step for removing the fourth dielectric layer because the portions of the third dielectric layer that are directly on the substrate are underneath the fourth dielectric layer, and the step for removing the fourth dielectric layer is anisotropic for forming the trenches. *See* Ex. 1001, 4:62–5:44, Fig. 4.

Significantly, HSC's arguments and expert testimony narrowly focus on the first phase of Nakamura's etching process, and not the entire etching process. Ex. 1004, 13:23–64. In fact, as discussed above and shown in Figures 5C and 6A of Nakamura (reproduced above), Nakamura etches the unmasked portions of the fourth dielectric layer using a patterned resist layer to form a plurality of trenches adjacent to the gate electrodes (as shown in Figures 5C), and etches portions of the third dielectric layer to expose the substrate and to form spacers on the sidewalls of the gate electrodes (as shown in Figure 6A). *Id*. Moreover, the claim language does not require the resist mask to be in place during the entire etching process. HSC's arguments once again attempt to import improperly an extraneous limitation into the claims. *Hoganas*, 9 F.3d at 950.

Second, HSC contends that Nakamura uses two etch steps to remove portions of the fourth dielectric layer—a first patterned etch followed by a second unpatterned etch. PO Resp. 46–47. HSC also argues that no masked

portions of the fourth dielectric layer should be removed. *Id*. However, HSC's arguments attempt to import improperly extraneous negative limitations into the claims. *Hoganas*, 9 F.3d at 950. Each challenged claim uses the open-ended transitional term "comprising" which does not exclude additional, unrecited elements. *See Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997). The claim language only requires removal of the unmasked portions of the fourth dielectric layer to form a plurality of trenches adjacent to the gate electrode. As discussed above, Nakamura discloses etching unmasked portions of fourth dielectric layer using a patterned resist layer, forming a plurality of trenches adjacent to the gate electrodes, as shown in Figure 5C of Nakamura (reproduced above). Ex. 1004, 13:39–47. More importantly, there is no dispute that Nakamura's etching process as a whole produces all three results identified by HSC, including exposing portions of the substrate and forming spacers on the sidewall of the gate electrode, as well as forming a plurality of trenches that extend down to the substrate, as shown in Figure 6A of Nakamura (reproduced above). *Id*. at 13:23–64.

Even if the claims require a continuous etching process for removing both the third and fourth dielectric layers with the resist layer in place, we are persuaded by Samsung's assertion that it would have been obvious to modify Nakamura's etching process in the third embodiment to leave the resist layer in place and continue the anisotropic etching process, in light of the teachings in the first embodiment of Nakamura, because "it would reduce the time necessary to complete the etching process and likely

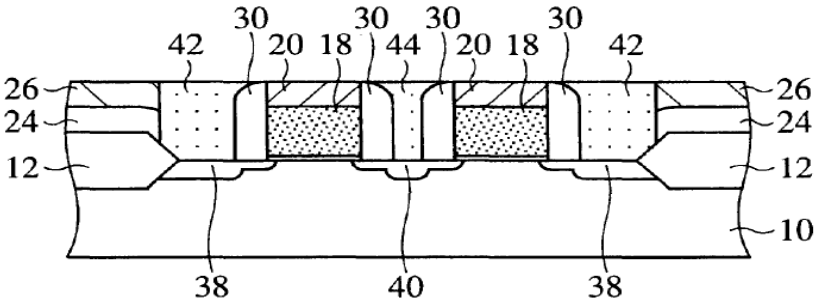
eliminate the need to transport the substrate between different tools." Pet. 37. Such modification would not conflict with the objective—improving depth of focus—Nakamura was trying to achieve, as alleged by HSC. PO Resp. 48–49. Nakamura also describes simplification of the fabrication process and reduction of cost as important objectives. Ex. 1004, 10:57–61. As Dr. Rubloff explains, the process, as modified in light of Nakamura's first embodiment, would still improve depth of focus, which is only one of the objectives taught by Nakamura, as well as achieving efficiency. Ex. 1014 ¶¶ 14–20. Dr. Rubloff testifies that one of ordinary skill in the art would consider all of the goals described by Nakamura and, after weighing the costs and benefits of each known technique, would make adjustments accordingly to improve the process. Ex. 1014 ¶¶ 9–12. Indeed, the modified process would utilize the planarization CMP technique of Nakamura's third embodiment to improve depth of focus (Ex. 1004, 13:10–38), and the continuous etching technique (with the resist layer in place) of Nakamura's first embodiment to remove the third and fourth dielectric layers over the contact regions to improve efficiency (*id*. at 10:17–61). Therefore, we are persuaded that Samsung has articulated reasoning with rational underpinnings for modifying Nakamura's third embodiment in light of the first embodiment of Nakamura. *See KSR*, 550 U.S. at 417 ("[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.").

For the foregoing reasons, we determined that Samsung has demonstrated sufficiently that the combination of Nakamura and Muller would render obvious the disputed claim limitation, as recited in claims 1 and 16, and as similarly recited in claim 14.

Forming raised electrodes, source, and drain

Samsung asserts that the combination of Nakamura and Muller describes forming the raised source and drain electrodes, as well as forming the raised source and drain, for a metal-oxide-semiconductor field-effect transistor (MOSFET), as required by claims 1, 14–16, 19, and 20. Pet. 38–42. HSC does not challenge this assertion. *See generally* PO Resp.

Upon review of the Petition and prior art disclosures, we are persuaded by Samsung's contention. Notably, Figure 7B of Nakamura, reproduced below, shows a transistor having raised electrodes, source, and drain.



As shown in Figure 7B of Nakamura, a transistor is formed on substrate 10, within device active region between isolation regions 12. Ex. 1004, 9:27–36, 14:34–37, 16:56–67. Each gate electrode 18 has a gate dielectric, conductive film, dielectric film 20, and sidewall spacers 30. *Id*. at 9:37–45, 10:21–42, 12:60–67, 14:34–37. Nakamura discloses that raised

source and drain electrodes 42, 44 are formed, in self-alignment with gate electrodes 18, by: (1) depositing a conductive film (e.g., a polysilicon film) on the entire surface, filling the trenches adjacent to the gate electrodes; (2) etching back the conductive film, leaving only the portions in the trenches; and (3) doping the conductive film. Ex. 1004, 11:9–11, 14:58–67; 15:27–55. Nakamura further describes forming raised source and drain 38, 40 by using a thermal processing, diffusing the dopant from raised source and drain electrodes 42, 44 into the substrate. *Id*. at 15:36–46.

Given the evidence before us, we determine that Samsung has shown sufficiently that Nakamura's transistor is a MOSFET having raised electrodes, source, and drain. *See, e.g.*, Pet. 53–54 (citing Ex. 1003 ¶ A-3; Ex. 1004, 16:18–23, 20:1–8; Ex. 1007, 611).

Conclusion on obviousness over Nakamura and Muller

With respect dependent claims 9, 11, 12, 15, 19, and 20, we agree with Samsung's showing that the combination of Nakamura and Muller renders the claimed subject matter as a whole obvious. Pet. 16–39, 45–54; Ex. 1003. HSC relies on the same arguments presented in connection with independent claims 1, 14, and 16. PO Resp. 49–50. As discussed above, we found those arguments unavailing.

For the foregoing reasons, we determine that Samsung has demonstrated a preponderance of the evidence that independent claims 1, 9, 11, 12, 14–16, 19, and 20 are unpatentable over the combination of Nakamura and Muller.

D. Obviousness over Nakamura and Muller, in view of Mukherjee, Wolf, Ghandhi, and Pierret

Samsung contends that: (1) claims 2–4, 6–8, 17, and 18 are unpatentable under § 103(a) as obvious over the combination of Nakamura, Muller, and Mukherjee (Pet. 40–45, 54–56); (2) claim 5 is unpatentable under § 103(a) over the combination of Nakamura, Muller, and Wolf (*id*. at 56–57); (3) claim 10 is unpatentable under § 103(a) over the combination of Nakamura, Muller, and Ghandhi (*id*. at 57–59); and (4) claim 13 is unpatentable under § 103(a) over the combination of Nakamura, Muller, and Pierret (*id*. at 59–60). As support, Samsung provides detailed explanations as to how the combination of prior art meets each claim limitation, as well as reasons as to why one with ordinary skill in the art would have combined the technical disclosures of the prior art references. *Id.* at 40–45, 54–60. Samsung also relies upon the Declaration of Dr. Rubloff (Ex. 1003).

With respect to claims 2–8, 10, 13, 17, and 18, HSC relies on the same arguments presented in connection with independent claims 1, 14, and 16. PO Resp. 49–50. We addressed those arguments in our obviousness analysis based on the combination of Nakamura and Muller above, and found them unavailing.

Upon consideration Samsung's explanations and supporting evidence, we are persuaded by Samsung's contentions. For example, with respect to claims 2 and 17, which require a step of forming a lightly doped well in the substrate, Samsung directs our attention to Mukherjee that discloses a basic MOS fabrication technique using a diffusion process to create a p-well in an

n-type substrate or an n-well in a p-type substrate. Pet. 54–56 (citing Ex. 1005, 119–126). Indeed, Mukherjee describes forming a lightly doped well in the substrate in the device active area and using a thick oxide layer as a mask to select the regions where implantation is needed. Ex. 1005, 123. Moreover, Dr. Rubloff testifies that it would have been obvious to one with ordinary skill in the art to modify Nakamura to implement Mukherjee's technique to form a lightly doped well "to improve transistor characteristics such as the transistor threshold." Ex. 1003 ¶¶ C-2, C-3.

Given the evidence in this record, we determine that Samsung has demonstrated by a preponderance of the evidence that the combinations of the cited prior art references render claims 2–8, 10, 13, 17, and 18 unpatentable.

III. CONCLUSION

For the foregoing reasons, we determine that Samsung has demonstrated by a preponderance of the evidence that claims 1–20 of the '244 patent are unpatentable based on the following grounds:

Challenged Claim(s)	Basis	References
1, 9, 11, 12, 14–16, 19, and 20	§ 103(a)	Nakamura and Muller
2–4, 6–8, 17, and 18	§ 103(a)	Nakamura, Muller, and Mukherjee
5	§ 103(a)	Nakamura, Muller, and Wolf
10	§ 103(a)	Nakamura, Muller, and Ghandhi
13	§ 103(a)	Nakamura, Muller, and Pierret

IV. ORDER

For the foregoing reasons, it is

ORDERED that claims 1–20 of the ’244 patent are held unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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