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Paper No. 33
Filed: December 14, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DIABLO TECHNOLOGIES, INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00883
Patent 8,081,536 B1

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

BRADEN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6(c). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 1, 16, 17, 24, 30, and 31 of U.S. Patent No. 8,081,536 B1 (Ex. 1001, "the '536 patent") are unpatentable.

A. Procedural History

Diablo Technologies, Inc. ("Petitioner") filed a Corrected Petition (Paper 4, "Pet.") to institute an *inter partes* review of claims 1, 16, 17, 24, 30, and 31 of the '536 patent. Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 8, "Prelim. Resp."). Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of all challenged claims on the following grounds alleged in the Petition.

References	Basis	Claims Challenged
Klein[1] and Amidi[2]	§ 103	1, 16, 17, 24, 30, and 31
Klein, Amidi, and Dell[3]	§ 103	16, 17, 30, and 31

Paper 11 ("Dec. to Inst."), 26.

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 25, "PO Resp."), to which Petitioner filed a Reply (Paper 27, "Reply"). An oral argument was held on July 28, 2015, consolidated with

[1] US Patent Publication No. 2001/0008006 A1, pub. July 12, 2001 ("Klein," Ex. 1006).
[2] US Patent Publication No. 2006/0117152 A1, pub. June 1, 2006 (filed Jan. 5, 2004) ("Amidi," Ex. 1008).
[3] U.S. Patent No. 6,446,184 B2, iss. Sept. 3, 2002 ("Dell," Ex. 1009).

the oral hearings for IPR2014-00882 and IPR2014-01011. *See* Paper 30. A transcript ("Tr.") of the oral argument is included in the record. Paper 31.

B. Related Proceedings

The parties inform us that the '536 patent is the subject of the following federal district court case: *Netlist, Inc. v. Smart Modular Technologies,* Case. No. 4:13-cv-05889-YGR (N.D. Cal.). Papers 6, 10.

The '536 patent claims priority to U.S. Patent No. 7,289,386 ("the '386 patent). Pet. 7. Petitioner informs us that the related '386 patent is the subject of *inter partes* reexamination 95/000,577. *Id*. The '386 patent is also the subject of district court case *Google, Inc. v. Netlist, Inc*., Case No. C08-4144 SBA (N.D. Cal.). *Id*. at 11.

In addition, Petitioner filed two other petitions requesting *inter partes* review of related U.S. Patent No. 7,881,150 B2. Paper 6, 2. These cases are: IPR 2014-00882 and IPR2014-01011. *Id.* We consolidated the oral hearings for IPR2014-00882, IPR2014-00883, and IPR 2014-01011. *See* Paper 30.

C. The '536 Patent

The '536 patent is directed to a memory module of a computer system with improved performance and memory capacity. Ex. 1001, 1:35–38. Memory module 10 includes a plurality of memory devices 30 (arranged in ranks 32) and circuit 40. *Id.* at 5:25–34; Fig. 1. Circuit 40 is electrically coupled to the memory devices 30 and memory controller 20 of a computer system. *Id.* The memory module improves performance and memory capacity by isolating electrical loads of the memory devices from the computer system. *Id.* at 5:34–35.

Circuit 40 receives input signals from memory controller 20. *Id.* Figure 1, reproduced below, illustrates input signals (corresponding to a number of memory devices) from memory controller 20, such as chip select signals ("cs#"), that are directed to memory module 10, which can act as a virtual memory module. *Id*. at 16:57–65; Figs. 1, 9A, 9B.

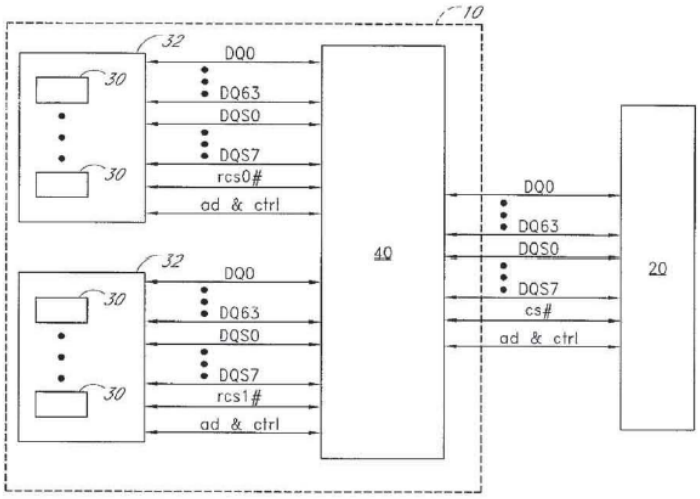

Figure 1 is a schematic of a memory module with circuit 40 and memory devices 30 and connectable to memory controller 20.

As shown in Figure 1, based on the received input signals from memory controller 20, circuit 40 generates output signals corresponding to memory devices 30 on the memory module. *Id*. at Fig. 1. The output signals include a different number of chip select signals (e.g., "rcs0#" and "rcs1#") corresponding to memory devices 30 shown in ranks 32. *Id*. at 17:7–12; Fig. 1.

Circuit 40 includes a logic element, such as a programmable logic device (PLD), an application-specific integrated circuit (ASIC), a field programmable gate array (FPGA), or a complex programmable-logic device (CPLD). Ex. 1001, 6:40–45. As shown in Figure 9A, reproduced below,

circuit 40 also includes register 230 and phase-lock loop device (PLL) 220. *Id.* at 15:52–58; Fig. 9A.

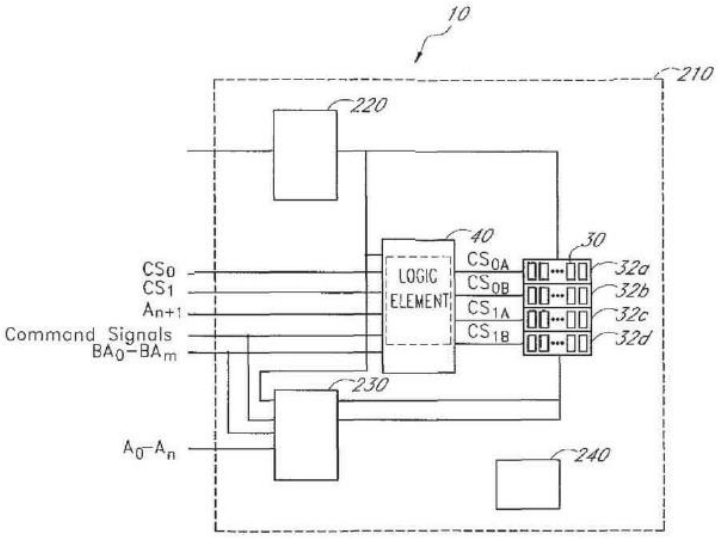

Figure 9A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system.

Figure 9A illustrates circuit 40 receiving a set of input command signals, address signals (A_{n+1}), including bank address signals (BA_0-BA_m), row address signals (A_0-A_n), column address signals, gated column address strobe signals, and chip-select signals (CS_0, CS_1), from memory controller 20 of the computer system. *Id.* at 16:36–41, 17:19–34. "In response to the set of input address and command signals, circuit 40 generates a set of output address and command signals." *Id.* at 16:42–44.

With the output address and command signals, circuit 40 isolates the electrical loads of some of memory devices 30 from the computer system. *Id.* at 7:17–31. According to the '536 patent, load isolation may result in specific benefits including reduced load related to data signal lines. *Id*. at 14:57–62. In order to isolate the loads, the logic element of circuit 40 translates between a system memory domain of the computer system and a

physical memory domain of memory module 10. *Id.* at 7:17–31. As shown in Figure 3, reproduced below, the circuit isolates the load of a memory device by isolating one or both of DQ data signal lines 102a, 102b of two memory devices 30a and 30b from common DQ data signal line 112 that is coupled to the computer system. Ex. 1001, 7:32–38, Fig. 3A.

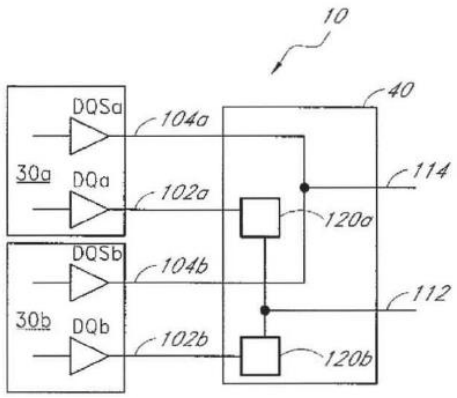

Figure 3A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system.

Circuit 40 can electrically couple one or both of the DQ data signal lines 102a, 102b of the two memory devices 30a and 30b to the common data signal line 112, at the same time. *Id.* at 7:58–62. Circuit 40 also allows a DQ data signal to be transmitted from memory controller 20 of the computer system to one or both of DQ data signal lines 102a, 102b. *Id.* at 7:38–41. The logic element of circuit 40 uses switches 120a, 120b in order to isolate or couple one or both of DQ data signal lines 102a, 102b of memory devices 30a and 30b from common data signal line 112. *Id.* at 7:38–46.

D. Illustrative Claim

As noted above, *inter partes* review was instituted for claims 1, 16, 17, 24, 30, and 31 of the ’536 patent, of which claims 1 and 24 are

independent claims. Claim 1 is illustrative of the challenged claims and is reproduced below:

1. A circuit configured to be mounted on a memory module configured to be operationally coupled to a computer system, the memory module having a first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory circuits that are configured to be activated concurrently with one another for receiving and transmitting data having a bit width of the rank in response at least in part to a first number of DDR chip-select signals, the circuit including at least one configuration in which the circuit is configured to:
receive a set of signals comprising address signals and a second number of DDR chip-select signals smaller than the first number of DDR chip-select signals;
generate phase-locked clock signals and transmit the phase-locked clock signals to the DDR memory circuits of the first number of ranks;
selectively isolate a load of the DDR memory circuits of at least one rank of the first number of ranks from the computer system in response at least in part to the set of signals; and
generate the first number of DDR chip-select signals in response at least in part to the phase-locked clock signals, the address signals, and the second number of DDR chip-select signals.

Ex. 1001, 41:20–43.

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 ("Congress implicitly approved the broadest reasonable interpretation standard in enacting the AIA," and "the standard was properly adopted by PTO

regulation."). Under that standard, and absent any special definitions, we give claim terms their ordinary and customary meaning as would be understood by one of ordinary skill in the art at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Yet a "claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history." *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002).

1. "Selectively Isolate" and "Selectively Isolating,"

In the Decision to Institute, we construed the terms "Selectively Isolate" and "Selectively Isolating," which are recited in all the challenged independent claims. *See* Dec. to Inst. 8–10. In their papers, neither party challenged our constructions of these claim terms.[4] PO Resp. 4, 25–27; Reply 3–8. Thus, for the terms "Selectively Isolate" and "Selectively Isolating," we see no reason to alter the constructions of these claim terms as set forth in the Decision to Institute as shown below, and we incorporate our previous analysis for purposes of this decision.

[4] Patent Owner's Declarant, Dr. Sechen, testifies based on the claim constructions in Patent Owner's Preliminary Response and not on the constructions set forth in the Decision to Institute. *Compare* Ex. 2002 ¶¶ 38–70 (Declaration of Dr. Carl Sechen), *with* Dec. to Inst. 8–10. In several instances, Dr. Sechen acknowledges that Patent Owner does not propose constructions in its Patent Owner Response. Ex. 2002 ¶¶ 38, 59, 64. Dr. Sechen does not contend we should modify our claim constructions, nor does he provide sufficient rationale as to why we should modify our claim constructions. *Id.*

Claim Term	Construction
"selectively isolate" / "selectively isolating"	"electrical separation from one selected component from another selected component"

See Dec. to Inst. 8–10.

Patent Owner, however, argued at the oral hearing for a different construction for "Circuit Configured to be Mounted on a Memory Module." Tr. 68:1–18. Therefore, we address Patent Owner's contentions and construe "Circuit Configured to be Mounted on a Memory Module" as discussed below.

2. "Circuit Configured to be Mounted on a Memory Module"

In the Decision to Institute, we construed the term "a circuit configured to be mounted on a memory module," to encompass "circuitry configured to be mounted on at least a portion of a memory module." Dec. to Inst. 11–12. Such a construction is consistent with the ordinary and customary meaning of "a circuit configured to be mounted on a memory module." *Id.* at 12.

Petitioner agrees with the construction set forth in the Decision to Institute. Reply 4; Tr. 5:25–6:10. Patent Owner, however, contends that "a circuit configured to be mounted on a memory module" should be construed as "an entire circuit configured to be mounted on a single memory module." PO Resp. 11–13; Tr. 68:1–18.

Patent Owner notes that our claim construction, as set forth in the Decision to Institute, is ambiguous in that it can be read two ways:

> One might read the Board's construction as meaning that the circuit is mounted on and occupies at least a portion of the memory module (Ex. 2002, ¶ 62), which may be consistent with

> Netlist's construction. On the other hand, one might read the Board's construction as encompassing portions of the circuit to be mounted off-module, which would be unreasonably broad to a [person of ordinary skill in the art].

Id. at 11 (citing Ex. 2002 ¶ 62). According to Patent Owner, "memory module" is a term of art that would have had have a well-understood meaning to a person of ordinary skill in the art at the time of the invention and a person of ordinary skill in the art would not have understood "a circuit configured to be mounted on a memory module" to include circuit parts off of that memory module or on a different memory module. *Id.* at 12 (citing Ex. 2002 ¶ 60). Patent Owner contends that such a construction could include situations that defeat the purpose of a memory module to make removing and installing memory upgrades easy and error-free. *Id*. (citing Ex. 2002 ¶ 61).

We decline to adopt Patent Owner's claim construction as it is inconsistent with the definition of "circuit" as found in the specification of the '150 patent. The '150 patent defines "circuit" as "a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions." Ex. 1001, 5:9–13. The '150 patent does not limit a "circuit" to only a configuration of electrical components or devices that are mounted on a single memory module. Therefore, applying the broadest reasonable interpretation consistent with the specification of the '150 patent, we construe the claim element "a circuit configured to be mounted on a memory module," as we did in the Decision to Institute, but we further

clarify the construction to encompass "at least a portion of circuitry configured to be mounted on at least a portion of a memory module."

3. Other Claim Terms

We determine that no express constructions of any other claims terms are required for our analysis, and we apply the ordinary and customary meaning of each claim term.

B. Principles of Law

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

We analyze the instituted grounds of unpatentability in accordance with the above-stated principles.

C. Level of Ordinary Skill in the Art

In determining whether an invention would have been obvious at the time it was made, we determine the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere*, 383 U.S. at 17. "The

importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry." *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner's Declarant, Srinivasan Jagannathan, Ph.D. ("Dr. Jagannathan"), testifies that a person of ordinary skill in the art at the time of the '536 patent:

> would understand basic memory and data communication concepts, with a bachelor's degree in any of electrical engineering, computer engineering, computer science, or related field. Course work for one of ordinary skill in the art would have included a course on computer organization, principles of digital design, or computer architecture. One of ordinary skill in the art would also have around one year of experience related to computer memory systems. For example, such experience may include experience in DRAM memory technology and related industry standards such as JEDEC standards for DRAM memories and memory modules.

Ex. 1011 ¶ 50.

Patent Owner's Declarant, Carl Sechen, Ph.D. ("Dr. Sechen"), testifies that one of ordinary skill in the art at the time of the '536 patent would have had an undergraduate degree in electrical engineering or computer engineering, at least two years of professional experience in the design of memory systems, familiarity with the latest JEDEC standard specifications for memory devices and modules, and familiarity with the latest DRAM memory devices widely available in the market. Ex. 2002 ¶ 14. Dr. Sechen further testifies that a person of ordinary skill in the art would have design proficiency in memory modules comprising DDR memory technology, such as memory modules with JEDEC standard DDR SDRAM devices. *Id.* at ¶ 15. Patent Owner concurs with Dr. Sechen's

opinion regarding the level of skill in the art at the time of the '536 patent. PO Resp. 13–15 (citing Ex. 2002 ¶¶ 14–16, 18–20, 28).

Based on our review of the '536 patent and the types of problems and solutions described in the '536 patent and cited prior art, we conclude a person of ordinary skill in the art at the time of the '536 patent would have a Bachelor's degree in electrical engineering, computer engineering, computer science, or related field and at least one year of work experience, including familiarity with computer memory systems and related industry standards such as JEDEC standards for DRAM memories and memory modules. We further note that the applied prior art reflects the appropriate level of skill at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

D. Expert Testimony

Patent Owner argues that Petitioner's declarant, Dr. Jagannathan, does not qualify as a person of ordinary skill in the art at the time of the invention because of his alleged lack of experience designing memory modules. PO. Resp. 13–22. According to Patent Owner, Dr. Jagannathan's experience and background is directed to software and is not relevant to the case. *Id.* at 15–20. Patent Owner argues that, unlike Dr. Jagannathan, its Declarant Dr. Sechen has significant practical experience designing memory modules. *Id.* at 20 (citing Ex. 2002, Exhibit A).

As to his hardware and memory design experience, Dr. Jagannathan was awarded a Doctorate degree in Computer Science, and has "two decades of experience in the design, development, and analysis of a wide range of hardware, software, network and database systems." Ex. 1011 ¶ 2. He has designed and implemented hardware virtual memory caches, and researched

theoretical performance measures of various cache coherency protocols. *Id.* Dr. Jagannathan also stated during his deposition that he has experience in the design of memory systems. Ex. 2003, 124:12–126:1. Patent Owner contends, however, that Dr. Jagannathan fails to qualify as a person of ordinary skill in the art because he lacks sufficient professional experience physically designing (i.e., "actually putting down a design and saying this is what it would be") a memory module. PO Resp. 18 (citing Ex. 2003, 125:14–17). We disagree. To testify as an expert under Fed. R. Evid. 702, a person need not be a person of ordinary skill in the art, but rather must be "qualified in the pertinent art." *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008); *see SEB S.A. v. Montgomery Ward & Co.*, 594 F.3d 1360, 1372–73 (Fed. Cir. 2010) (upholding a district court's ruling to allow an expert to provide testimony at trial because the expert "had sufficient relevant technical expertise" and the expert's "knowledge, skill, experience, training [and] education . . . [wa]s likely to assist the trier of fact to understand the evidence"); *Mytee Prods., Inc. v. Harris Research, Inc.*, 439 Fed. App'x 882, 886–87 (Fed. Cir. 2011) (non-precedential) (upholding admission of the testimony of an expert who "had experience relevant to the field of the invention," despite admission that he was not a person of ordinary skill in the art). We find that, although Dr. Jagannathan is less experienced than Dr. Sechen in the area of memory module design, he is qualified sufficiently to testify as an expert witness about memory systems and memory modules.

E. Alleged Obviousness of Claims 1, 16, 17, 24, 30, and 31 in view of Klein and Amidi

Petitioner alleges claims 1, 16, 17, 24, 30, and 31 of the '536 patent are unpatentable under 35 U.S.C. § 103 in view of Klein and Amidi. Pet. 18–27. Patent Owner disputes Petitioner's position, arguing that a person of ordinary skill in the art would not have had reason to combine the references in the manner proposed by Petitioner (PO Resp. 28) and further that the combination of the references fails to teach or suggest all of the claim limitations (*id.* at 4–5, 22–28).

We have reviewed the Petition, the Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers. For reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 1, 16, 17, 24, 30, and 31 of the '536 patent are unpatentable as obvious over the combination of Klein and Amidi.

1. Overview of Klein

Klein discloses a method for bus capacitance reduction. Ex. 1006, Abstract. According to Klein, data bus capacitance is reduced by decoupling unaccessed memory circuits from a data bus during data transfers to or from other memory circuits. *Id.* One embodiment in Klein provides memory controller 22 connects to circuitry 26 for interfacing with one or more memory circuits 28, as shown in Figure 3, reproduced below. *Id.* ¶ 28, Fig. 3.

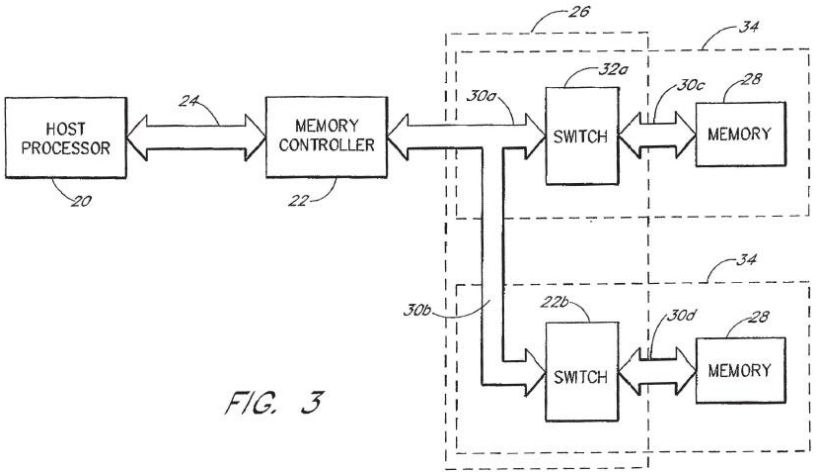

Figure 3 is a schematic of a bus switch that couples or decouples memory elements 28 and memory controller 22.

Figure 3 illustrates that the data bus between memory controller 22 and memory elements 28 may comprise several branches 30a, 30b, one for each separate memory element 28. *Id*. Each branch may include switch 32a, 32b, that may be used to selectively isolate portions (30c, 30d) of the data bus running from memory controller 22 to circuitry memory element 28. *Id*. Klein states that memory circuit 28 may be a conventional DRAM integrated circuit. *Id*. ¶ 29. According to Klein, the embodiment shown in Figure 3 may reduce the parasitic capacitance that the memory controller needs to charge and discharge during data transfers because a portion of the data bus and the stray capacitance of unaccessed memory circuits are removed. *Id*. ¶ 28.

Another embodiment in Klein is illustrated in Figure 6, reproduced below.

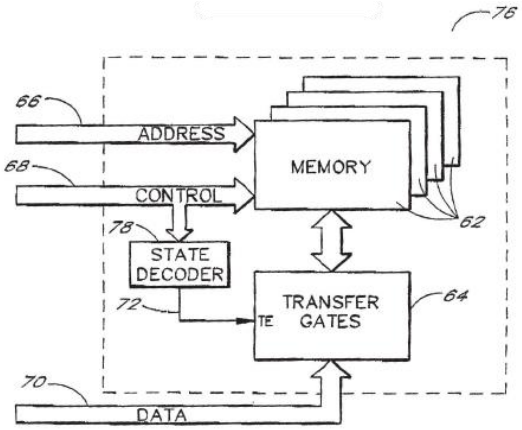

Figure 6 is a schematic of a memory module with memory elements that connect to an integrated circuit with transfer gates and state decoder.

As shown in Figure 6, a circuit is provided on memory module 76 that includes transfer gates 64 and state decoder 78. Ex. 1006 ¶¶ 35, 39. Klein discloses that state decoder 78 includes inverter 80 (*id.* ¶ 36), and that "the state decoder 78 could comprise a state machine 84 made with a programmable gate array for example" (*Id.* ¶ 37). Also, Klein teaches that the state decoder may be implemented as a state machine. *Id.* ¶ 37, Fig. 8.

Klein further discloses control logic circuitry, data buffer registers, and a bus switch that is incorporated into memory modules. *Id.* ¶¶ 29, 39, 40; Figs. 3, 10. According to Klein, the integrated circuit and a transfer gate output are connected to data buffer registers. *Id.* ¶ 40, Fig. 10.

2. Overview of Amidi

Amidi discloses a memory interface system with a processor, a memory controller, and a memory module. Ex. 1008 ¶ 3. According to Amidi, a prior art memory interface system is shown in Figure 1, reproduced below.

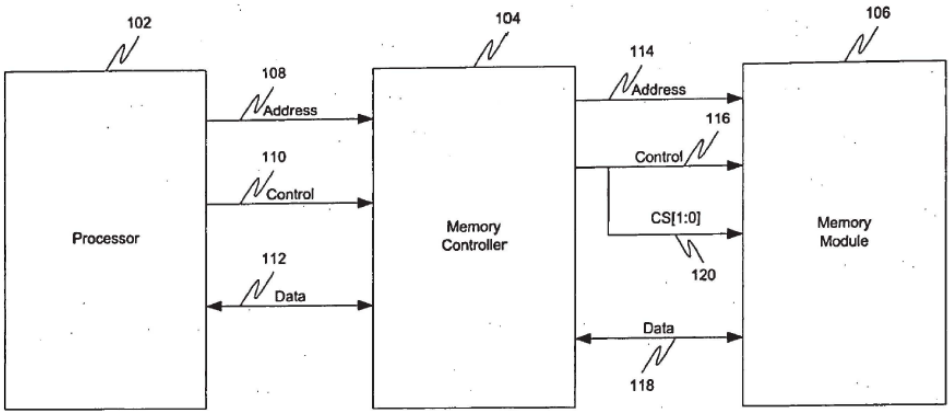

Figure 1 is a schematic of a standard prior art memory interface system.

The prior art system in Figure 1 includes memory module 106 with controller address bus 114, controller control signal bus 116, and controller data bus 118. *Id*. ¶ 3, Fig. 1. As illustrated in Figure 1, memory module 106 communicates with memory controller 104 via busses 114, 116, 118. *Id*. at Fig. 1. Amidi teaches that each stack of DDR memory devices has a data signal line and a data strobe line DQS. *Id*. ¶ 32, Fig. 2. Amidi also teaches that at least two DDR memory devices are connected to a common data memory bus. *Id*. ¶ 34, Fig. 3.

Amidi further discloses multiple memory devices mounted on the front and back side of memory module 400 as shown in Figure 4A reproduced below. *Id*. ¶¶ 34, 37.

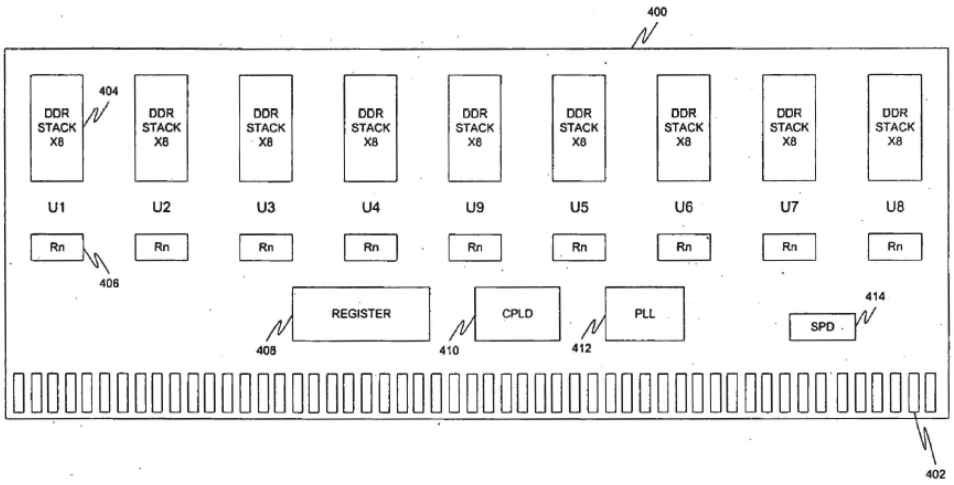

Figure 4A is a schematic of a DDR memory module.

Figure 4A illustrates one embodiment of Amidi where memory module 400 includes memory devices 404, resistor network 406, register 408, complex programmable logic device (CPLD) 410, phase-locked loop (PLL) 412, and SPD 414[5]. *Id.* According to Amidi, memory module 400 receives input signals, including address (Add(n)) signals, row address strobe (RAS) signal, column address strobe (CAS) signal, and bank address (BA[1:0]) signals. Ex. 1008 ¶ 50, Fig. 6A.

Another embodiment of Amidi's memory interface system is shown in Figure 6A, reproduced below.

[5]Amidi discloses that SPD 414 is a simple "I2C interface EEPROM [Electrically Erasable Programmable Read-Only Memory] to hold information regarding memory module for BIOS during the power-up sequence." Ex. 1008 ¶ 40.

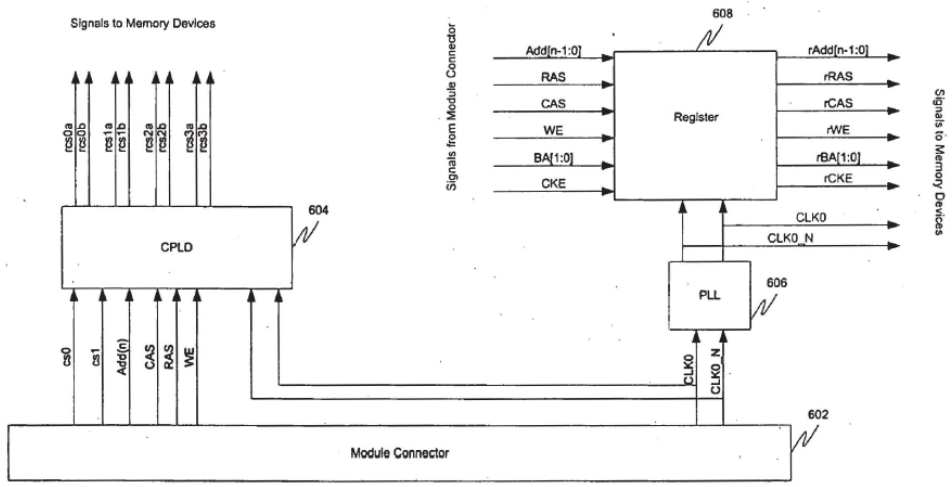

Figure 6A is a schematic of a row address decoding system for a transparent four rank memory module.

As illustrated in Figure 6A, module connector 602 sends signals to CPLD 604, PLL 606, and register 608. *Id*. CPLD 604 also ensures that all commands for a two rank memory module conveyed by module connector 602 are performed on the four rank memory modules. *Id*. ¶ 52. Amidi explains that the system chip select signals control the ranks of individual memory modules. *Id*. ¶¶ 2, 3.

3. Analysis

a. Klein and Amidi Teach or Suggest All the Recited Limitations of Independent Claims 1 and 24

Petitioner contends the combined disclosures of Klein and Amidi, as summarized above, teach or suggest each limitation of independent claims 1, and 24 of the ’536 patent. Petitioner first argues that the system described in Klein includes a switch and switch control circuitry interfacing with memory circuits, and, therefore, is a disclosure of a circuit electrically coupled to DDR memory devices. Pet. 18–19 (citing Ex. 1006 ¶ 32). Petitioner then explains that Klein discloses a circuit that is mounted on a memory module and includes a state decoder that may comprise a programmable logic

device. *Id*. at 13, 22–24; *see* Ex. 1006 ¶ 35). Petitioner also contends that Amidi discloses a circuit mounted on a memory module, where the circuit includes a logic element, a register, and a phase-lock loop device. *Id*. at 22–24 (citing Ex. 1008 ¶¶ 37; 43, 50, 52, Figs. 4A, 6A); Ex. 1011 ¶¶ 58, 64. According to Petitioner, Amidi discloses a memory module having one or more ranks of double-data-rate (DDR) memory devices, which are electrically coupled to the components of the circuit (CPLD). Pet. 23–24 (citing Ex. 1008, ¶¶ 43, 44, 50, 52, Fig. 6A).

Petitioner then argues that Amidi discloses CPLD 604, which activates one of the four ranks with memory devices 306 ("plurality of DDR memory circuits are configured to be activated concurrently with one another for receiving and transmitting data") in response to four chip-select signals that are generated from two input chip-select signals CS0, CS1, and address signal Add(n). *Id*. at 20, 23–24 (citing Ex. 1008 ¶¶ 43, 52, Fig. 6A). According to Petitioner, Amidi also discloses that PLL generates CLKO and CLKO_N signals ("phase-locked clock signals") with the chip select signals (rcs0, rcs 1, rcs2, rcs3) and relays them to memory devices 306. *Id*. at 21–22, 23–24 (citing Ex. 1008 ¶¶ 50, 52, Fig. 6A). CLKO and CLKO_N signals are also provided to the register and CPLD. *Id.* Petitioner argues that both CPLD 604 and PLL 606 receive clock signals (CLKO and CLKO_N) from module connector 602. *Id.* at 23–24 (citing Ex. 1008, Fig. 6A). Petitioner's declarant, Dr. Jagannathan, opines that a person of skill in the art would have recognized that the CPLD could receive the clock signals from the PLL. Ex. 1011 ¶ 71.

Finally, Petitioner argues that Klein teaches a circuit that can "selectively isolate" a load because Klein discloses bus switches 32a and

32b ("the circuit") that selectively couple data bus segment 30c of memory circuit 28 to input data bus segments 30a, 30b, and decouple ("selectively isolates") data bus segment 30d of another memory circuit ("a load of the DDR memory circuits of at least one rank") from the input data bus 30a, 30b that is connected to the memory controller. Pet. 22–23 (citing Ex. 1006 ¶¶ 28, 31, 38, Fig. 6A); Ex. 1011 ¶¶ 72, 98. Petitioner notes Klein specifically states that "[d]ata bus capacitance is reduced by decoupling unaccessed memory circuits from a data bus during data transfers to or from other memory circuits." Pet. 22 (citing Ex. 1006, Abstract).

According to Petitioner, a person of ordinary skill in the art would have been motivated to combine the teachings of Klein and Amidi, because (1) both references relate to memory devices, (2) both references describe coupling or isolating memory device loads, and (3) the combined teachings would result in the benefit of isolating a memory device load from a computer system so as to reduce parasitic capacitance and increase the speed at which memory accesses can be performed. *Id.* at 26 (citing Ex. 1008 ¶¶ 38, 39, 43, 44, 62; Ex. 1006 ¶¶ 5–10, 28); Ex. 1011 ¶¶ 99, 101.

Petitioner supports its position with the Declaration of Dr. Jagannathan, who testifies that a person of ordinary skill in the art would have had reason to apply the bus switch of Klein to the circuit architecture of Amidi in order to reduce the load seen by the memory controller. Ex. 1011 ¶ 99. Dr. Jagannathan further opines that one of ordinary skill implementing the teachings of Klein would have understood that using a circuit that allows for emulating a higher memory density configuration with lower memory density devices provides the predictable benefit of a cheaper implementation as taught by Amidi. *Id*. ¶ 101.

Patent Owner contests Petitioner's position, arguing that the combination of Amidi and Klein fails to teach or suggest all the recited claim limitations of claims 1 and 24 and that a person of ordinary skill in the art would not have had a reason to combine the disclosures of the cited references. PO Resp. 25–32.

Patent Owner first contends that Klein fails to teach or suggest "selectively isolate a load of DDR memory circuits," as recited in the challenged claims. PO Resp. 4–5. Patent Owner argues that different portions of Klein should not be joined together to meet the claim limitations directed to "address signals and a second number of DDR chip-select signals" because a person of ordinary skill in the art would not conflate the embodiments disclosed in Figures 6, 7, and 9 of Klein. *Id.* at 5. According to Patent Owner, Figures 6, 7, and 9 of Klein "are disclosed disparately and their conflation would destroy an intended design purpose of Figure 6 as Klein makes clear." *Id.* (citing Ex. 1006 ¶¶ 35, 36, 38; Ex. 2002 ¶¶ 98–103). Patent Owner explains that the embodiments illustrated in Figures 5, 6, and 9 of Klein could not be combined without going against the design purpose of Figure 6, which is to avoid an "unconventional" signal line and to not require modification of a DRAM to memory controller interface. *Id.* at 5–11.

Patent Owner relies on the Declaration of Dr. Sechen to support its position. Dr. Sechen testifies that "[a person of ordinary skill in the art] would have understood that the intended purpose of Klein's Fig. 6 is to promote interoperability by omitting unconventional signals." Ex. 2002 ¶ 99 (citing Ex. 1006 ¶ 35). According to Dr. Sechen, memory module 60 of Figure 5 has an unconventional signal line because gate control signal 72 is

received as an input to memory module 60, whereas in Figure 6, gate control signal 72 is generated in memory module 76 by state decoder 78. *Id.* ¶ 100 (citing Ex. 1006, Figs. 5, 6). Dr. Sechen then testifies that in Figure 6, there is no unconventional signal line for gate control (e.g., gate control signal 72) that needs to be created and routed to the memory module. *Id.* (citing Ex. 1006 ¶ 35). Dr. Sechen further states:

> Even if one moved the Fig. 9 circuitry of Klein into the Fig. 6 circuitry somehow, Dr. Jagannathan's position—that Klein discloses selecting a memory module in response to the chip-select signal from the state decoder 78 of Fig. 6 and in response to address bus 87 from the decode circuit 86 of Fig. 9—would lead directly to an inoperable circuit. In this strange case, two sets of TE signals would be generated, one based on control signals and one based on address signals, with no clear way to determine which is the correct TE signal to use for any given set of address and control signals. There is no reasonable way for this to lead to a properly functioning circuit.

Id. ¶ 101. Dr. Sechen, thus, concludes that a person of ordinary skill in the art would not have understood Klein to include selecting a memory module in response to the chip-select signal from state decoder 78 of Figure 6 and in response to address bus 87 from decode circuit 86 of Figure 9, because it would be contrary to Klein's intended purpose. *Id.* ¶ 102.

We are not persuaded by Patent Owner's contentions that Klein's switch is incapable of using address signals *in addition* to chip select signals. We do not find the embodiments illustrated in Figures 4, 5, 6, 7, and 9 to be disparate embodiments that teach away from each other. Rather, we agree with Petitioner's position that Klein provides a variety of design examples that are intended to be versatile in their application. *See* Pet. 12. In particular, we credit the testimony of Dr. Jagannathan who explains the

various applications of Klein's teachings and how they would function together. *See e.g.,* Ex. 1026 ¶¶ 19–21 (Supplemental Declaration of Dr. Srinivasan Jagannathan).

Furthermore, we disagree with Patent Owner's contention that the intended design purpose of Klein is to avoid using an unconventional signal line for switch control. *See* PO Resp. 5–11. To the contrary, Klein specifically states that its design purpose is to reduce the parasitic capacitance of a data bus (i.e., capacitive load) (s*ee* Ex. 1006 ¶ 10), and we credit the testimony of Dr. Jagannathan, who explains that combining the decoder circuit of Klein Figures 6 and 9 does not destroy this stated purpose (Ex. 1026 ¶ 44). Additionally, the description of Figure 6 does not support Patent Owner's position regarding Klein's intended purpose, because Klein teaches merely that "[t]his embodiment has the advantage that no unconventional signal line for gate control needs to be created and routed to the memory module." *See* Ex. 1001 ¶ 35 (emphasis added), Fig. 6. Noting a design advantage is not the same as indicating a design purpose. *See e.g., In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004) (reference does not teach away if it merely expresses a general preference for an alternative invention, but does not "criticize, discredit, or otherwise discourage" investigation into the invention claimed).

Patent Owner then contends that Amidi fails to teach or suggest "selectively isolate a load of DDR memory circuits," as recited in the challenged claims. PO Resp. 22–28. Patent Owner specifically argues that Amidi discloses only permanent hard-wiring of all four memory ranks to a data bus and that choosing a rank of memory devices while inactivating other ranks is not selectively isolating a load of DDR memory circuits,

because neither involves electrical separation from the computer system. *Id.* at 22–23. Patent Owner asserts that direct hard-wiring is permanent, does not allow for separation, and is not subject to acts of selectively isolating (i.e., it does not respond to a selection). *Id.* at 23. Patent Owner, thus, concludes that hard-wiring between the memory ranks and the data bus is a permanent electrical connection that cannot be "selectively isolate[d]." *Id.*

Patent Owner further argues that the proper kind of isolation specified by the challenged claims is load isolation, not merely any kind of isolation, such as some kind of rank-inactivation isolation. *Id.* at 24. According to Patent Owner, a person of ordinary skill in the art would understand that load isolation is directed specifically to the issue of electrical loading. *Id.* (citing Ex. 2002 ¶ 67). Patent Owner concludes that "[d]ue to the permanent hard-wiring of the memory device's data pin to its line of Amidi's 72-line data bus, its electrical load is always electrically connected, not separated nor isolated, regardless of any rank activation or inactivation in Amidi. *Id.* at 25.

We do not agree with Patent Owner's position that hard-wired data signal lines cannot be electrically isolated in a selective fashion. As discussed above, we construe "selectively isolate" as "electrical separation of a selected component from another component." *See supra*, Section II.A. Amidi's disclosure of directing electrical signals down a specific signal line or data bus in order to electrically activate a rank within the memory devices and electrically inactivate other ranks falls within the scope of the term "selectively isolate" as we have construed the term. We are further unpersuaded by Patent Owner's argument that "selectively isolate" is limited narrowly to a particular kind of load isolation. The '536 patent defines the

term "load" broadly and includes "*without limitation*, electrical load, such as capacitive load, inductive load, or impedance load." Ex. 1001, 5:39–41 (emphasis added). Thus, Patent Owner's arguments are not commensurate with the '536 patent definition of "load" or with the scope of the challenged claims.

Patent Owner also contends that Klein and Amidi are improperly combined by Petitioner. PO Resp. 28. Patent Owner explains that the Petitioner's combination is internally inconsistent and based on impermissible hindsight. *Id*. at 28–32. Specifically, Patent Owner argues that the combination of Klein and Amidi is inconsistent, because for a "first number of DDR chip-select signals" the Petitioner relies on off-module signals in Klein and on-module signals in Amidi. *Id*. at 29. According to Patent Owner, it would have been internally inconsistent and impossible to have the "first number of DDR chip-select signals:" be both off-module on-module. *Id*. at 29–30.

Again, we do not agree with Patent Owner. Rather, we agree with Petitioner's position and we find that Klein's Figure 10 indicates that the switch and control logic can be incorporated *inside* each memory device, and therefore need not be generated *off*-module. *See* Ex. 1006 ¶¶ 39, 40, Fig. 10; Ex. 1025, 69:13–70:16 (Dr. Sechen's Deposition Transcript); Reply 16. Klein Figure 10's teachings demonstrates that the control logic of Figures 7–9 can be combined and even incorporated inside individual memory devices. Patent Owner has not provided sufficient rationale as to why the control signal circuitry shown in Figures 4 and 9 cannot be implemented on module in conformance with Klein's teachings that "all of the circuitry shown in FIG. 3 may be placed on a single IC, or may be

provided in a multi-chip package." Ex. 1006 ¶ 29. Therefore, we are satisfied that use of off-module signals in Klein and on-module signals in Amidi would not be inconsistent with the teachings of Klein.

Finally, Patent Owner contends that a person of ordinary skill in the art would not combine Klein and Amidi because there is a conflict of which "transfer enable" or TE signal to use at Klein's transfer gates. PO Resp. 31–32 (citing Ex. 2002 ¶¶ 107, 108, 109). Patent Owner relies on the Declaration of Dr. Sechen to support its position regarding the inoperability of a Klein-Amidi combination. *See* Ex. 2002 ¶¶ 107–109. Dr. Sechen specifically states that:

> I see that the Patent Owner has identified a technical problem: "a conflict of which TE signal to use at Klein's transfer gates," a TE signal from state decoder 78 in Fig. 6 or a TE signal from decode circuit 86 in Fig. 9. (Prelim. Resp., 32.) A [person of ordinary skill in the art] would recognize that such a conflict would not make technical sense, further indicating that the Petitioner and Board are misreading Klein.

Id. ¶ 108. Patent Owner concludes that resolving such a conflict would (i) require undue experimentation by a person of ordinary skill in the art, (ii) change the operating principle of Klein's transfer gates, and (iii) introduce purposeless redundancy, which would not be obvious to a person of ordinary skill in the art. PO Resp. 32.

We are not persuaded by Patent Owner's position. Rather, we are satisfied that Klein, specifically, teaches timing control of a transfer gate switch. *See* Ex. 1006 ¶ 23, Fig. 1. We credit the testimony of Dr. Jagannathan, who testifies that Klein teaches how to time the opening and closing of a transfer gate switch. Ex. 1026 ¶¶ 46, 47 (citing Ex. 1006, Fig. 1). Dr. Jagannathan, further testified that "when Klein refers to a 'signal'

used in any of the circuits taught therein, one of ordinary skill would understand it is 'a varying electrical impulse that conveys information from one point to another.'" Ex. 1011 ¶ 89; *see e.g.*, Ex. 1026 ¶¶ 45–47. Thus, we are not persuaded that Amidi's CS signal and Klein's TE ('transfer enable") signal are not equivalent in their signaling function, or that the teachings of Amidi and Klein would not have been combinable to one of ordinary skill in the art, because a person of ordinary skill in the art would have known how to address the timing control for a transfer gate switch based on the teachings of Klein. *See e.g.*, Ex. 1009 ¶ 26 (explaining that transistors are turned on by asserting the gates 15 via an input "transfer enable" signal line labeled TE in Figure 2 and that bus switch circuits such as that illustrated in Figure 2 are known to those of skill in the art).

The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art. *Id*. Patent Owner has not argued that Klein and Amidi teach away from each other. Also, we credit the testimony of Dr. Jagannathan, who states that "[i]t would have been obvious to one of ordinary skill that this teaching of Klein can be applied to Amidi, whereby these elements may be incorporated into a memory integrated circuit." Ex. 1011 ¶ 99. Therefore, we are persuaded that the teachings of Klein and Amidi are combinable.

Based on the evidence of record, we agree with Petitioner's position that challenged independent claims 1 and 24 would have been obvious over Klein and Amidi. First, we are persuaded by Petitioner's reasoning and the

evidentiary record that Klein discloses a switch and switch control circuitry that are provided on a memory module. We are further persuaded that Amidi teaches a circuit with a logic element and PLL that is mounted on a memory module and that is electrically coupled to four memory ranks made of a plurality of DDR memory devices. We also are persuaded that the teachings of Klein could have been implemented using the circuitry disclosed in Amidi so as to selectively isolate a load of the DDR memory devices from a computer system in response at least in part to a set of signals as required in the challenged claims. Additionally, we credit the testimony of Dr. Jagannathan that a person of ordinary skill in the art would have had a reason to combine the teachings of Klein and Amidi, which both relate to memory devices, such as DIMMS and describe isolating memory device loads. *See* Ex. 1011 ¶¶ 99, 101.

Second, despite Patent Owner's argument to the contrary (*see* PO Resp. 33–35), the arguments presented by Patent Owner generally attack the references individually, rather than in combination. Nonobviousness cannot be established by attacking the references individually when a challenge is predicated upon a combination of prior art disclosures. *See In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d at 425). In attacking the references individually, Patent Owner fails to address Petitioner's actual challenges and establish an insufficiency in the combined teachings of the references and show Petitioner has not met its burden in arguing obviousness of the challenged claims.

Lastly, we note that the testimony of Patent Owner's Declarant, Dr. Sechen, is based on the claim constructions proffered by Patent Owner and not on the constructions set forth in the Decision to Institute. *Compare* Ex.

2002 ¶¶ 38–72, *with* Dec. to Inst. 8–10. We have considered, however, the relevant portions of Dr. Sechen's analysis regarding the prior art and alleged non-obviousness of the claims and accorded the appropriate weight to that particular testimony.

Accordingly, we hold that Petitioner has shown by a preponderance of the evidence that independent claims 1 and 24 of the '536 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Klein and Amidi.

b. Klein and Amidi Teach or Suggest All the Recited Limitations of Dependent Claims 16, 17, 30, and 31

Claim 16 depends from claim 1 and recites "[t]he circuit of claim 1, wherein the memory module has attributes." Ex. 1001, 42:46–51. Petitioner contends the combined disclosures of Klein and Amidi, as summarized above, teach or suggest each limitation of dependent claims 16, 17, 30, and 31 of the '536 patent. Pet. 34–36. Petitioner specifically contends that Amidi references JEDEC21 C 4-20-4 and Amidi discloses JEDEC compliant DDR DIMMS. *Id.* at 34. According to Petitioner JEDEC21C 4-20-4 defines the specifications for DDR DIMMs, and discloses attributes associated with the plurality of DDR memory devices. *Id.* Thus, Petitioner concludes that Amidi in view of JEDEC21 C 4-20-4 teaches the further limitations of dependent claim 16. *Id.*

Claim 17 depends from claim 16 and recites a circuit of claim 16, wherein the attributes are selected from a group consisting of: a number of row addresses, a number of column addresses, a number of DDR memory circuits, a data width of the DDR memory circuits, a memory density per DDR memory circuit, a number of ranks, and a memory density per

rank. Ex. 1001, 42:52–57. Petitioner contends Amidi and Klein meet the limitations of claim 17, because Amidi teaches the following:

> the memory module has at least the following attributes: a number of row addresses, a number of column addresses, thirty-six memory devices ("a number of DDR memory circuits"), 8 data bits ("a data width per DDR memory circuit"), 16 M Byte memory density per memory device ("a memory density per DDR memory circuit"), four ranks (rank 0, rank 1, rank 2, rank 3) ("a number of ranks of DDR memory circuit"),

Id. at 36 (citing Ex. 1008 ¶ 8). According to Petitioner, it would have been obvious to one of ordinary skill in the art that the attributes include at least the number of row address signals. *Id.* (citing Ex. 1001 ¶ 57).

Claims 30 and 31 are method claims that are substantially the same as claims 16 and 17. Ex. 1001, 43:63–44:6.

Patent Owner does not provide separate contentions regarding additional limitations recited in the dependent claims. *See generally* PO Resp.

After consideration of the language recited in claims 16, 17, 30, and 31 of the '536 patent, the Petition, the Patent Owner Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers, we find that one of ordinary skill in the art would have considered these dependent claims obvious over the combination of Klein and Amidi. Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that dependent claims 16, 17, 30, and 31 of the '536 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Klein and Amidi.

F. Asserted Obviousness of Claims 16, 17, 30, and 31 in view of Klein, Amidi, and Dell

Petitioner contends claims 16, 17, 30, and 31 of the '536 patent are unpatentable under 35 U.S.C. § 103 in view of Klein, Amidi, and Dell. Pet. 27–33. Patent Owner disputes Petitioner's position, arguing that Dell fails to make up for the deficiencies of Klein and Amidi with respect to certain claim limitations. PO Resp. 35–36.

We have reviewed the Petition, the Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers. For reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 16, 17, 30, and 31 of the '536 patent are unpatentable as obvious over the combination of Klein, Amidi, and Dell.

1. Overview of Klein

See Section II.D.1., discussed above.

2. Overview of Amidi

See Section II.D.2., discussed above.

3. Overview of Dell

Dell discloses a system for address re-mapping for memory modules using presence detect data. Ex. 1009, Abstract. Dell discloses a memory module having a presence detect (PD) that allows a four bank memory device to be used with a computer system that is expecting a two bank memory device. *Id.* at 3:30–33; 4:55–58. The PD data provides the operational characteristics and compatibility with system requirements of the memory module. *Id.* at 2:8–12. Dell discloses that memory module 20, shown in Figure 1 reproduced below, includes logic circuit 24 that interfaces

with memory controller 14 of CPU system 12 using address, data, and bus control signals. *Id.* at 3:66–4:5, 3:40–42.

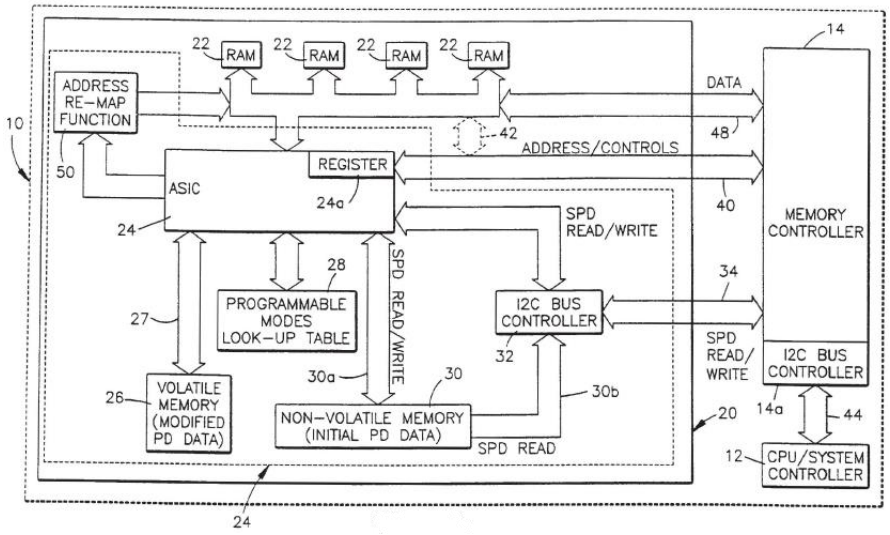

Figure 1 is a schematic of memory module 20 connected to computer system 12.

As illustrated in Figure 1, memory module 20 includes a plurality of memory devices being configured as memory banks 22. *Id.* at 2:48–51. The memory devices may be DDR synchronous DRAM (SDRAM). *Id.* at 1:56–67. Dell discloses that memory module 20 includes non-volatile memory 30 for storing serial PD (SPD) data that is accessible to system controller 12. *Id.* at 5:28–32. Memory module 20 includes volatile memory 26 for storing modified PD data that is transferred from CPU system 12 based on system requirements. *Id.* at 7:5–16.

4. Analysis

Claim 16 depends from claim 1 and recites "[t]he circuit of claim 1, wherein the memory module has attributes." Ex. 1001, 42:46–51. Petitioner contends that Dell discloses a memory module with attributes, because the memory module of Dell has (1) presence detect (PD) data, and (2) memory device characteristics determined from serial presence detect (SPD) data.

Pet. 27. Claim 16 further requires "the circuit in the at least one configuration is further configured to store data accessible to the computer system." Petitioner contends that Dell discloses that non-volatile memory 30 stores serial presence detect (SPD) data that is accessible to system controller 12, thereby meeting the required elements of claim 16. *Id*. at 28.

Claim 17 depends from claim 16 and recites a circuit of claim 16, wherein the attributes are selected from a group consisting of: a number of row addresses, a number of column addresses, a number of DDR memory circuits, a data width of the DDR memory circuits, a memory density per DDR memory circuit, a number of ranks, and a memory density per rank. Ex. 1001, 42:52–57. Petitioner contends Dell meets the limitations of claim 17, because Dell discloses that a SDRAM 22 uses twelve address signals A0-A11 and Dell discloses storing modified PD data as the up-to-date PD data and performing an address-remapping function 50. Pet. 31.

Claims 30 and 31 are method claims that are substantially the same as claims 16 and 17. Ex. 1001, 43:63–44:6.

According to Petitioner, a person of ordinary skill in the art would have been motivated to combine the teachings of Klein, Amidi, and Dell, because (1) all three references relate to memory devices, and (2) a person of skill in the art would have been motivated to use the non-volatile memory and volatile memory in Dell with the SPD in Amidi and the switches of Klein to have a higher density memory device using a number of lower density memory devices that are comparatively inexpensive and readily available. *Id*. at 32–33 (citing Ex. 1008 ¶ 8; Ex. 1009, 4:55–58); Ex. 1011 ¶¶ 99, 101.

Petitioner supports its position with the Declaration of Dr. Jagannathan, who testifies that using lower memory density devices poses the challenge of reporting a different configuration to the memory controller. Ex. 1011 ¶ 102. According to Dr. Jagannathan, Dell teaches a solution to that problem. *Id*. Thus, Dr. Jagannathan concludes that one of ordinary skill would seek to apply Dell to Amidi to further improve an actual memory system for emulating a different configuration expected by a host system. *Id*.

Patent Owner contends that Dell fails to curer the deficiencies Patent Owner perceives in Klein and Amidi. PO Resp. 35–36. Therefore, Patent Owner concludes that dependent claims 16, 17, 30, and 31 would not have been rendered obvious for the same reasons cited by Patent Owner in its arguments against the combination of Klein and Amidi. *Id*.

After careful consideration of the language recited in claims 16, 17, 30, and 31 of the ’536 patent, the Petition, the Patent Owner Response, and Petitioner’s Reply, as well as the relevant evidence discussed in those papers, we find that for the same reasons discussed in detail previously (*see supra*, Section II.D.3), one of ordinary skill in the art would have considered these dependent claims obvious over the combination of Klein, Amidi, and Dell. Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that dependent claims 16, 17, 30, and 31 of the ’536 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Klein, Amidi, and Dell.

III. CONCLUSION

We conclude Petitioner has shown by a preponderance of the evidence that claims 1, 16, 17, 24, 30, and 31 of the '536 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of (1) Klein and Amidi and (2) Klein, Amidi, and Dell.

IV. ORDER

For the reasons given, it is

ORDERED that, by a preponderance of the evidence, claims 1, 16, 17, 24, 30, and 31 of the '536 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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