

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

DIABLO TECHNOLOGIES, INC.,  
Petitioner,

v.

NETLIST, INC.,  
Patent Owner.

---

Case IPR2014-00882  
Patent 7,881,150 B2

---

Before LINDA M. GAUDETTE, BRYAN F. MOORE, and  
GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

BRADEN, *Administrative Patent Judge*.

FINAL WRITTEN DECISION  
*35 U.S.C. § 318 and 37 C.F.R. § 42.73*

## I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6(c). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of US Patent No. 7,881,150 B2 (Ex. 1001, “the ’150 patent”) are unpatentable.

### A. Procedural History

Diablo Technologies, Inc. (“Petitioner”) filed a Corrected Petition (Paper 5, “Pet.”) to institute an *inter partes* review of claims 15–17, 22, 24, 26, and 31–33 of the ’150 patent. Netlist, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 9, “Prelim. Resp.”). Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of all challenged claims on the following grounds alleged in the Petition.

References	Basis	Claims Challenged
Amidi <sup>1</sup> and Klein <sup>2</sup>	§ 103	15–17, 22, 24, 26, and 31–33
Amidi and Wiggers <sup>3</sup>	§ 103	15–17, 22, 24, 26, and 31–33

Paper 11 (“Dec. to Inst.”), 33.

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 25, “PO Resp.”), to which Petitioner filed a Reply (Paper 27, “Reply”). An oral argument was held on July 28, 2015, consolidated with

---

<sup>1</sup> US Patent Publication No. 2006/0117152 A1, pub. June 1, 2006 (filed Jan. 5, 2004) (“Amidi,” Ex. 1008).

<sup>2</sup> US Patent Publication No. 2001/0008006 A1, pub. July 12, 2001 (“Klein,” Ex. 1009).

<sup>3</sup> US Patent No. 6,011,710, iss. Jan. 4, 2000 (“Wiggers,” Ex. 1010).

IPR2014-00882  
Patent 7,881,150 B2

the oral hearings for IPR2014-00883 and IPR2014-01011. *See* Paper 30. A transcript (“Tr.”) of the oral argument is included in the record. Paper 31.

### *B. Related Proceedings*

Petitioner informs us that the ’150 patent is involved in the following federal district court cases: *Diablo Technologies, Inc. v. Netlist, Inc.*, Case No. 4:13-CV-03901-YGR (N.D. Cal.); and *Netlist, Inc. v. Smart Modular Technologies*, Case No. 4:13-CV- 05889-YGR (N.D. Cal.). Paper 10, 1. In addition, Petitioner filed two other petitions requesting *inter partes* review of the ’150 patent and related U.S. Patent No. 8,081,536 B1. *Id.* at 2. These cases are: IPR 2014-00883 and IPR2014-01011. *Id.* We consolidated the oral hearings for IPR2014-00882, IPR2014-00883, and IPR 2014-01011. *See* Paper 30.

Petitioner further informs us that related US Patent Nos. 7,619,912 and 7,636,274 are the subjects of *inter partes* reexamination (95/000,578 and 95/001,337). Pet. 10–11. Petitioner also informs us that related U.S. Patent No. 7,289,386 is the subject of district court case *Google, Inc. v. Netlist, Inc.*, Case No. C 08-4144 SBA (N.D. Cal.). *Id.* at 14–15.

### *C. The ’150 Patent*

The ’150 patent relates to a memory module of a computer system with improved performance and memory capacity. Ex. 1001, 1:30–34. Memory module 10 includes a plurality of memory devices 30 (arranged in ranks 32) and circuit 40. *Id.* at 4:56–65; Fig. 1. Circuit 40 is electrically coupled to the memory devices 30 and memory controller 20 of a computer system. *Id.* The memory module improves performance and memory capacity by isolating electrical loads of the memory devices from the computer system. *Id.* at 4:65–66.

Circuit 40 receives input signals from memory controller 20. *Id.* Figure 1, reproduced below, illustrates input signals (corresponding to a number of memory devices) from memory controller 20, such as chip select signals (“cs#”), that are directed to memory module 10, which can act as a virtual memory module. *Id.* at 16:47–57; Figs. 1, 9A, 9B.

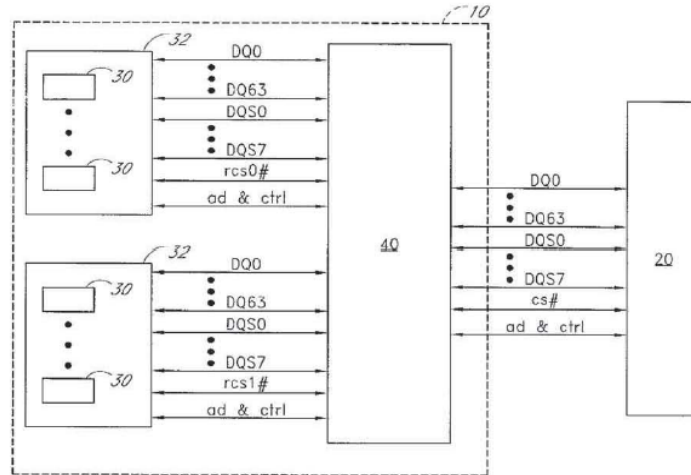


Figure 1 is a schematic of a memory module with circuit 40 and memory devices 30 and connectable to memory controller 20.

As shown in Figure 1 above, based on the received input signals from memory controller 20, circuit 40 generates output signals corresponding to memory devices 30 on the memory module. *Id.* at Fig. 1. The output signals include a different number of chip select signals (e.g., “rcs0#” and “rcs1#”) corresponding to memory devices 30 shown in ranks 32. *Id.* at 16:66–17:4; Fig. 1.

Circuit 40 includes a logic element, such as a programmable logic device (PLD), an application-specific integrated circuit (ASIC), a field programmable gate array (FPGA), or a complex programmable-logic device (CPLD). Ex. 1001, 6:4–18. As shown in Figure 9A, reproduced below, circuit 40 may also include register 230 and phase-lock loop device (PLL) 220. *Id.* at 15:35–41; Fig. 9A.

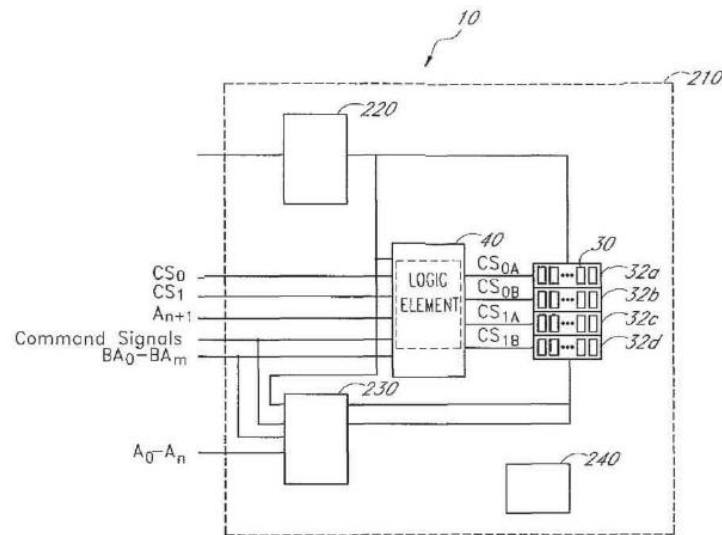


Figure 9A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system.

Figure 9A above illustrates circuit 40 receiving a set of input command signals, address signals ( $A_{n+1}$ ), including bank address signals ( $BA_0$ - $BA_m$ ), row address signals ( $A_0$ - $A_n$ ), column address signals, gated column address strobe signals, and chip-select signals ( $CS_0$ ,  $CS_1$ ), from memory controller 20 of the computer system. Ex. 1001, 16:24-29, 17:11-26. In response to the set of input address and command signals, circuit 40 generates a set of output address and command signals. *Id.* at 16:31-33.

With the output address and command signals, circuit 40 isolates the electrical loads of some memory devices 30 from the computer system. *Id.* at 6:48-62. According to the '150 patent, load isolation may result in specific benefits including reduced load related to data signal lines. *Id.* at 14:34-40. In order to isolate the loads, the logic element of circuit 40 translates between a system memory domain of the computer system and a physical memory domain of memory module 10. *Id.* at 6:48-62. As shown in Figure 3, reproduced below, the circuit isolates the load of a memory

device by isolating one or both of DQ data signal lines 102a, 102b of two memory devices 30a and 30b from common DQ data signal line 112 that is coupled to the computer system. *Id.* at 6:63–7:2, Fig. 3A.

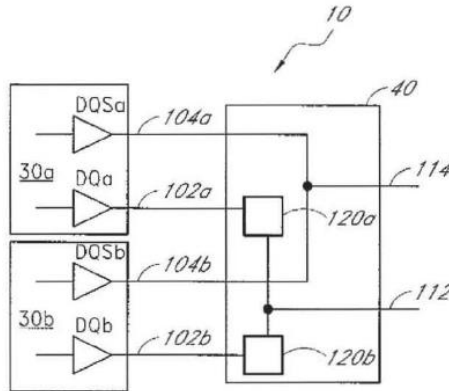


Figure 3A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system.

Circuit 40, shown in Figure 3A above, can electrically couple one or both of DQ data signal lines 102a, 102b of memory devices 30a and 30b to common data signal line 112, at the same time. *Id.* at 7:22–26; Fig. 3A. Circuit 40 also allows a DQ data signal to be transmitted from memory controller 20 of the computer system to one or both of DQ data signal lines 102a, 102b. *Id.* at 7:2–5. The logic element of circuit 40 uses switches 120a, 120b in order to isolate or couple one or both of DQ data signal lines 102a, 102b of memory devices 30a and 30b from common data signal line 112. *Id.* at 7:2–12.

#### D. Illustrative Claim

As noted above, *inter partes* review was instituted for claims 15–17, 22, 24, 26, and 31–33 of the '150 patent, of which claims 15, 22, and 31 are independent claims. Claim 15 is illustrative of the challenged claims and is reproduced below:

15. A circuit configured to be mounted on a memory module so as to be electrically coupled to a first double-data-rate (DDR) memory device having a first data signal line and a first data strobe line, to a second DDR memory device having a second data signal line and a second data strobe line, and to a common data signal line, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals comprising row address signals, column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit comprising:

a logic element;

a register;

a phase-lock loop device configured to be operationally coupled to the first DDR memory device, the second DDR memory device, the logic element, and the register,

wherein the circuit is configurable to be responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain has a first memory density per memory device, and the physical memory domain has a second memory density per memory device less than the first memory density per memory device.

Ex. 1001, 42:41–43:2.

## II. DISCUSSION

### A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 (Fed. Cir. 2015) (“Congress implicitly approved the broadest reasonable interpretation standard in enacting the AIA,” and “the standard was properly adopted by

PTO regulation.”). Under this standard, claim terms generally are given their ordinary and customary meaning, as understood by one of ordinary skill in the art in the context of the patent’s entire written disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Yet a “claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history.” *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002).

In the Decision to Institute, we construed the terms “Memory Module,” “Circuit Configured to be Mounted on a Memory Module,” and “Selectively Electrically Coupling,” which are recited in all the challenged independent claims. *See* Dec. to Inst. 7–12. During the course of the trial, Patent Owner argued for altered constructions of these claim terms. PO Resp. 5–16. Therefore, we address these contentions and construe each claim term as discussed below.

1. “*Memory Module*”

In the Decision to Institute, we construed the term “memory module,” as “a plurality of memory devices and a circuit” thereby encompassing “additional circuitry and multiple printed circuit boards.” Dec. to Inst. 7–9.

Petitioner agrees with the construction set forth in the Decision to Institute. Reply 4; Tr. 5:25–6:10. Patent Owner, however, contends that “memory module” should be construed as “a packaging arrangement of one or more memory device(s) for use in a computer socket.” PO Resp. 5; Tr. 47:5–7. According to Patent Owner, the construction of “memory module” in the Decision to Institute is unreasonably broad, because it is inconsistent with the ordinary and customary meaning of the term as it would be



understood by a person of ordinary skill in the art. PO Resp. 6–10. Patent Owner argues the Board erred by construing the term by analyzing each component of the word separately (*id.* at 6) and relying on the ’150 patent specification (Tr. 47:17–20), whereas a person of ordinary skill in the art would have understood “memory module” to be a term of art (PO Resp. 6; Ex. 2002 ¶ 54 (Declaration of Dr. Carl Sechen)). Patent Owner explains that under the Board’s construction of “memory module,” the term would encompass a memory controller and associated memory devices. PO Resp. 10.

Patent Owner further contends that the Board’s construction of “memory module” is inconsistent with the ’150 patent disclosure. *Id.* at 11. Patent Owner notes that claims 15, 22, and 31 recite “the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals.” *Id.* (emphasis omitted). According to Patent Owner, due to the use of different terms in the ’150 patent, “memory module” would not be read as including the ’150 patent’s “memory controller” by a person of ordinary skill in the art. *Id.*; Ex. 2002 ¶ 59.

We are charged with interpreting claim terms according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Additionally, when construing claim terms, we “should also consult the patent’s prosecution history in proceedings in which the patent has been brought back to the [U.S. Patent and Trademark Office] for a second review.” *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015). Yet, we must be careful not to improperly import limitations into the claims or to read a particular

embodiment appearing in the written description into the claim, if the claim language is broader than the embodiment. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

The specification of the '150 patent does not define explicitly the term “memory module.” The specification does, however, teach embodiments that describe a memory module as comprising a plurality of memory devices on a carrier and a circuit. Ex. 1001, 2:63–64; 3:7–9; 4:59–63. In another embodiment, a memory module comprises (i) a printed circuit board on which memory devices are mounted, (ii) a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and (iii) a plurality of electrical conduits which electrically couple the memory devices to the circuit and which electrically couple the circuit to the edge connectors. *Id.* at 5:24–32. The '150 patent also teaches that memory modules in the disclosed embodiments are compatible with at least single in-line memory modules (SIMMS) and dual in-line memory modules (DIMMS). *Id.* at 5:32–39.

Although the embodiments disclosed in the '150 patent are instructive, the claims recite language broader than that found in the embodiments. *See In re Van Geuns*, 988 F.2d at 1184. Therefore, we decline to adopt Patent Owner’s claim construction as it would import limitations improperly from the specification into the claims and unnecessarily limit the scope of the claims. We credit, however, the testimony of Patent Owner’s Declarant, Dr. Sechen, who explains the state of the art and the customary meaning of “memory module” as it would be understood by one of ordinary skill in the art to encompass at least a “removable circuit board, cartridge, or other carrier that contains one or

more RAM memory chips.” *See* Ex. 2002 ¶¶ 41–59. Therefore, we modify the construction of “memory module” from that set forth in the Decision to Institute, wherein we construed the term as “a plurality of memory devices and a circuit” that “encompasses additional circuitry and multiple printed circuit boards.” Dec. to Inst. 9. Rather, we construe the term “memory module” as “one or more memory devices on a carrier,” because such a construction is consistent with the disclosure of the ’150 patent and with the ordinary and customary meaning of “memory module.”

2. “*Selectively Electrically Coupling*”

In the Decision to Institute, we construed the term “selectively electrically coupling,” as “making a selection between at least two components so as to transfer power or signal information from one component to at least one other component.” Dec. to Inst. 9–11.

Petitioner agrees with the construction set forth in the Decision to Institute. Reply 4; Tr. 5:25–6:10. Patent Owner, however, contends that “selectively electrically coupling” should be construed as “electrically coupling in response to a selection.” PO Resp. 13–16; Tr. 70:4–9. According to Patent Owner, the Board’s construction is unreasonably broad, whereas its proffered construction is more consistent with the disclosure of the ’150 patent. PO Resp. 15 (citing Ex. 1001, 5:29–30, 7:22; Ex. 2002 ¶¶ 68–69). Patent Owner specifically argues that “electrically coupling” in the ’150 Patent is provided by a structural pathway for electricity, and this is also consistent with the meaning of “electrically coupling” as a term of art. *Id.* (citing Ex. 2002 ¶ 68). Patent Owner further argues that a person of ordinary skill in the art would understand the act of electrically coupling to

take place between strictly two components, between which a structural pathway for electricity would be formed. *Id.*

We are unpersuaded by Patent Owner's position. The specification of the '150 patent does not define explicitly the term "selectively electrically coupling." Therefore, we refer to its ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d at 1257 (Fed. Cir. 2007). A technical dictionary, the IEEE Dictionary,<sup>4</sup> defines "electrical coupling" as "[e]lectrical charges in conductors of a disturbed circuit formed by electrical induction." Ex. 3001. The IEEE Dictionary explains that "[s]ince the ratio of a conductor's electrostatic charge to the potential difference between conductors (required to maintain that charge) is the general definition of capacitance, electrical coupling is also called capacitive coupling." *Id.* The IEEE Dictionary defines "coupling capacitance (1) (ground systems)" ("capacitive coupling") as "[t]he association of two or more circuits with one another by means of capacitance mutual to the circuits." Ex. 3002. We understand this to mean that the two or more circuits are associated in such a way that power or signal information may be transferred from one circuit to another. The Oxford English Dictionary defines "selectively" as "[i]n a selective manner; by selection." Ex. 3003. The Oxford English Dictionary also defines "select" as "[t]o choose or pick out in preference to another or others." Ex. 3004.

---

<sup>4</sup> IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, Standards Information Network, IEEE Press (2000).

Accordingly, we modify slightly the construction from the Decision to Institute of “selectively electrically coupling,” as “making a selection between at least two components so as to transfer power or signal information from one selected component to at least the other selected component,” because such a construction is consistent with the ordinary and customary meaning of “selectively electrically coupling.”

3. “*Circuit Configured to be Mounted on a Memory Module*”

In the Decision to Institute, we construed the term “a circuit configured to be mounted on a memory module,” to encompass “circuitry configured to be mounted on at least a portion of a memory module.” Dec. to Inst. 11–12. Such a construction is consistent with the ordinary and customary meaning of “a circuit configured to be mounted on a memory module.” *Id.* at 12.

Petitioner agrees with the construction set forth in the Decision to Institute. Reply 4; Tr. 5:25–6:10. Patent Owner, however, contends that “a circuit configured to be mounted on a memory module” should be construed as “an entire circuit configured to be mounted on a single memory module.” PO Resp. 11–13; Tr. 68:1–18.

Patent Owner notes that our claim construction, as set forth in the Decision to Institute, is ambiguous in that it can be read two ways:

One might read the Board’s construction as meaning that the circuit is mounted on and occupies at least a portion of the memory module (Ex. 2002, ¶ 62), which may be consistent with Netlist’s construction. On the other hand, one might read the Board’s construction as encompassing portions of the circuit to be mounted off-module, which would be unreasonably broad to a [person of ordinary skill in the art].

*Id.* at 11 (citing Ex. 2002 ¶ 62). According to Patent Owner, “memory module” is a term of art that would have had a well-understood meaning to a person of ordinary skill in the art at the time of the invention and a person of ordinary skill in the art would not have understood “a circuit configured to be mounted on a memory module” to include circuit parts off of that memory module or on a different memory module. *Id.* at 12 (citing Ex. 2002 ¶ 60). Patent Owner contends that such a construction could include situations that defeat the purpose of a memory module to make removing and installing memory upgrades easy and error-free. *Id.* (citing Ex. 2002 ¶ 61).

We decline to adopt Patent Owner’s claim construction as it is inconsistent with the definition of “circuit” as found in the specification of the ’150 patent. The ’150 patent defines “circuit” as “a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.” Ex. 1001, 5:9–13. The ’150 patent does not limit a “circuit” to only a configuration of electrical components or devices that are mounted on a single memory module. Therefore, applying the broadest reasonable interpretation consistent with the specification of the ’150 patent, we construe the claim element “a circuit configured to be mounted on a memory module,” as we did in the Decision to Institute, but we further clarify the construction to encompass “at least a portion of circuitry configured to be mounted on at least a portion of a memory module.”

#### *4. Other Claim Terms*

We determine that no express constructions of any other claims terms are required for our analysis, and we apply the ordinary and customary meaning of each claim term.

#### *B. Principles of Law*

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

We analyze the instituted grounds of unpatentability in accordance with the above-stated principles.

#### *C. Level of Ordinary Skill in the Art*

In determining whether an invention would have been obvious at the time it was made, we determine the level of ordinary skill in the pertinent art at the time of the invention. *Graham*, 383 U.S. at 17. “The importance of resolving the level of ordinary skill in the art lies in the necessity of

maintaining objectivity in the obviousness inquiry.” *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner’s Declarant, Srinivasan Jagannathan, Ph.D. (“Dr. Jagannathan”), testifies that a person of ordinary skill in the art at the time of the ’150 patent:

would understand basic memory and data communication concepts, with a bachelor’s degree in any of electrical engineering, computer engineering, computer science, or related field. Course work for one of ordinary skill in the art would have included a course on computer organization, principles of digital design, or computer architecture. One of ordinary skill in the art would also have around one year of experience related to computer memory systems. For example, such experience may include experience in DRAM memory technology and related industry standards such as JEDEC standards for DRAM memories and memory modules.

Ex. 1007 ¶ 53. Patent Owner’ Declarant, Carl Sechen, Ph.D. (“Dr. Sechen”), testifies that one of ordinary skill in the art at the time of the ’150 patent would have had an undergraduate degree in electrical engineering or computer engineering, at least two years of professional experience in the design of memory systems, familiarity with the latest JEDEC standard specifications for memory devices and modules, and familiarity with the latest DRAM memory devices widely available in the market. Ex. 2002 ¶ 14. Dr. Sechen further testifies that a person of ordinary skill in the art would have design proficiency in memory modules comprising DDR memory technology, such as memory modules with JEDEC standard DDR SDRAM devices. *Id.* ¶ 15.

Based on our review of the ’150 patent and the types of problems and solutions described in the ’150 patent and cited prior art, we conclude a



person of ordinary skill in the art at the time of the '150 patent would have a Bachelor's degree in electrical engineering, computer engineering, computer science, or related field, and at least one year of work experience, including familiarity with computer memory systems and related industry standards such as JEDEC standards for DRAM memories and memory modules. We further note that the applied prior art reflects the appropriate level of skill at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

*D. Expert Testimony*

Patent Owner argues that Petitioner's Declarant, Dr. Jagannathan, does not qualify as a person of ordinary skill in the art at the time of the invention because of his alleged lack of experience designing memory modules. PO. Resp. 16–17. According to Patent Owner, Dr. Jagannathan's experience and background is directed to software and is not relevant to the case. *Id.* at 18–23. Patent Owner argues that, unlike Dr. Jagannathan, its Declarant Dr. Sechen has significant practical experience designing memory modules. *Id.* at 18; Ex. 2001 ¶¶ 3, 4, Exhibit A.

As to his hardware and memory design experience, Dr. Jagannathan was awarded a Doctorate degree in Computer Science, and has two decades of experience in the design, development, and analysis of a wide range of hardware, software, network and database systems. Ex. 1007 ¶ 2. He has designed and implemented hardware virtual memory caches, and researched theoretical performance measures of various cache coherency protocols. *Id.* Dr. Jagannathan also stated during his deposition that he has experience in the design of memory systems. Ex. 2003, 124:12–126:1. Patent Owner contends, however, that Dr. Jagannathan fails to qualify as a person of

ordinary skill in the art because he lacks sufficient professional experience physically designing (i.e., “actually putting down a design and saying this is what it would be”) a memory module. PO Resp. 21 (citing Ex. 2003, 125:14–17). We disagree.

To testify as an expert under FRE 702, a person need not be a person of ordinary skill in the art, but rather must be “qualified in the pertinent art.” *Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008); *see SEB S.A. v. Montgomery Ward & Co.*, 594 F.3d 1360, 1372–73 (Fed. Cir. 2010) (upholding a district court’s ruling to allow an expert to provide testimony at trial because the expert “had sufficient relevant technical expertise” and the expert’s “knowledge, skill, experience, training [and] education . . . [wa]s likely to assist the trier of fact to understand the evidence”); *Mytee Prods., Inc. v. Harris Research, Inc.*, 439 F. App’x 882, 886–87 (Fed. Cir. 2011) (non-precedential) (upholding admission of the testimony of an expert who “had experience relevant to the field of the invention,” despite admission that he was not a person of ordinary skill in the art). We find that, although Dr. Jagannathan is less experienced than Dr. Sechen in the area of memory module design, he is qualified sufficiently to testify as an expert witness about memory systems and memory modules.

*E. Alleged Obviousness of Claims 15–17, 22, 24, 26, and 31–33 in view of Amidi and Klein*

Petitioner alleges claims 15–17, 22, 24, 26, and 31–33 of the ’150 patent are unpatentable under 35 U.S.C. § 103 over the combination of Amidi and Klein. Pet. 22–44. Patent Owner disputes Petitioner’s position, arguing that a person of ordinary skill in the art would not have had reason to combine the references in the manner proposed by Petitioner (PO Resp.

35) and further that the combination of the references fails to teach or suggest all of the claim limitations (*id.* at 25–35, 44–47, 56–58).

We have reviewed the Petition, the Patent Owner Response, and Petitioner’s Reply, as well as the relevant evidence discussed in those papers. For reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of the ’150 patent are unpatentable as obvious over the combination of Amidi and Klein.

### 1. Overview of Amidi

Amidi discloses a memory interface system with a processor, a memory controller, and a memory module. Ex.1008 ¶¶ 2, 3. According to Amidi, a prior art memory interface system is shown in Figure 1, reproduced below.

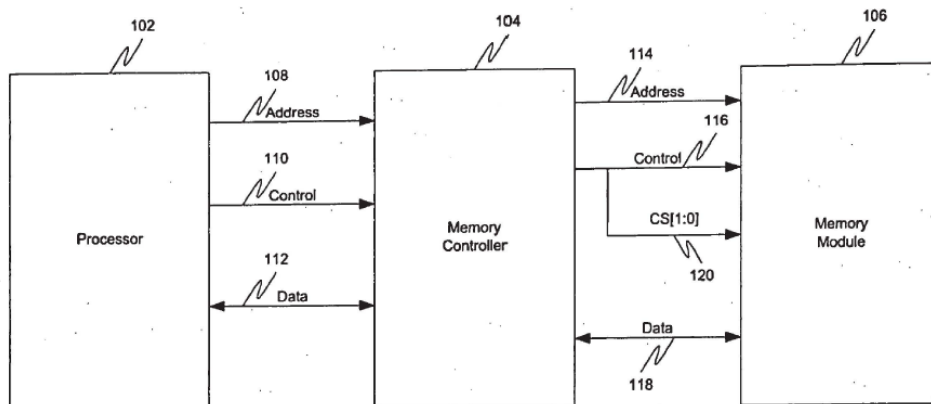


Figure 1 is a schematic of a standard prior art memory interface system.

The prior art system in Figure 1 includes memory module 106 with controller address bus 114, controller control signal bus 116, and controller data bus 118. *Id.* ¶ 2, Fig. 1. As illustrated in Figure 1, memory module 106 communicates with memory controller 104 via busses 114, 116, 118. *Id.* at Fig. 1. Amidi teaches that each stack of DDR memory devices has a data

signal line and a data strobe line DQS. *Id.* ¶ 32; Fig. 2. Amidi also teaches that at least two DDR memory devices are connected to a common data memory bus. *Id.* ¶ 34; Fig. 3.

Amidi further discloses multiple memory devices mounted on the front and back side of memory module 400 as shown in Figure 4A reproduced below. *Id.* ¶¶ 34, 37.

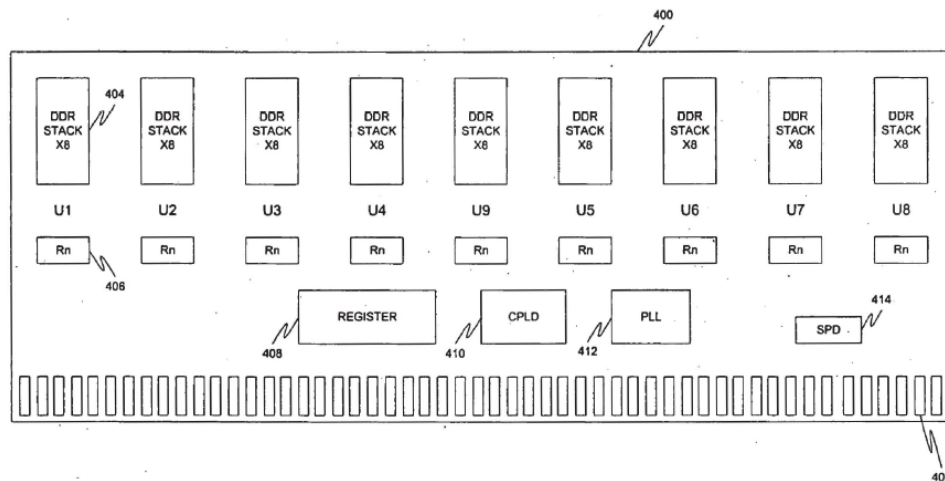


Figure 4A is a schematic of a DDR memory module.

Figure 4A, above, illustrates one embodiment of Amidi where memory module 400 includes memory devices 404, resistor network 406, register 408, complex programmable logic device (CPLD) 410, phase-locked loop (PLL) 412, and SPD 414<sup>5</sup>. *Id.* According to Amidi, memory module 400 receives input signals, including address (Add(n)) signals, row address strobe (RAS) signal, column address strobe (CAS) signal, and bank address (BA[1:0]) signals. Ex. 1008 ¶ 50; Fig. 6A.

<sup>5</sup> Amidi discloses that SPD 414 is a simple “I2C interface EEPROM [Electrically Erasable Programmable Read-Only Memory] to hold information regarding memory module for BIOS during the power-up sequence.” Ex. 1008 ¶ 40.

Another embodiment of Amidi's memory interface system is shown in Figure 6A, reproduced below.

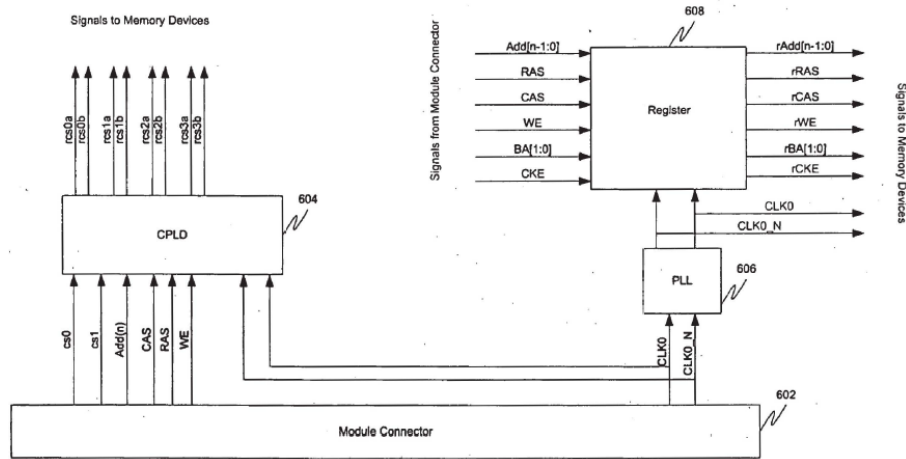


Figure 6A is a schematic of a row address decoding system for a transparent four rank memory module.

As illustrated in Figure 6A above, module connector 602 sends signals to CPLD 604, PLL 606, and register 608. *Id.* CPLD 604 also ensures that all commands for a two rank memory module conveyed by module connector 602 are performed on the four rank memory modules. *Id.* ¶ 52. Amidi explains that the system chip select signals control the ranks of individual memory modules. *Id.* ¶¶ 2, 3.

## 2. Overview of Klein

Klein discloses a method for bus capacitance reduction. Ex. 1009, Abstract. According to Klein, data bus capacitance is reduced by decoupling unaccessed memory circuits from a data bus during data transfers to or from other memory circuits. *Id.* One embodiment in Klein provides memory controller 22 connects to circuitry 26 for interfacing with one or more memory circuits 28, as shown in Figure 3, reproduced below. *Id.* ¶ 28; Fig. 3.

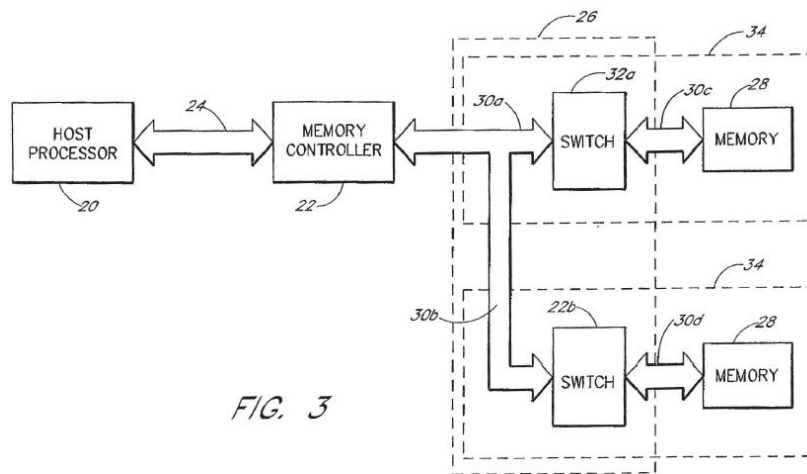


Figure 3 is a schematic of a bus switch that couples or decouples memory elements 28 and memory controller 22.

Figure 3, above, illustrates that the data bus between memory controller 22 and memory elements 28 may comprise several branches 30a, 30b, one for each separate memory elements 28. *Id.* Each branch may include switch 32a, 22b that may be used to selectively isolate portions (30c, 30d) of the data bus running from memory controller 22 to memory circuitry 28. *Id.* Klein states that memory circuit 28 may be a conventional DRAM integrated circuit. *Id.* ¶ 29. According to Klein, the embodiment shown in Figure 3 may reduce the parasitic capacitance that the memory controller needs to charge and discharge during data transfers because a portion of the data bus and the stray capacitance of unaccessed memory circuits are removed. *Id.* ¶ 28.

Another embodiment in Klein is illustrated in Figure 6, reproduced below.

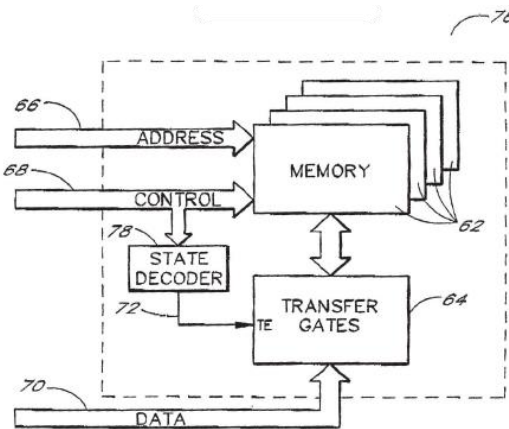


Figure 6 is a schematic of a memory module with memory elements that connect to an integrated circuit with transfer gates and state decoder.

As shown in Figure 6, a circuit is provided on memory module 76 that includes transfer gates 64 and state decoder 78. Ex. 1009 ¶¶ 35, 39. Klein discloses that state decoder 78 includes inverter 80 (*Id.* ¶ 36), and that “the state decoder 78 could comprise a state machine 84 made with a programmable gate array for example” (*Id.* ¶ 37). Also, Klein teaches that the state decoder may be implemented as a state machine. *Id.* ¶ 37, Fig. 8.

Klein further discloses control logic circuitry, data buffer registers, and a bus switch are incorporated into memory modules. *Id.* ¶¶ 29, 39, 40; Figs. 3, 10. According to Klein, the integrated circuit and a transfer gate output are connected to data buffer registers. *Id.* ¶ 40; Fig. 10.

### 3. Analysis

#### a. Amidi and Klein Teach or Suggest All the Recited Limitations of Independent Claims 15, 22, and 31

Petitioner contends the combined disclosures of Amidi and Klein, as summarized above, teach or suggest each limitation of independent claims 15, 22, and 31 of the '150 patent. Pet. 22–44. Petitioner first argues that Amidi discloses a circuit mounted on a memory module, where the circuit

includes a logic element, a register, and a phase-lock loop device. *Id.* at 23 (citing Ex. 1008 ¶¶ 2, 37; Figs. 4A, 6A); Ex. 1007 ¶¶ 58, 64; Reply 12.

According to Petitioner, the system described in Amidi includes a memory module having one or more ranks of double-data-rate (DDR) memory devices, which are electrically coupled to the components of the circuit (CPLD). Pet. 24–25 (citing Ex. 1008, Figs. 4A, 4B, 6A); Reply 12–13.

Petitioner then explains that Klein also discloses a circuit that is mounted on a memory module and includes a state decoder that may comprise a programmable logic device. Pet. 23–24 (citing Ex. 1009 ¶ 35). Petitioner contends that Klein’s disclosure of circuitry interfacing with memory circuits is a disclosure of a circuit electrically coupled to DDR memory devices. *Id.* at 25.

Petitioner then argues that Amidi discloses the following claim limitations: (i) memory devices having data signal lines and data strobe lines (Ex. 1008 ¶¶ 29, 32; Figs. 2, 3); (ii) stacks of DDR memory devices having a data signal line and a data strobe line DQS (*id.* ¶ 32; Fig. 3); and (iii) at least two DDR memory devices connected to the same (common) memory bus (“common data signal line”) (*id.* ¶¶ 34–35; Fig. 3). Pet. 27. According to Petitioner, a person of ordinary skill in the art would recognize that each DDR memory device has its own data bus and that they are connected to a common data signal line, and therefore, the circuit of Amidi is “electrically coupled” to the common data bus. *Id.* (citing Ex. 1009 ¶¶ 61, 63, 65, 72); Reply 13–14. Petitioner further argues that Klein discloses that bus switch 33 is electrically coupled to output data buses 31c, 31d, 31e, 31f and to a single input data bus 31a (i.e., the “common data signal line”). Pet. 27–28 (citing Ex. 1009 ¶¶ 28, 29); Ex. 1007 ¶¶ 80, 83.



Petitioner provides arguments that the sending and receiving of input signals by the systems occurs in Amidi and Klein, and explains how each reference teaches a circuit that is responsive to such input signals. Pet. 28–43. Petitioner specifically argues that Amidi teaches a circuit that is “responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line.” Petitioner makes this argument because Amidi teaches that CPLD 404, 604 is responsive to a set of input signals (address signal Add(b) and chip select signals cs0, cs1) to determine (“selectively electrically coupling”) an active rank of the four ranks while inactivating the other three ranks of memory devices from the computer system. *Id.* at 33 (citing Ex. 1008 ¶¶ 43, 44, 62); Ex. 1007 ¶ 72). Petitioner’s Declarant, Dr. Jagannathan, in the Supplemental Declaration (“Ex. 1023”), testifies that when Amidi’s CPLD provides a chip select signal to a rank of memory devices, the signal selects the rank and thereby causes the rank to be coupled to the data bus. Ex. 1023 ¶ 32. According to Petitioner, the act in Amidi of activating one rank and sending a chip select signal to that rank while inactivating other ranks constitutes “selectively coupling” and “selectively isolating.” Pet. 33–36. Petitioner also argues that Klein teaches “selectively isolating,” because Klein discloses that bus switches 32a and 32b (“the circuit”) respond to control lines 68 (“the set of input signals”) to disconnect (“selectively isolating”) one of two output data buses 30c and 30d (“one or more loads of the DDR memory devices”) from input data bus 30a. *Id.* at 36; Reply 16–17.

According to Petitioner, a person of ordinary skill in the art would have been motivated to combine the teachings of Amidi and Klein, because (1) both references relate to memory devices, such as DIMMS, (2) both references describe coupling or isolating memory device loads, and (3) the combined teachings would result in the benefit of isolating a memory device load from a computer system so as to reduce parasitic capacitance and increase the speed at which memory accesses can be performed. Pet. 43–44 (citing Ex. 1008 ¶¶ 38, 39, 43, 44, 62; Ex. 1009 ¶¶ 9, 10,<sup>6</sup> 28); Ex. 1007 ¶¶ 89, 91.

Petitioner supports its position with the Declaration of Dr. Jagannathan, who testifies that a person of ordinary skill in the art would have reason to apply the bus switch of Klein to the circuit architecture of Amidi in order to reduce the load seen by the memory controller. Ex. 1007 ¶ 91. Dr. Jagannathan further opines that one of ordinary skill implementing the teachings of Klein would understand that using a circuit that allows for emulating a higher memory density configuration with lower memory density devices provides the predictable benefit of a cheaper implementation as taught by Amidi. *Id.* Dr. Jagannathan notes that Klein specifically teaches how to control the timing of a data bus switch (e.g., the transfer gate switch in Figure 1) and teaches a variety of ways for generating control signals for data bus switches. Ex. 1023 ¶¶ 40–43, 46, 47. According to Dr. Jagannathan, a person of ordinary skill in the art seeking to implement the bus switch of Klein in the memory module of Amidi would have understood

---

<sup>6</sup> The Petitioner cites to Ex. 1009, 1:33–2:18, which appears to correspond to paragraphs 9 and 10 of Klein.

the timing relationships between the chip select signal and when the data is communicated over the data signal lines, because such relationships are dictated by the JEDEC standards (which is cited by Amidi). *Id.* ¶ 45; *see* Ex. 1008 ¶ 7.

Patent Owner contests Petitioner’s position, arguing that the combination of Amidi and Klein fails to teach or suggest all the recited claim limitations and that a person of ordinary skill in the art would not have had a reason to combine the disclosures of the cited references. PO Resp. 25–32, 35–47.

Patent Owner first contends that the combination of Amidi and Klein fails to teach or suggest a “circuit configured to be mounted on a memory module[,] . . . the circuit . . . selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal to the common data signal line,” as recited in the challenged claims. *Id.* at 25–28. Specifically, Patent Owner contends that Petitioner misapplies the prior art because claims 15 and 31 require a “circuit” to perform the “selectively electrically coupling” and the “circuit” is distinct from the claimed “DDR memory device.” *Id.* at 27. Thus, according to Patent Owner, any internal switching function “inside the memory device,” does not meet the claimed “circuit” performing the “selectively electrically coupling.” *Id.*

Patent Owner further contends that Amidi’s disclosure of hard-wiring of all four memory ranks to a data bus constitutes permanent coupling, so that choosing a rank of memory devices does not alter the coupling between data signal lines. *Id.* at 29. Patent Owner argues that direct hard-wiring is static and permanent, and does not respond to a selection. *Id.* at 29–30.

Patent Owner adds to this argument by contending that “electrically couple” is provided by structure so there is a pathway for electricity, which is different from Amidi’s signal transmission that directs signals down a specific signal line or data bus and constitutes a transmitted flow of electricity. PO Resp. 32 (citing Ex. 1001, 5:29–30; Ex. 2002 ¶ 82).

According to Patent Owner, “[a] pathway for electricity (as for “selectively electrically coupling” in the ’150 Patent) is not a flow of electricity (as for Amidi’s ‘directing signals’).” *Id.* Patent Owner, thus, concludes that Amidi fails to meet the challenged claim limitations because hard-wiring between the memory ranks and the data bus is a permanent coupling and cannot be “selectively electrically coupling.” *Id.* at 30–31.

We do not agree with Patent Owner. Rather, based on the definition of circuit discussed above (*see* Section II.A.3) and as supported by the ’150 patent (*see* Ex. 1001, 5:9–13) and , we find that the combined disclosures of Amidi and Klein teach a “circuit . . . mounted on a memory module” that performs the “selectively electrically coupling” as recited by the challenged independent claims. Specifically, we find that Klein teaches a memory circuit that may be a conventional Dynamic Random Access (“DRAM”) integrated circuit (“IC”) and the DRAM IC may be part of a memory module that also incorporates a separate IC forming the bus switch. Ex. 1009 ¶ 29, Fig. 3. Thus, Klein teaches that the components of a circuit can be installed in a single integrated circuit and mounted on one memory module. *Id.* Therefore, Klein’s disclosure of a memory circuit meets the limitation of a “circuit . . . mounted on a memory module” that provides “selectively electrically coupling.”

Additionally, we are unpersuaded by Patent Owner’s argument that hard-wired data signal lines, such as that taught by Amidi, cannot be electrically coupled in a selective fashion. As discussed above, we construe “selectively electrically coupling” as “making a selection between at least two components so as to transfer power or signal information from one selected component to at least the other selected component.” *See supra* Section II.A.2. Amidi’s disclosure of directing signals down a specific signal line or data bus in order to determine an active rank within the memory devices falls within the scope of the term “selectively electrically coupling” as we have construed the term. Furthermore, Patent Owner’s Declarant, Dr. Sechen, testified that Klein discloses the use of MOSFET switches (i.e., data bus switches) for decoupling select memory circuits from the data bus. *See Ex. 1022, 49:16–50:18, 88:5–22.*

Patent Owner also contends that the combination of Amidi and Klein is improper and based on impermissible hindsight because Amidi’s CPLD output CS signal and Klein’s TE (“transfer enable”) signal are not equivalent due to difference in respective timing operation and purposes. PO Resp. 35–46; *see also* Ex. 1009 ¶ 26 (explaining that transistors are turned on by asserting the gates 15 via an input “transfer enable” signal line labeled TE in Figure 2 and that bus switch circuits such as that illustrated in Figure 2 are known to those of skill in the art.). Patent Owner argues that the specific implementation details, e.g., timing considerations, are critical, and a person of ordinary skill would have found an Amidi-Klein combination inoperable due to timing problems. *Id.* at 38 (citing Ex. 2002 ¶ 127). Patent Owner relies on the Declaration of Dr. Sechen to support its position regarding the

inoperability of an Amidi-Klein combination. *See* Ex. 2002 ¶¶ 127–130.

Dr. Sechen specifically states that:

due to standardized DDR memory device operation, a DDR read (or write) command's chip-select signal (*e.g.*, Amidi's CPLD output chip-select signal) does not coincide with its read (or write) data (*e.g.*, to be gated by Klein's TE signal). Thus, by failing to properly transfer the target data, the Petition's proposal—DDR chip-select signals from Amidi's CPLD = Klein's input TE signal—would malfunction and be inoperable.

*Id.* ¶ 127.

Patent Owner then argues that an Amidi-Klein combination is also inoperable because a DDR chip-select signal (as used in Amidi) is not designed to be a timing signal, whereas a timing signal is required for Klein's transfer gates to operate properly. PO Resp. 38–39. Patent Owner supports its position with the Declaration of Dr. Sechen, who testifies that “[f]undamentally, a DDR chip-select signal lacks enough timing information to indicate when to properly open and close Klein's transfer gates. Thus, a DDR chip-select signal, as output by Amidi's CPLD, would not be a usable signal at all for controlling Klein's transfer gates.” Ex. 2002 ¶ 128.

Again, we do not agree with Patent Owner. Rather, we agree with Petitioner's position and we find that the timing requirements for memory devices are dictated by the JEDEC standards, which were known to a person of ordinary skill in the art at the time of the '150 patent. *See e.g.*, Ex. 1008 ¶ 7. Additionally, Klein teaches both (i) the coordination of the signal between the chip-select signal and when the data is being received by the memory device, and (ii) to adjust the timing of the chip-select signals to control access to the device. *See* Ex. 1009 ¶¶ 22–23, Fig. 1. We also credit the testimony of Dr. Jagannathan, who testifies regarding the JEDEC21C-

4.5.7 standard as it relates to the 168 Pin Registered SDRAM DIMM Family of memory devices. *See e.g.*, Ex. 1007 ¶¶ 43–51. Dr. Jagannathan specifically testifies that

There is a Phase-Locked Loop (PLL) clock input provided to the register and to the memory devices. This is depicted in JEDEC21C-4.5.7, Figure as “PCK” input to the register, and as “CK0 \_ PLL” in the case of the memory devices. A phase-locked loop device receives an input clock signal and generates another clock signal whose phase matches (within tolerance) the input clock. The details of the PLL are specified in JEDEC21C-4.5.7 at p. 4.5.7-8. Specifically, the PLL clock output is depicted as driving a number of SDRAM devices and registers.

*Id.* ¶ 45.

The concept of a PLL would generally be well understood by one of ordinary skill in the art. For instance, Jacob teaches that “[t]he function of a PLL or DLL, in general, is to synchronize two periodic signals so that a certain fixed amount of phase-shift or apparent delay exists between them. The two are similar, and the terms are often used interchangeably.

*Id.* ¶ 46 (citing Ex. 1018, 11).

Thus, we find that a person of ordinary skill in the art would have known how to address the timing and use of chip-select signals so that the teachings of Klein would have been applicable to Amidi.

Moreover, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art. *Id.* We credit the testimony of Dr. Jagannathan, who states that “when Klein refers to a ‘signal’ used in any

of the circuits taught therein, one of ordinary skill would understand it is ‘a varying electrical impulse that conveys information from one point to another.’” Ex. 1007 ¶ 77; *see* Ex. 1023 ¶¶ 33–35. Thus, we are not persuaded that Amidi’s CS signal and Klein’s TE signal are not equivalent in their signaling function, or that the teachings of Amidi and Klein would not have been combinable to one of ordinary skill in the art.

Based on the evidence of record, we agree with Petitioner’s position that challenged claims 15–17, 22, 24, 26, and 31–33 would have been obvious over Amidi and Klein. First, we are persuaded by Petitioner’s reasoning and the evidentiary record that Amidi teaches a circuit mounted on a memory module that is electrically coupled to a first DDR memory device and a second DDR memory device. We are further persuaded that Amidi teaches a circuit with a logic element, a register, and a PLL. We also are persuaded that the teachings of Amidi could have been implemented using the common data signal line and switch system disclosed in Klein so that by (i) selectively electrically coupling a first data signal line to the common data signal line and (ii) selectively electrically coupling a second data signal line to the common data signal line, the circuit is responsive to a set of input signals. Additionally, we credit the testimony of Dr. Jagannathan that a person of ordinary skill in the art would have had a reason to combine the teachings of Amidi with Klein, which both relate to memory devices, such as DIMMS, and describe coupling or isolating memory device loads. *See* Ex. 1007 ¶¶ 89, 91; Ex. 1023 ¶ 45.

Second, the arguments presented by Patent Owner generally attack the references individually, rather than in combination. PO Resp. 25–32. Nonobviousness cannot be established by attacking the references



individually when a challenge is predicated upon a combination of prior art disclosures. *See In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986); *cf. Keller*, 642 F.2d at 426 (“[O]ne cannot show non-obviousness by attacking references individually where . . . the rejections are based on combinations of references.”). In attacking the references individually, Patent Owner again fails to address Petitioner’s actual challenges and establish an insufficiency in the combined teachings of the references and show Petitioner has not meet its burden in arguing obviousness of the challenged claims.

Lastly, we note that the testimony of Patent Owner’s Declarant, Dr. Sechen, is based on the claim constructions proffered by Patent Owner and not on the constructions set forth in the Decision to Institute. *Compare Ex. 2002 ¶¶ 38–72, with Dec. to Inst. 7–12.* We have considered as relevant, however, the portions of his analysis regarding the prior art and alleged non-obviousness of the claims and accorded the appropriate weight to that particular testimony.

Accordingly, we hold that Petitioner has shown by a preponderance of the evidence that claims 15, 22, and 31 of the ’150 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Amidi and Klein.

*b. Amidi and Klein Teach or Suggest All the Recited Limitations of Dependent Claims 16, 17, 24, 26, 32, and 33*

Claims 16, 24, and 32 recite “wherein the two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.” Ex. 1001, 43:3–5, 44:1–3, 44:58–60. Dependent claim 17 recites that the circuit includes “one or more switches selectively electrically

coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the one or more switches operatively coupled to the logic element to receive control signals from the logic element.” Dependent claim 33 recites a similar limitation. *Id.* at 43:6–12. Dependent claim 26 further recites that the claimed circuit is “configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system.” *Id.* at 44:8–11.

Petitioner contends the combined disclosures of Amidi and Klein, as summarized above, teach or suggest each limitation of dependent claims 16, 17, 24, 26, 32, and 33 of the ’150 patent. Pet. 22–44. Patent Owner does not provide separate contentions regarding additional limitations recited in the dependent claims. *See generally* PO Resp.

After consideration of the language recited in claims 16, 17, 24, 26, 32, and 33 of the ’150 patent, the Petition, the Patent Owner Response, and Petitioner’s Reply, as well as the relevant evidence discussed in those papers, we find that one of ordinary skill in the art would have considered these dependent claims obvious over the combination of Amidi and Klein. Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that claims 16, 17, 24, 26, 32, and 33 of the ’150 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Amidi and Klein.

*F. Asserted Obviousness of Claims 15–17, 22, 24, 26, and 31–33 in view of Amidi and Wiggers*

Petitioner contends claims 15–17, 22, 24, 26, and 31–33 of the ’150 patent are unpatentable under 35 U.S.C. § 103 in view of Amidi and

Wiggers. Pet. 44–57. Patent Owner disputes Petitioner’s position, arguing that a person of ordinary skill in the art would not have had reason to combine the references in the manner proposed by Petitioner (PO Resp. 47–58) and further that the combination of the references fails to teach or suggest all of the claim limitations (*id.* at 33–35).

We have reviewed the Petition, the Patent Owner Response, and Petitioner’s Reply, as well as the relevant evidence discussed in those papers. For reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of the ’150 patent are unpatentable as obvious over the combination of Amidi and Wiggers.

1. *Overview of Amidi*

See Section II.D.1. discussed above.

2. *Overview of Wiggers*

Wiggers discloses a system for a reduced capacitance memory system and increased propagation speed for data traveling both from a memory chip to a memory controller and in the reverse direction. Ex. 1010, 1:7–11; 3:17–19. One embodiment of the system disclosed in Wiggers is shown in Figure 3, reproduced below.

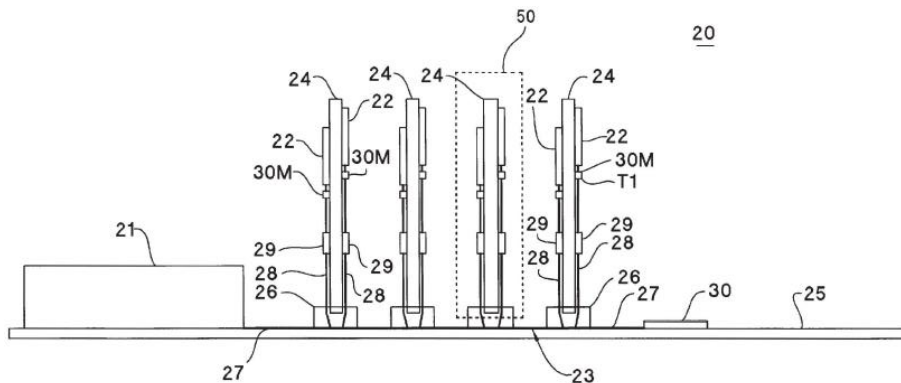


Figure 3 is a schematic of a memory system with memory controller 21, data bus 23, and memory devices 22.

As shown in Figure 3, a central processing unit (CPU) acts as dedicated memory controller 21 that is connected to data bus 23. *Id.* at 4:38–47. Memory controller 21 selectively accesses numerous memory devices 22 which are arranged either serially, in parallel, or in some combination of the two along the data bus 23. *Id.* at 4:47–50. According to Wiggers, the memory devices may include read only memory (ROM) or random access memory (RAM), or dynamic random access memory (DRAM). *Id.* at 4:50–53.

Wiggers further discloses memory devices 22 and switches 29 are preferably affixed to removable memory modules 24 that allow the memory system configuration to be easily changed by simply adding modules or by replacing some or all of the modules. Ex. 1010, 4:61–65. Further, Wiggers discloses switches 29 including field effect transistor (FET) type switches. *Id.* at 4:47–57. Switches 29 of Wiggers are electrically coupled to memory devices 22. *Id.* at 4:53–57.

An embodiment of memory module 24 is shown in Figure 5, reproduced below.

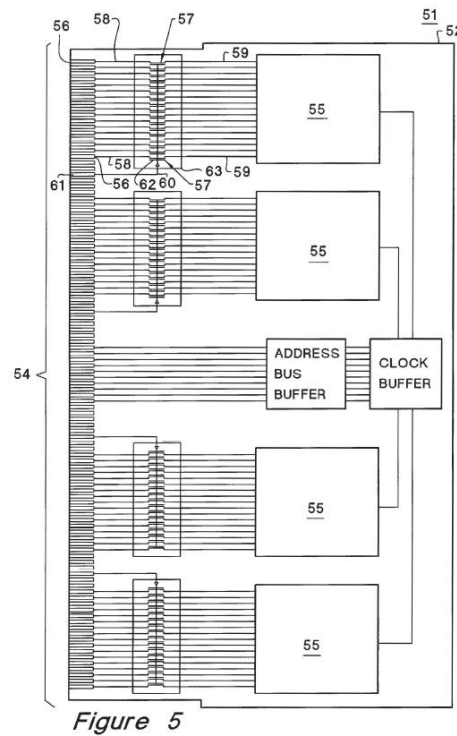


Figure 5 is a detailed plan view of memory module 51, which corresponds to memory module 24 from Figure 3.

Wiggers discloses that Figure 5, above, illustrates “a memory module for reducing the capacitive load in the data bus of a memory system according to the invention and of a type shown in box 50 of Fig. 3.” *Id.* at 6:33–36. Memory module 51 includes substrate 52, at least one memory chip 55 and switches 57 affixed to substrate 52. *Id.* at 6:35–40. Primary data lines 58 connect each data pin to an associated switch and secondary data lines 59 connect each switch to a memory device. *Id.* at 6:41–43. The switches include position controllers 62 for switching the switches between an open and closed position. Ex. 1010, 6:43–45. The position controllers are electrically connected to control line 60 that also electrically connected to control pin 61. *Id.* at 6:46–49.

Another embodiment of the system disclosed in Wiggers is shown in Figure 4, reproduced below.

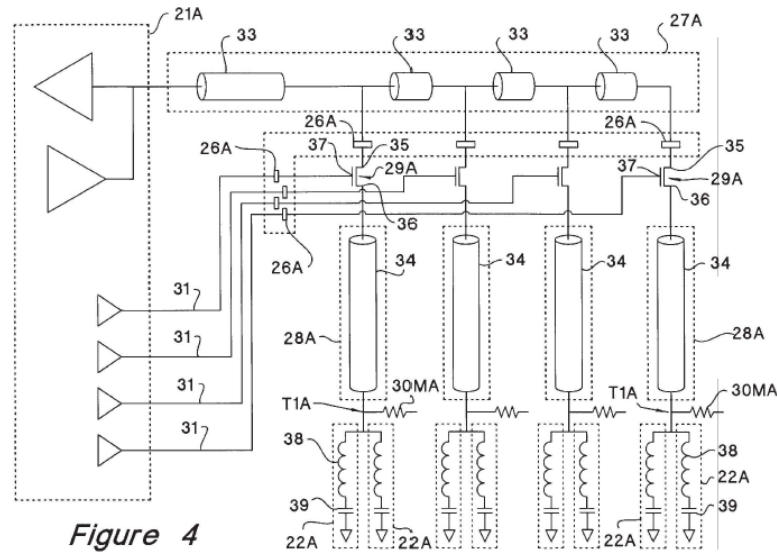


Figure 4

Figure 4 is a schematic of a memory system with the data bus 23 depicted as transmission lines 33.

As shown in Figure 4, data bus 23 (from Figure 3) is illustrated as a series of transmission lines. *Id.* at 5:20–21. Specifically, Wiggers teaches that board portion 27A includes transmission lines 33. *Id.* at 5:21–23. Wiggers also teaches that the memory controller uses switches to selectively (i) couple a memory device to a data bus when accessing a memory location in the memory device and (ii) decouple the memory device from the data bus at other times. *Id.* at 3:25–28. According to Wiggers, the selective coupling of the memory devices minimizes capacitive loading of the data bus. *Id.* at 3:28–31. Wiggers specifically discloses “there is at least one switch 29A for each data line connected to a memory module.” Ex. 1010, 5:40–41. Wiggers further discloses that “[w]hen multiple data lines are involved, the switches 29A can be grouped together into set (not shown in Fig. 4) with each switch in the set controlled by a common control signal on a single control line.” *Id.* at 5:47–51.

3. *Analysis*

a. *Amidi and Wiggers Teach or Suggest All the Recited Limitations of Independent Claims 15, 22, and 31*

Petitioner contends the combined disclosures of Amidi and Wiggers, as summarized above, teach or suggest each limitation of independent claims 15, 22, and 31 of the '150 patent. Pet. 44–57. As discussed below, Petitioner presents arguments identifying each claim element in the disclosures of Amidi and Wiggers. Petitioner first argues that Amidi discloses a circuit mounted on a memory module, where the circuit includes a logic element, a register, and a phase-lock loop device. *Id.* at 44 (referencing Ex. 1008 ¶¶ 2, 37; Figs. 4A, 6A); Ex. 1007 ¶ 93. According to Petitioner, the system described in Amidi includes a memory module having one or more ranks of double-data-rate (DDR) memory devices, which are electrically coupled to the components of the circuit (CPLD). *Id.* at 44–45 (citing Ex. 1008, Figs. 4A.) Petitioner then explains that Wiggers discloses a circuit electrically coupled to memory devices. *Id.* (citing Ex. 1010, 4:53–57).

Petitioner argues that Amidi discloses the following claim limitations: (i) memory devices having data signal lines and data strobe lines (Ex. 1008 ¶¶ 29, 32; Figs. 2, 3); (ii) stacks of DDR memory devices having a data signal line and a data strobe line DQS (*id.* ¶ 32; Fig. 3); and (iii) at least two DDR memory devices connected to the same (common) memory bus (“common data signal line”) (*id.* 34–35; Fig. 3). Pet. 27. According to Petitioner, a person of ordinary skill in the art would have recognized that each DDR memory device has its own data bus and that they are connected to a common data signal line, and that the circuit of Amidi is “electrically

coupled” to the common data bus. *Id.* at 27 (citing Ex. 1009 ¶¶ 61, 63, 65, 72. Petitioner further argues that Wiggers discloses that switches 29A are electrically coupled to a memory device by module portion 28A. *Id.* at 45 (citing Ex. 1010, 6:23–27; Fig. 4); Ex. 1007 ¶ 94. According to Petitioner, given the combined teachings of Amidi and Wiggers, a person of ordinary skill in the art would have found it obvious to organize the memory devices 22 of Wiggers into multiple ranks. Pet. 46 (citing Ex. 1007 ¶ 96).

Petitioner then concludes that it would have been obvious to a person of ordinary skill in the art to form a switch that is electrically coupled to a plurality of memory devices arranged in ranks on the memory module, as required by independent claim 22. *Id.*

Petitioner provides arguments for the sending and receiving of input signals by the systems in Amidi and Wiggers, and how each reference teaches a circuit that is responsive to such input signals. *Id.* at 47–52. Petitioner specifically argues that Amidi teaches a circuit that is “responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line,” because Amidi teaches that CPLD 404, 604 is responsive to a set of input signals (address signal Add(b) and chip select signals cs0, cs1) to determine (“selectively electrically coupling”) an active rank of the four ranks and inactivating the other three ranks of memory devices from the computer system. Pet. 49 (citing Section V.A.1 of the Petition). According to Petitioner, the act in Amidi of activating one rank while inactivating other ranks constitutes “selectively coupling” and “selectively isolating.” *Id.* Petitioner also argues that Wiggers teaches selectively electrically coupling



and decoupling individual memory devices (“first data signal line” and “second data signal line”) from the data bus (“common data signal line”). *Id.* Petitioner explains that the memory controller can also selectively electrically couple and decouple each of the memory devices from the data bus, either individually or in small groups using a number of switches 29, preferably including field effect transistor (FET) type switches. *Id.* (citing Ex. 1010, 4:53–57). Petitioner further notes that Wiggers discloses that switch 29A (“the circuit”) responds to a control line 31 (“the set of input signals”) from the memory controller 21A to electrically couple or decouple a memory module from the data bus. *Id.* at 49–50 (citing Ex. 1010, 5:40–47).

According to Petitioner, a person of ordinary skill in the art would have been motivated to combine the teachings of Amidi and Wiggers because (1) both references relate to memory devices, (2) both references describe coupling or isolating memory device loads, and (3) the combined teachings would result in the benefit of isolating a memory device load from a computer system so as to reduce parasitic capacitance and increase the speed of data propagation. Pet. 56–57 (citing Ex. 1008 ¶¶ 38, 39, 43, 44, 62; Ex. 1010, 4:27–37; 5:62–66); Ex. 1007 ¶¶ 96.

Petitioner supports its position with the Declaration of Dr. Jagannathan, who testifies that a person of ordinary skill in the art would have had a reason to apply the switches of Wiggers to the memory module of Amidi in order to increase the speed of data propagation. Ex. 1007 ¶ 96 (citing Ex. 1010, 3:39–40; 4:27–37). Dr. Jagannathan further opines that implementing the switches of Wiggers into the architecture of Amidi would

have been routine for one of ordinary skill in the art and the result of such application would have been as expected and taught by Wiggers. *Id.*

Patent Owner proffers several arguments contending that the combination of Amidi and Wiggers fails to teach or suggest a “circuit configured to be mounted on a memory module[] . . . the circuit . . . selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal to the common data signal line,” as recited in the challenged claims. PO Resp. 33–35.

Patent Owner first contends that although Wiggers discloses individual switch 29 on a single memory module 24 (as shown in Wiggers Fig. 3), Petitioner identifies only a collective group of switches 29A as its “circuit,” which spans across four (not one) of Wiggers’ memory modules. *Id.* at 33–34. According to Patent Owner, the collective group of switches 29A is designed to function across multiple memory modules and cannot be mounted on only a single memory module. *Id.* at 34. Patent Owner, thus, concludes that the “circuit” in Wiggers fails to meet the claim limitation “circuit configured to be mounted on a memory module,” because the collective group of switches 29A cannot be “configured to be mounted on” a single memory module of Wiggers (memory module 24) or Amidi (e.g., Figures 4A, 4B), even in the Amidi–Wiggers combination. *Id.*

We do not agree with Patent Owner. Rather, we are persuaded by Petitioner’s position and we find that Wiggers’ collective group of switches is controlled by a single memory controller. Ex. 1010, 5:40–51. As can be seen in Figure 5 of Wiggers, there is a single substrate 52 affixed with multiple switches 57 that connect via lines 59 to multiple memory devices

55. *Id.* at Fig. 5; 6:36–49. The memory module 51 of Figure 5 is a plan view of memory module 24 shown in box 50 of Figure 3. *Id.* at 6:33–36. As shown in Figure 3, the electrical connections include interconnects between the main board portion 27 of the data bus and the module portion 28 on the data bus. *Id.* at 5:1–4; Fig. 3. Therefore, we are satisfied that Wiggers teaches a “circuit configured to be mounted on a memory module[] . . . the circuit . . . selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal to the common data signal line,” as recited in the challenged claims.

Patent Owner further contends we erred in construing “circuit configured to be mounted on a memory module,” in an unreasonably broad manner. PO Resp. 34. According to Patent Owner, a person of ordinary skill in the art would understand the claim language of “circuit configured to be mounted on a memory module” as Patent Owner proposed: “an entire circuit configured to be mounted on a single memory module.” *Id.*; *see supra*, Section II.A.3. Based on Patent Owner’s proffered claim construction, Patent Owner argues that the entirety of the Petition’s “circuit” is the collective group (of Wiggers’ switches 29A) itself, which structurally spans multiple memory modules, and thus cannot, and is designed to not, be mounted on only a single memory module. PO Resp. 34–35.

As discussed above, we are not persuaded by Patent Owner’s contentions regarding claims construction. To the contrary, we construe “circuit configured to be mounted on a memory module” to encompass “circuitry configured to be mounted on at least a portion of a memory module.” *See supra*, Section II.A.3. Wiggers’ disclosure of switches (i.e.,

circuitry) mounted on memory modules controlled by a single memory controller falls within the scope of the term “circuit configured to be mounted on a memory module” as we have construed the term.

Patent Owner also contends that Amidi and Wiggers are improperly combined by Petitioner. PO Resp. 47. Patent Owner explains that the Petitioner’s combination is based on impermissible hindsight and would result in an inoperable system, and that the testimony of Dr. Jagannathan is insufficient to overcome the impediments to combining Amidi and Wiggers. *Id.* at 47–50. According to Patent Owner, Amidi’s CPLD output CS signal and control signals for Wiggers’ switches are not equivalent, based on specific differences in respective timing operation and purpose, and a person of ordinary skill in the art would have understood that the specific implementation details, e.g., timing considerations, are critical in evaluating the operability of using Amidi’s CPLD output CS signal and control signals for Wiggers’ switches equivalently. *Id.* at 48 (citing Ex. 2002 ¶ 113). Patent Owner argues that the timing problems that would arise from an Amidi-Wiggers combination would render such a combination inoperable. *Id.* at 48–49.

Patent Owner relies on the Declaration of Dr. Sechen to support its position regarding the inoperability of an Amidi-Wiggers combination. *See* Ex. 2002 ¶¶ 112–118. Dr. Sechen specifically states that:

due to standardized DDR memory device operation, a DDR read (or write) command’s chip-select signal (*e.g.*, Amidi’s CPLD output chip-select signal) does not coincide with its read (or write) data (*e.g.*, to be gated by Wiggers’ switch control signal). Thus, by failing to properly transfer the target data, the Petitioner’s proposal—DDR chip-select signals from Amidi’s

CPLD = Wiggers' switch control signals—would malfunction and be inoperable.

*Id.* ¶ 113.

Patent Owner then argues that an Amidi-Wiggers combination is also inoperable because a DDR chip-select signal (as used in Amidi) is not designed to be a timing signal, whereas a timing signal is required for Wiggers switch 20A to operate properly. PO Resp. 49. Patent Owner supports its position with the Declaration of Dr. Sechen, who testifies that “[f]undamentally, a DDR chip-select signal in itself lacks timing information to indicate when to properly open and close a switch 29A of Wiggers. Thus, a DDR chip-select signal, as output by Amidi’s CPLD, would not be a usable signal at all for controlling Wiggers’ switch 29A.” Ex. 2002 ¶ 114.

Again, we do not agree with Patent Owner. Rather, we agree with Petitioner’s position and we find that Wiggers teaches timing operations for its switches that would have been applicable to Amidi. Additionally, we are persuaded that the timing requirements for memory devices are dictated by the JEDEC standards, which were known to a person of ordinary skill in the art at the time of the ’150 patent. *See e.g.*, Ex. 1008 ¶ 7. We credit the testimony of Dr. Jagannathan, which states that Figure 6 of Wiggers “teaches how to time the coupling and decoupling of a select memory device to the data bus when writing to or reading therefrom.” Ex. 1023 ¶ 51 (citing Ex. 1010, Fig. 6). We also credit the testimony of Dr. Jagannathan regarding the JEDEC21C-4.5.7 standard as it relates to the 168 Pin Registered SDRAM DIMM Family of memory devices. *See e.g.*, Ex. 1007 ¶¶ 43–51. Dr. Jagannathan specifically testifies that

There is a Phase-Locked Loop (PLL) clock input provided to the register and to the memory devices. This is depicted in

JEDEC21C-4.5.7, Figure as “PCK” input to the register, and as “CK0 \_ PLL” in the case of the memory devices. A phase-locked loop device receives an input clock signal and generates another clock signal whose phase matches (within tolerance) the input clock. The details of the PLL are specified in JEDEC21C-4.5.7 at p. 4.5.7-8. Specifically, the PLL clock output is depicted as driving a number of SDRAM devices and registers.

*Id.* ¶ 45.

The concept of a PLL would generally be well understood by one of ordinary skill in the art. For instance, Jacob teaches that “[t]he function of a PLL or DLL, in general, is to synchronize two periodic signals so that a certain fixed amount of phase-shift or apparent delay exists between them. The two are similar, and the terms are often used interchangeably.”

*Id.* ¶ 46 (citing Ex. 1018, 11).

Thus, we find that a person of ordinary skill in the art would have known how to address the timing and use of chip-select signals so that the teachings of Wiggers would have been applicable to Amidi.

The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference (*Keller*, 642 F.2d at 425). Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art. *Id.* We credit the testimony of Dr. Jagannathan, who states that (i) “when Wiggers refers to a ‘signal’ used in any of the circuits taught therein, one of ordinary skill would understand it is ‘a varying electrical impulse that conveys information from one point to another’” (Ex. 1007 ¶ 93) and (ii) “[o]ne of ordinary skill in the art would have been motivated to apply the switch taught by Wiggers to the memory module of Amidi,

because the switch of Wiggers increases the speed of data propagation.” Ex. 1007 ¶ 96 (citing Wiggers, 3:39–40, 4:27–37). Thus, we are not persuaded that the control signals from Amidi’s CPLD could not be used as control signals for Wiggers’ switch, or that the teachings of Amidi and Wiggers are not combinable.

Based on the evidence of record, we agree with Petitioner’s position that challenged claims 15–17, 22, 24, 26, and 31–33 would have been obvious over Amidi and Wiggers. First, we are persuaded by Petitioner’s reasoning and the evidentiary record that Amidi teaches a circuit mounted on a memory module that is electrically coupled to a first DDR memory device and a second DDR memory device. We are further persuaded that Amidi teaches a circuit with a logic element, a register, and a PLL. We also are persuaded that the teachings of Amidi could have been implemented using the common data signal line and switch system disclosed in Wiggers so that by (i) selectively electrically coupling a first data signal line to the common data signal line and (ii) selectively electrically coupling a second data signal line to the common data signal line the circuit is responsive to a set of input signals. Additionally, we credit the testimony of Dr. Jagannathan that a person of ordinary skill in the art would have had reason to combine the teachings of Amidi with Wiggers, because both references relate to memory devices, both references discuss the problem of reducing the load seen by the memory controller, and both references describe coupling or isolating memory device loads. *See* Ex. 1007 ¶ 96.

Second, the arguments presented by Patent Owner generally attack the references individually, rather than in combination. PO Resp. 33–35, 47–58. Nonobviousness cannot be established by attacking the references

individually when a challenge is predicated upon a combination of prior art disclosures. *See Merck*, 800 F.2d at 1097; *cf. Keller*, 642 F.2d at 426 (“[O]ne cannot show non-obviousness by attacking references individually where . . . the rejections are based on combinations of references.”). In attacking the references individually, Patent Owner fails to address Petitioner’s actual challenges and establish an insufficiency in the combined teachings of the references. Patent Owner has not convinced us that Petitioner failed to meet its burden to establish a reasonable likelihood it would prevail in showing obviousness of the challenged claims.

Lastly, we note that the testimony of Patent Owner’s Declarant, Dr. Sechen, is based on the claim constructions proffered by Patent Owner and not on the constructions set forth in the Decision to Institute. *Compare Ex. 2002 ¶¶ 38–72, with Dec. to Inst. 7–12*. Although we have reviewed Dr. Sechen’s testimony in detail, for the reason stated above, we considered as relevant the portions of his analysis regarding the prior art and alleged non-obviousness of the claims and accorded the appropriate weight to that particular testimony.

Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that claims 15, 22, and 31 of the ’150 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Amidi and Wiggers.

*b. Amidi and Wiggers Teach or Suggest All the Recited Limitations of Dependent Claims 16, 17, 24, 26, 32, and 33*

Claims 16, 24, and 32 recite “wherein the two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.” Ex. 1001, 43:3–5, 44:1–3, 44:58–60. Dependent claim 17



recites that the circuit includes “one or more switches selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the one or more switches operatively coupled to the logic element to receive control signals from the logic element.” Dependent claim 33 recites a similar limitation. *Id.* at 43:6–12. Dependent claim 26 further recites that the claimed circuit is “configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system.” *Id.* at 44:8–11.

Petitioner contends the combined disclosures of Amidi and Wiggers, as summarized above, teach or suggest each limitation of dependent claims 16, 17, 24, 26, 32, and 33 of the ’150 patent. Pet. 53–57. Patent Owner does not provide separate contentions regarding additional limitations recited in the dependent claims. *See generally* PO Resp.

After careful consideration of the language recited in claims 16, 17, 24, 26, 32, and 33 of the ’150 patent, the Petition, the Patent Owner Response, and Petitioner’s Reply, as well as the relevant evidence discussed in those papers, we find that one of ordinary skill in the art would have considered these dependent claims obvious over the combination of Amidi and Wiggers. Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that claims 16, 17, 24, 26, 32, and 33 of the ’150 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Amidi and Wiggers.

### III. CONCLUSION

We conclude Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of the '150 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combinations of (1) Amidi and Klein and (2) Amidi and Wiggers.

### IV. ORDER

For the reasons given, it is

ORDERED that, by a preponderance of the evidence, claims 15–17, 22, 24, 26, and 31–33 of the '150 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2014-00882  
Patent 7,881,150 B2

FOR PETITIONER:

Fabio Marino  
fmarino@mwe.com

Bernie Knight  
bknight@mwe.com

Barrington Dyer  
bdyer@mwe.com

MCDERMOTT WILL & EMERY

FOR PATENT OWNER:

Mehran Arjomand  
marjomand@mofocom  
patentdocket@mofocom

David Kim  
dkim@mofocom  
patentdocket@mofocom

Erol Basol  
ebasol@mofocom  
patentdocket@mofocom

Jean Nguyen  
jnguyen@mofocom  
patentdocket@mofocom

Jonathan Statman  
jstatman@mofocom  
patentdocket@mofocom

MORRISON & FOERSTER LLP