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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX, INC.,
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00390
Patent 8,629,542 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and FRANCES L. IPPOLITO, *Administrative Patent Judges*.

IPPOLITO, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively "Petitioner") filed a Petition on December 28, 2015, requesting an *inter partes* review of claims 1–3, 30, 31, 33, 40, 41, and 44 of U.S. Patent No. 8,629,542 B2 (Ex. 1001, "the '542 patent"). (Paper 4, "Pet."). Patent Owner, Elm 3DS Innovations, LLC, filed a Preliminary Response to the Petition on April 6, 2016 (Paper 10, "Prelim. Resp.").

Based on these submissions, we instituted an *inter partes* review of claims 1–3, 30, 31, 33, 40, 41, and 44 of the '542 patent on the following grounds:

Reference(s)	Basis	Claims Challenged
Bertin '754[1], Poole[2], and Leedy '695[3]	§ 103	1–3, 30, 31, 33, 40, 41, and 44
Hsu[4] and Leedy '695	§ 103	1–3, 30, 31, 33, 40, 41, and 44
Bertin '754 and Poole	§ 103	1 and 44
Hsu	§ 103	1 and 44

Paper 13 ("Dec. on Inst.").

After institution, Patent Owner filed its Patent Owner Response on October 14, 2016 (Paper 53, "PO Resp.") and Petitioner filed a Reply (Paper 59, "Reply,"). A consolidated oral hearing was held on April 6, 2017, and a transcript of the oral hearing is of record. Paper 63 ("Tr.").

[1] US Patent No. 5,202,754, issued April 13, 1993 (Ex. 1004, "Bertin '754").
[2] US Patent No. 5,162,251, issued Nov. 10, 1992 (Ex. 1005, "Poole").
[3] US Patent No. 5,354,695, issued Oct. 11, 1994 (Ex. 1006, "Leedy '695").
[4] US Patent No. 5,627,106, issued May 6, 1997 (Ex. 1008, "Hsu").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a final written decision under 35 U.S.C. § 318(a) as to the patentability of the challenged claims. For the reasons that follow, we determine Petitioner has not shown by a preponderance of the evidence that claims 1–3, 30, 31, 33, 40, 41, and 44 of the '542 patent are unpatentable.

A. Related Proceedings

Petitioner indicates that the '542 patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK Hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

Additionally, patents related to the '542 patent are also the subjects of petitions filed in IPR2016-00386 (US Patent No. 8,653,672); IPR2016-00387 (US Patent No. 8,841,778); IPR2016-00388 and IPR2016-00393 (US Patent No. 7,193,239); IPR2016-00389 (US Patent No. 8,035,542); IPR2016-00391 (US Patent No. 8,796,862); IPR2016-00394 (US Patent No. 8,410,617); IPR2016-00395 (US Patent No. 7,504,732); IPR2016-00687 (US Patent No. 8,928,119); IPR2016-00691 (US Patent No. 7,474,004); IPR 2016-00708 (US Patent No. 8,907,499); IPR 2016-00770 (US Patent No. 8,907,499); and IPR 2016-00786 (US Patent No. 8,933,570).

We also note that Petitioner filed two additional petitions requesting *inter partes* review of U.S. Patent No. 8,791,581 (IPR2016-00703 and IPR2016-00706) for which we did not institute a review.

B. Time Bar under 35 U.S.C. § 315(b)

In our Decision to Institute, we did not agree with Patent Owner that the Petition was barred under 35 U.S.C. § 315(b) because, according to

Patent Owner, the Office lacked authority to treat certain days, on which the Office experienced an emergency situation such that many of its online and information technology systems were shut down, as federal holidays. Dec. on Inst. 3–4. Patent Owner has not raised this issue subsequent to institution in this proceeding.

C. The '542 Patent

The '542 patent is directed generally to a "[t]hree-[d]imensional [s]tructure (3DS)" for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1*a* is reproduced below.

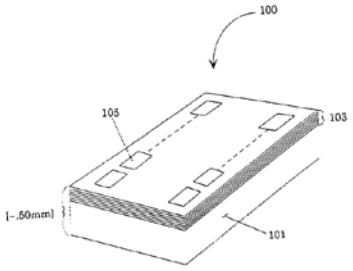


Figure 1a

Figure 1*a* shows 3DS memory device 100 having a stack of integrated circuit layers with a "fine-grain inter-layer vertical interconnect" between all circuit layers. *Id.* at 4:10–13. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:30–32. The '542 patent discloses that "each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 µm and typically less than 10 µm in thickness." *Id.* at 4:35–37. The '542 patent further discloses that the "thinned (substantially flexible) substrate circuit layers are preferably made

with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication." *Id.* at 8:58–63.

Figure 1*b* is reproduced below.

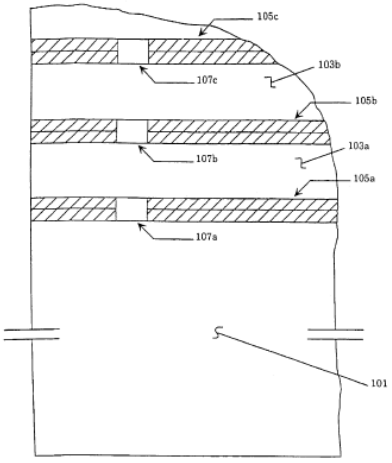


Figure 1b

Referring to Figure 1*b*, the '542 patent shows a cross-section of a 3DS DRAM integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:51–53. Bond and interconnect layers 105a, 105b, etc. are shown between circuit layers 103a and 103b. *Id.* at Fig. 1*b*. The '542 patent discloses that pattern 107a, 107b, etc. in the bond and interconnect layers 105a, 105b, etc. define the vertical interconnect contacts between the integrated circuit layers and serve to electrically isolate these contacts from each other and the remaining bond material. *Id.* at 4:24–28. Additionally, the '542 patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:29–29.

Further, the '542 patent teaches that the "term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through

a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 μm." *Id.* at 4:14–17. The fine-grained inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:18–20.

D. Illustrative Claim

Of the challenged claims, claim 1 (reproduced below) is independent and illustrative of the subject matter of the '542 patent:

> 1. A stacked integrated circuit comprising:
>
> a circuit substrate;
>
> a first integrated circuit having circuitry formed on a front surface thereof, the front surface or a back surface being bonded to the circuit substrate; and
>
> one or more additional integrated circuits each having circuitry formed on respective front surfaces thereof, each additional integrated circuit having the front surface or a back surface thereof adjacent to the front surface or a back surface of an adjacent integrated circuit;
>
> wherein at least one of the first integrated circuit and the one or more additional integrated circuits is substantially flexible and comprises a substantially flexible semiconductor substrate of one piece made from a semiconductor wafer thinned by at least one of abrasion, etching and parting, and subsequently polished to form a polished surface.

II. ANALYSIS

A. Claim Construction

Following institution, the parties submitted briefing regarding the claim construction standard applicable in this proceeding. Papers 21, 24, 26. Patent Owner further certified that the '542 would expire before the deadline for issuing a final written decision in this proceeding, and both parties requested the application of a district court-type construction under *Phillips v. AWH Corp*., 415 F.3d 1303, 1312, 1327 (Fed. Cir. 2005). Paper 21; Paper 26, 4–5. Patent Owner indicated that the '542 patent would expire by April 4, 2017, which has passed. Paper 21.

In our Decision regarding claim construction, we determined that a district court-type construction standard applies to the claims at issue in the expired '542 patent. Paper 26, 7. We construe expired patent claims according to the standard applied by the district courts. *See In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). Specifically, we apply the principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Extrinsic evidence, such as expert testimony and dictionary definitions, can be helpful but is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc. v. U.S. Surgical Corp*., 388 F.3d 858, 862 (Fed. Cir. 2004) (internal quotation marks omitted)). Also, extrinsic

evidence is to be considered within the context of the intrinsic evidence. *Id.* A claim term may be construed contrary to its ordinary and customary meaning only "under two circumstances: '(1) when a patentee sets out a definition and acts as [its] own lexicographer, or (2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.'" *Aventis Pharma S.A. v. Hospira, Inc.*, 675 F.3d 1324, 1330 (Fed. Cir. 2012) (quoting *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)); *Hill-Rom Svcs, Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014). Further, only those terms which are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

We construe the challenged claims according to these principles.

1. "substantially flexible semiconductor substrate" [5] *(claim 1)*

Based on the preliminary record, we construed the term "substantially flexible semiconductor substrate" to mean "a semiconductor substrate that has been thinned to a thickness of less than 50 μm." Dec. on Inst. 11. In our Decision on Institution, we also stated that the claim construction "may change as a result of the record developing during trial." *Id.* "We note[d], for example, that Patent Owner has not yet filed its response under 37 C.F.R.

[5] The term "substantially flexible" is at issue in thirteen of the Elm 3DS *inter partes* reviews: IPR2016-00386 ('672 patent), IPR2016-00387 ('778 patent), IPR2016-00388 ('239 patent), IPR2016-00390 ('542 patent), IPR2016-00391 ('862 patent), IPR2016-00393 ('239 patent), IPR2016-00394 ('617 patent), IPR2016-00395 ('732 patent), IPR2016-00687 ('119 patent), IPR2016-00691 ('004 patent), IPR2016-00708 ('499 patent), IPR2016-00770 ('499 patent), and IPR2016-00786 ('570 patent).

§ 42.120 or any new testimonial evidence." *Id.* At this juncture, based on the complete record, we modify our construction of "substantially flexible semiconductor substrate" as discussed below.

In reviewing the complete record for the instant proceeding, we note that the parties' proposed constructions, arguments, and supporting evidence, mirror those submitted in IPR2016-00386, IPR2016-00387, and IPR2016-00388. IPR2016-00386, -00387, and -00388 all involve related patents that share the same specification as the '542 patent, and, further, involve the construction of the same term "substantially flexible semiconductor substrate." *See* IPR2016-00386, Paper 68.

In those proceedings, as with this one, Petitioner construes the term "substantially flexible semiconductor substrate" as "a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed."[6] Pet. 10; *See* IPR2016-00386, Paper 68. Further, in response, Patent Owner proposes that "substantially flexible" should be construed to mean "largely able to bend without breaking." PO Resp. 51 (citing Ex. 2165).

Additionally, we observe that at the consolidated Oral Hearing, the parties presented arguments directed to the construction of "substantially flexible," generally, without any indication of there being any difference in construction for any one of the consolidated cases (e.g., IPR2016-00386,

[6] In its Petition, Petitioner asserted the construction of the term is the same under both the broadest reasonable construction standard and under *Phillips.* Tr. 13:8–11 (Petitioner's counsel indicating that for substantially flexible the "construction would be the same under [broadest reasonable interpretation] and *Phillips*."); *see* Tr. 11:21–13:16.

-00387, -00388, and -00390). *See* Tr. 63, 5:7–19:15, 24:1–52:20, 56:20–66:9.

Our construction of "substantially flexible semiconductor substrate" and the basis for this construction are discussed in extensive detail in the Final Written Decisions issued in IPR2016-00386, IPR2016-00387, and IPR2016-00388. In those Final Written Decisions, having considered the intrinsic evidence (including the claim language, written description, and prosecution history of related patent applications) and extrinsic evidence, we determine that one of ordinary skill in the art in the context of the challenged patent would understand a "substantially flexible semiconductor substrate" to mean "a substantially flexible semiconductor substrate" within the context of the subject matter of the patent is "a semiconductor substrate that is largely able to bend without breaking." *See* IPR2016-00386, Paper 68, Sect. II.B. Given the shared specification of the patents and identical constructions and arguments presented by the parties, our analysis in IPR2016-00386, -00387, and -00388 applies with equal force here. Indeed, the relied upon evidence of record in those cases are also of record in this case. *See* IPR2016-00386, Paper 68 (citing Paper 55, 51; Paper 1, 9); Pet. 10; PO Resp. 51. Thus, for IPR2016-00390, we adopt and incorporate our discussion and construction of "substantially flexible" provided in the Final Written Decision for IPR2016-00386, IPR2016-00387, and IPR2016-00388. IPR2016-00386, Paper 68; IPR2016-00387, Paper 63; IPR2016-00388, Paper 60.

Additionally, we note that the specific claim language at issue in this proceeding, though not identical, is very similar to that at issue in IPR2016-00386, -00387, and -00388. For example, independent claim 1

recites, in relevant part, "[a] stacked integrated circuit comprising . . . at least one of the first integrated circuit and the one or more additional integrated circuits is substantially flexible and comprises a substantially flexible semiconductor substrate of one piece made from a semiconductor wafer thinned by at least one of abrasion, etching and parting, and subsequently polished to form a polished surface." Similar to IPR2016-00386, the language in claim 1 does not contextually define "substantially flexible," and adopting Petitioner's construction would read out "thinned by at least one of abrasion, etching and parting, and subsequently polished to form a polished surface."

Accordingly, having considered the full and complete record in this proceeding, we construe "substantially flexible semiconductor substrate" to mean "a semiconductor substrate that is largely able to bend without breaking." *See* IPR2016-00386, Paper 68, Sect. II.B.

2. Substantially flexible integrated circuit/circuit substrate (claim 1, 40)

In the challenged claims, the term "substantially flexible" also modifies "integrated circuit," and "circuit substrate." Ex. 1001, claims 1, 40. Nonetheless, we find that our construction of "substantially flexible" does not change in this context.

In the Petition, Petitioner proposes that a "substantially flexible integrated circuit" or "circuit substrate" is "an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed, and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm^2 tensile or less." Pet. 14–

17. For its proposed construction, Petitioner relies on many of the same arguments discussed above and in detail in the Final Written Decision for IPR2016-00386, -00387, and -00388, for this proposed construction. *See* Pet. 14–17. For these similar arguments, we rely on and adopt the discussion in the Final Written Decision of IPR2016-00386, -00387, and -00388.

Additionally, Petitioner asserts that the Patent Owner (then, Applicant) defined "substantially flexible integrated circuit/circuit substrate" during examination of related patent applications. Pet. 14–17. Specifically, Petitioner cites to responses provided by Patent Owner during examination of U.S. Patent Application No. 12/497,652 ("the '652 application").[7] *Id.* Petitioner argues exclusively from the examination of the '652 application—not the prosecution history of the '542 patent at issue here.[8] Even so, "[t]he prosecution history of a related patent can be relevant if, for example, it addresses a limitation in common with the patent" at issue. *Advanced Cardiovascular Sys., Inc. v. Medtronic, Inc.*, 265 F.3d 1294, 1305 (Fed. Cir. 2001).

In this regard, Petitioner contends that during examination of the '652 application, the Applicant defined "substantially flexible" integrated circuit and circuit substrate to require a sufficiently thin semiconductor material (e.g., 50 microns or less) and a low stress dielectric material of 5 x 10^8 dynes/cm^2 or less. Pet. 15 (citing Ex. 1023, 28). Petitioner further asserts

[7] Petition refers to the prosecution history of U.S. Patent Application No. 12/497,653. However, Exhibits 1021 and 1023 are both responses from the examination of the '652 application.
[8] The '652 application was ultimately expressly abandoned by the Applicant, and did not issue.

that the Applicant confirmed this definition in a later September 26, 2013 response. *Id.* at 15–16 (citing Ex. 1021, 2–3).

Looking to the prosecution of the '652 application, we are not persuaded that these statements from the Applicant amount to a clear and unmistakable definition or disavowal of claim scope. In the April 5, 2013 response, Applicant stated that

> both Bertin and Kato fail to teach or suggest that at least one of the first and second *circuit layers* is substantially flexible, and the substrate thereof is a substantially flexible semiconductor substrate. Two features are required to achieve substantial flexibility. One is that the semiconductor material must be sufficiently thin, e.g., 50 microns or less. Bertin and Kato are believed to satisfy this requirement. The other is that the dielectric material used in processing the semiconductor material must be sufficiently low stress. Otherwise, substantial flexibility is defeated. As set forth in the present specification, stress of 5×10^8 dynes/cm^2 or less has been demonstrated to satisfy this requirement.

Ex. 1023, 28 (emphasis added). In a subsequent response on September 26, 2013, Applicant stated

> The *circuit layer* may be fabricated in a manner that undoes or defeats flexibility of the semiconductor substrate. More particularly, a circuit layer requires one or more dielectric layers. Dielectric material has an associated level of stress. For a circuit layer to be substantially flexible, Applicant has found that the dielectric material must have low tensile stress, for example, 5×10^8 dynes/cm^2 tensile.

Ex. 1021, 2–3 (emphasis added).

Initially, we note that Applicant's statements are directed to a "circuit layer," which is not the language at issue in this proceeding (i.e., "integrated circuit" and "circuit substrate"). For this reason, we are not persuaded that Applicant's statements regarding "circuit layer" is controlling, or even

informative, on whether Applicant defined or disavowed claim scope for different limitations "substantially flexible" integrated circuit and circuit substrate.

Further, even considering Petitioner's arguments and Applicant's statements, we determine that these statements do not define or disavow claim scope for these specific limitations at issue. Having reviewed these responses and the prosecution history of the '652 application, we understand Applicant to have taken the position that the thinness of the *semiconductor material* and the stress level of dielectric material used in processing the *semiconductor material* are factors for substantial flexibility. The Applicant did not, however, define a "substantially flexible" integrated circuit/circuit substrate in terms of the thinness of a semiconductor substrate, as Petitioner proposes. Rather, the Applicant's statements refer to a *semiconductor material*, not a semiconductor substrate, and do not discuss polishing or smoothing. This is further confirmed in the September 2013 response in which the Applicant states that the flexibility of the semiconductor substrate does not control the flexibility of the circuit layer because the "circuit layer may be fabricated in a manner that undoes or defeats flexibility of the semiconductor substrate." Ex. 1021, 2–3.

Additionally, we are not persuaded that the Applicant defined "substantially flexible" integrated circuit/circuit substrate to include a stress range. Instead, Applicant states "[a]s set forth in the present specification, stress of 5×10^8 dynes/cm^2 or less has been demonstrated to satisfy this requirement." Ex. 1023, 28. We view this statement as providing an example of low stress dielectrics that may allow for "substantially flexibility." Our reading of Applicant's statements is consistent with the

Specification, which teaches that "[t]he thinned substantially flexible) substrate circuit layers are *preferably* made with dielectrics in low stress (less than 5×10^8 dynes/cm^2)," (Ex. 1001, 8:58–63) (emphasis added), and the 3DS memory stacks are "typically organized" with a "thinned and substantially flexible circuit with net low stress," (*id.* at 4:30, 35–36)(emphasis added). Thus, we are not persuaded that Applicant's statements constitute a clear and unmistakable definition or disavowal of claim scope sufficient for us to depart from the ordinary and customary meaning of "substantially flexible," which is "largely able to bend without breaking" as discussed above, and in further detail in the Final Written Decisions of IPR2016-00386, -00387, and -00389.

Additionally, we observe that Petitioner's proposed construction requires a substantially flexible integrated circuit to include a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed. As such, adopting this proposal would effectively read "at least one of the first integrated circuit and the one or more additional integrated circuits is substantially flexible and *comprises a substantially flexible semiconductor substrate of one piece made from a semiconductor wafer thinned by at least one of abrasion, etching and parting, and subsequently polished to form a polished surface*" out claim 1. *See Stumbo v. Eastman Outdoors, Inc.*, 508 F.3d 1358, 1362 (Fed. Cir. 2007) (rejecting claim constructions that render phrases in claims superfluous).

Accordingly, based on the complete record, we determine that "substantially flexible" integrated circuit means "an integrated circuit that is largely able to bend without breaking"; and a "substantially flexible" circuit

substrate" is a "circuit substrate that is largely able to bend without breaking."

3. "low stress dielectric" (claim 2)

In the Decision on Institution, we construed a "low stress dielectric" to mean "a dielectric having a stress of less than 8 x 10^8 dynes/cm^2." The parties have not challenged this construction. Further, based on the complete record before us, we discern no reason to deviate from our previous determination here. For example, we note that the disclosure in the Specification of the '542 patent is consistent with our construction, and teaches that dielectrics in low stress include those that have a stress of less than 5×10^8 dynes/cm^2 and "low stress dielectrics are discussed at length in U.S. Pat. No. 5,354,695." Ex. 1001, 8:60–9:2. Looking to the disclosure of Leedy '695, U.S. Patent No. 5,354,695, the reference teaches "[l]ow stress is defined relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being *less than 8 x 10^8 dynes/cm^2 (preferably 1 x 10^7 dynes/cm^2) in tension*." Ex. 1006, 11:33–37 (emphasis added).

B. Grounds Under 35 U.S.C. § 103

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). 35 U.S.C. § 103. The ultimate determination of obviousness under § 103 is a question of law based on underlying factual findings. *In re Baxter Int'l, Inc.*, 678 F.3d 1357,

1362 (Fed. Cir. 2012) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966)). These underlying factual considerations consist of: (1) the "level of ordinary skill in the pertinent art," (2) the "scope and content of the prior art," (3) the "differences between the prior art and the claims at issue," and (4) "secondary considerations" of non-obviousness such as "commercial success, long-felt but unsolved needs, failure of others, etc." *KSR*, 550 U.S. at 406 (quoting *Graham*, 383 U.S. at 17–18).

We analyze the asserted grounds based on obviousness with the principles identified above in mind.

2. Level of Skill in the Art

Petitioner's declarant, Dr. Paul D. Franzon, testifies that a person of ordinary skill in the art at the time of the invention would have had at least a bachelor's degree in electrical engineering, material science, or equivalent thereof, and at least 3–5 years of experience in the relevant field, e.g., semiconductor processing. Ex. 1002 ¶¶ 53–54; Pet. 5. Patent Owner does not dispute Petitioner's assessment. *See* Tr. 161:21–25, 112:5–14. We adopt Petitioner's proposed level of skill in the art, which is consistent with the '542 patent and the asserted prior art. For example, the '542 patent is directed to stacked integrated circuits and Leedy '695 is directed to methods for fabricating integrated circuits from membranes formed of low stress dielectric materials. Ex. 1001, 1:23–24; Ex. 1006, Abstract.

3. Claims 1–3, 30, 31, 33, 40, 41, and 44 – Obvious over Bertin '754 and Poole

i. Bertin '754 (Ex. 1006)

Bertin '754 relates generally to "[a] fabrication method and resultant three-dimensional multichip package having a densely stacked array of semiconductor chips." Ex. 1004 at Abstract. Figure 3a is reproduced below.

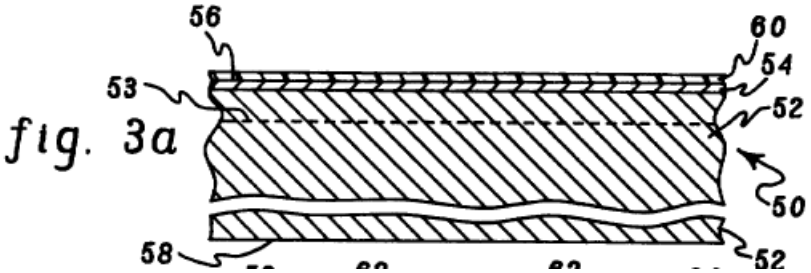


fig. 3a

Figure 3a depicts semiconductor device 50 having substrate 52 and active layer 54. Ex. 1004, 3:50–52. Layer 54 is adjacent to a first, upper planar surface 56 of device 50. *Id.* at 3:57–58. A second, lower planar surface 58 of device 50 is positioned substantially parallel to first planar surface 56. *Id.* at 3:59–60. Each stacked chip 50 includes a semiconductor "substrate 52" (*id.* at 3:50–4:3), which is thinned to 20 μm or less (*id.* at 3:25–46, 5:10–22). Bertin '754 further teaches that "dielectric layer 60, for example, SiO_2, is grown over active layer 54 of device 50." *Id.* at 3:60–62, Fig. 3a.

Figure 2b, reproduced below, illustrates another example of a multichip package fabricated pursuant to the method described in Bertin '754. Ex. 1004, 2:45–49.

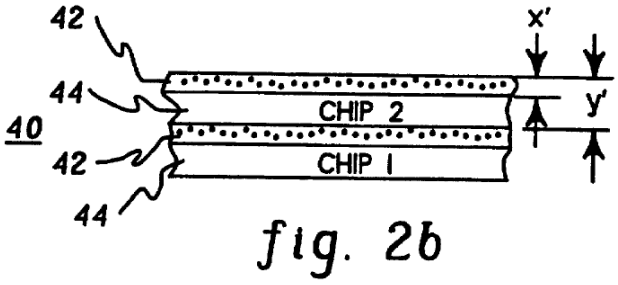


fig. 2b

Figure 2b shows two thin semiconductor chips, chip 1 and chip 2, stacked in package 40. *Id.* at 3:28–30. Active layer 42 of each chip in package 40 has a thickness "x" which, as shown, is a portion of the chip thickness "y." *Id.* at 3:30–33. Thickness "x" may be in the 5–20 micrometers range, while the overall thickness "y" of each device may be only 20 micrometers or less. *Id.* at 3:35–38.

Additionally, Bertin '754 teaches that the multichip package includes vertical electrical interconnections (e.g., metallized trenches 66) that pass completely through substrates 52. Ex. 1004, Abstract, 1:62–2:12, 4:11–52, Figs. 3c, 3b, 3e, 3g). Referring to Figure 3e, Bertin '754 provides that trenches 62 are filled with metal to create metallized trenches 66 that extend through etch stop layer 53. *Id.* at 4:43–48. Contact pads 68 interconnect the appropriate wiring on the chip to vertically disposed wiring 66 in trenches 62. *Id.* at 4:48–52.

ii. Summary of Poole (Ex. 1005)

Poole is directed to a method for making thinned charge-coupled devices, which are thinned to allow illumination of the backside of the device to improve quantum efficiency and UV spectral response. Ex. 1005, Abstract, 1:8–11. In one example, Poole teaches that a standard thick silicon charge-coupled device (Fig. 1A) has its pixel face mounted to a transparent, optically flat glass substrate using a thin layer of thermoset epoxy. *Id.* at

Abstract. The backside silicon of the charge-coupled device is thinned to 10 ±0.5 µm using a two-step chemi-mechanical process. *Id.* The bulk silicon is thinned to 75 µm with a 700 micro-grit aluminum oxide abrasive and is then thinned and polished to 10 µm using 80 nm grit colloidal silica. *Id.*

iii. Summary of Leedy '695 (Ex. 1006)

Leedy '695 relates to the fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and semiconductor materials. Ex. 1006, 1:38–41. In the Abstract, Leedy '695 indicates that the disclosed integrated circuits are fabricated from flexible membranes "formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers." *Id.* at Abstract. Leedy '695 also discloses forming a "tensile low stress dielectric membrane" on a semiconductor layer as part of its integrated circuit structure. *Id.* at 1:53–58. Leedy '695 further defines "[l]ow stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8×10^8 dynes/cm^2 (preferably 1×10^7 dynes/cm^2) in tension." *Id.* at 11:33–37. Additionally, Leedy '695 discloses two chemical vapor deposition (CVD) process recipes for manufacturing "structurally enhanced low stress dielectric circuit membranes." *Id.* at 11:51–65.

Referring to Figure 8, Leedy '695 discloses a three dimensional circuit membrane. *Id.* at 4:43. Figure 8 is reproduced below.

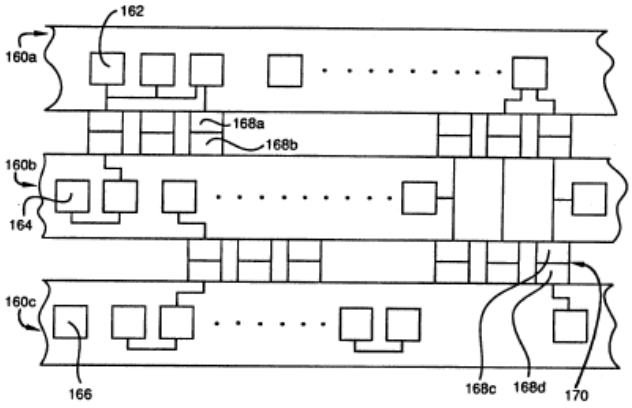


Fig_8

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three dimensional circuit structure. *Id.* at 16:38–40. Interconnection between circuit membranes 160a, 160b, 160c including SDs 162, 164, 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between 4 μm and 25 μm in diameter) on the surface of two circuit membranes 160b, 160c and using a mechanical or gas pressure source to press bond pads 168c, 168d together. *Id.* at 16:43–49.

iv. Analysis

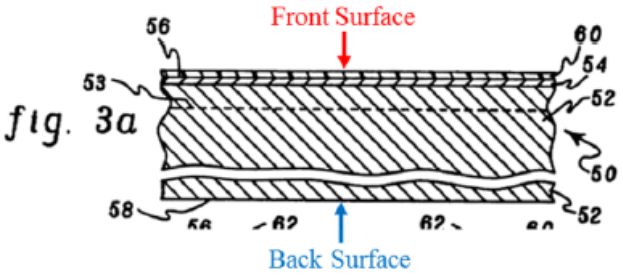
Petitioner argues that claims 1–3, 30, 31, 33, 40, 41, and 44 are obvious over the combination of Bertin '754, Poole, and Leedy '695. *See* Pet. 3. Below we discuss independent claim 1, which is illustrative of the subject matter of claims 2, 3, 30, 31, 33, 40, 41, and 44.

a) "Substantially flexible" limitations

Claim 1 is directed to a stacked integrated circuit, that includes "at least one of the first integrated circuit and the one or more additional integrated circuits is *substantially flexible* and comprises a *substantially*

flexible semiconductor substrate of one piece made from a semiconductor wafer thinned by at least one of abrasion, etching and parting, and subsequently polished to form a polished surface." Emphasis added.

Petitioner asserts that "Bertin teaches or suggests all but a few features recited in claims 1–3, 30, 31, 33, 40, 41, and 44, as construed by Petitioner." Pet. 22. Regarding claim 1, Petitioner relies on one of the stacked chips of Bertin '754's "three-dimensional multichip package having a densely stacked array of semiconductor chips" as the recited stacked integrated circuit comprising and first integrated circuit recited in claim 1. *Id.* at 28–30. Petitioner further provides the following annotated Figure 3a from Bertin '754 to explain its combination. *Id.* at 31 (depicting annotations of Bertin '754's Fig. 3a).



According to Petitioner, annotated Figure 3a shows stacked integrated circuit 50 with substrate 52. *Id.* at 30–31.

With respect to the "substantially flexible" limitations recited in claim 1, Petitioner argues that Bertin '754's substrate 52 is "substantially flexible" because Bertin '754 teaches that each device 50 may only be 20 micrometers or less, which means that substrate 52 within stacked devices 50 must also be 20 μm or less. Pet. 33 (citing Ex. 1004, 3:25–46, Fig. 2b). Petitioner adds that Bertin '754's substrate 52 is thinned by a conventional wet etching process, which begins "'with a semiconductor device 50 (preferably

comprising a wafer) having a substrate 52' thickness of 'approximately 750-800 micrometers (15 mils).'" Pet. 33 (citing Ex. 1004, 3:50–65, Figs. 3a–3e). Further, Petitioner argues Bertin '754 teaches that "[a]fter thinning, the stacked 'semiconductor chips . . . have only a thin layer of substrate for support of the active layer,' such that the overall thickness of each chip is '20 micrometers or less.'" *Id.* at 34 (citing Ex. 1004, 3:25–38, Fig. 2b). Petitioner adds that it would have been obvious to subsequently polish or smooth thinned substrate 52 with Poole's two-step thinning/polishing process. *Id.* at 33–35.

In response to the Petition, Patent Owner argues that Petitioner applies an incorrect construction of "substantially flexible" and has failed to adequately explain how the asserted combination teaches or suggests a "substantially flexible semiconductor substrate" and "substantially flexible" integrated circuit. PO Resp. 57–58. As discussed previously, Patent Owner asserts that the ordinary and customary meaning of "substantially flexible semiconductor [] substrate" is "a semiconductor substrate that is largely able to bend without breaking" and is the proper claim construction. Similarly, Patent Owner argues that the same ordinary and customary meaning applies to "substantially flexible" integrated circuit. *See* Tr. 32:1–24. As discussed above, we agree with Patent Owner's construction. *See supra* Section II.A.1.

In its Reply to Patent Owner's Response, Petitioner contends that Patent Owner's "response is premised on an incorrect claim construction of 'substantially flexible'" and "[u]nder a proper construction, [Patent Owner] offers no rebuttal to the conclusion that the 'substantially flexible' limitations are met." Reply 3; 29–31 (arguing that the "Board should reject

Patent Owner's newly proposed construction"). Nonetheless, Petitioner does not address in its Reply how the claims as Patent Owner construes them would have been obvious over the asserted prior art. *See generally* Reply. Rather, Petitioner argues that the prior art shows a particular thinning of a substrate, but Petitioner does not argue that the combination of Bertin '754, Poole, and Leedy '695 would have conveyed to one of ordinary skill in the art a substrate that is (largely) able to bend without breaking, which is required by the construction of substantially flexible semiconductor substrate. *Id*. Likewise, Petitioner does not argue that the combination of Bertin '754 and Poole would have taught or suggested an integrated circuit that is largely able to bend without breaking.

In essence, Petitioner argues that Bertin '754's disclosure of substrate and integrated circuit thinness is sufficient to teach flexibility. Nonetheless, a preponderance of the evidence establishes, however, that, in the context of semiconductor substrates, mere thinning is not the same as flexibility—being able to bend without breaking. The Examiner, during the prosecution history of the now-abandoned '652 application, agreed that flexibility is not the equivalent of mere thinning. Ex. 2168, 4 (The Examiner indicating that "Bertin '754 also fails to specifically teach wherein at least one of the first and second circuit layers is substantially flexible."). Neither party disputes this characterization of the Examiner's statement. PO Resp. 34–36 (Patent Owner indicating that the "Examiner agreed that flexibility is not the equivalent of mere thinning." (quoting Ex. 2168, 4)); Tr. 24:23–25:1 (Petitioner's counsel agreeing with Patent Owner's characterization that flexibility is not the equivalent of mere thinning).

Moreover, Petitioner's expert, Dr. Franzon, also testifies that the flexibility of a semiconductor substrate and integrated circuit depend on a number of factors, only one of which is the physical dimensions of the substrate—width and thickness. Ex. 1002 ¶ 71. Specifically, Dr. Franzon stated:

> In the context of semiconductor processing, the flexibility of a semiconductor substrate depends on a number of factors, including, for example, the type of semiconductor substrate (e.g., while silicon and gallium arsenide are both semiconductors, they have different elastic moduli), the crystal orientation of the material (e.g., {100} and {111} silicon wafers have different elastic moduli), and the physical dimensions of the substrate (e.g., width and thickness). The flexibility of a more complex structure, such as an integrated circuit, that comprises multiple different layers of different materials (e.g., semiconductors, dielectrics, conductors), must take into account additional factors, including the type and dimensions of all the materials in that structure.

Ex. 1002 ¶ 71; *see also* Tr. 33:8–24 (Patent Owner's counsel at oral hearing discussing Dr. Franzon's testimony about the factors on which flexibility of a semiconductor substrate depends); Tr. 64:16–65:11 (Petitioner's counsel responding to Patent Owner's argument about Dr. Franzon's testimony regarding the various factors that would be considered to determine whether something is flexible). Common sense also supports a conclusion that thickness is not the only factor that determines whether a material is flexible. After all, a thicker piece of rubber is more flexible than a thinner potato chip.

In addition, Petitioner's counsel argued at the Oral Hearing that the asserted art shows bendability in addition to thinning because the asserted

"prior [art] mirrors the prior [preferred] embodiment" described in the '542 patent. Tr. 175:21–176:2. Petitioner's counsel did not identify with particularity any portion of the asserted prior art that "mirrors" the preferred embodiment in the challenged patent, nor even identify what preferred embodiments Petitioner counsel had in mind as being mirrored by the prior art. Furthermore, Petitioner does not otherwise point to sufficient evidence to support its position that the prior art mirrors these embodiments in the challenged patent. *See generally* Tr. 175:13–180:16. For example, Petitioner contends that Dr. Franzon's testimony that the limitations are met by the prior art supports its position. Tr. 178:20–22 (Asking "is there any evidence of record that any of the combinations that you propose would be the same as the preferred embodiment"?); Tr. 180:8–10 (Petitioner's counsel responding that "[i]t's Dr. Franzon's testimony that those limitations are met by the prior art, and it's the prior art itself, lining up with the claims.").

Dr. Franzon, however, testifies that he was given Petitioner's proposed constructions of "substantially flexible semiconductor substrate" (i.e., "a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed"; "a semiconductor substrate that has been thinned to a thickness of less than 50 μm"; and "a semiconductor substrate that has been thinned to a thickness of 150 μm or less"), and he "applied Petitioner's construction in [his] analysis." Ex. 1002 ¶¶ 72–73. With regard to "substantially flexible" integrated circuit and

circuit substrate, Dr. Franzon indicates that even though "the term has an uncertain meaning," he applied the Petitioner's construction in his analysis.[9]

We are mindful that Petitioner has the burden "to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3)). Accordingly, we are not persuaded that Petitioner has demonstrated by a preponderance of the evidence that the prior art embodiments mirror the preferred embodiment in the challenged patent and, therefore, the prior art shows bendability. Furthermore, Petitioner's counsel at the Oral Hearing confirmed that Petitioner's Reply to Patent Owner's claim construction position is that "first and foremost their claim construction is improper because it is indefinite, so in drafting the reply, . . . we couldn't figure out how to apply their construction to the prior art, so the claim construction portion of the reply explains why their construction is incorrect." Tr. 176:7–12.

[9] Petitioner provided Dr. Franzon with three alternative proposed constructions of "substantially flexible" integrated circuit/circuit substrate. These being: (1) "an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed, and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm^2 tensile or less"; (2) "an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of less than 50 μm, and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm^2 tensile or less"; and (3) "an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of 150 μm or less." Ex. 1002 ¶¶ 76–77.

For these reasons, we determine that Petitioner has not demonstrated by a preponderance of the evidence that the combination of Bertin '754, Poole, and Leedy '695 would have conveyed to one of ordinary skill in the art the "substantially flexible semiconductor substrate," as recited in independent claim 1 and required in claims 2, 3, 30, 31, 33, 40, 41, and 44, which depend from claim 1.

For many of the same reasons discussed above, we are further not persuaded that Petitioner has demonstrated that Bertin '754, Poole, and Leedy '695 teach or suggest a "substantially flexible" circuit substrate or integrated circuit. Ex. 1001, claims 1, 40. For example, Petitioner does not argue that the combination of Bertin '754, Poole, and Leedy '695 would have taught or suggested an integrated circuit or circuit layer that is largely able to bend without breaking. Reply 29–31. Rather, as with "substantially flexible" semiconductor substrate, Petitioner relies heavily on its proposed construction that we have not adopted.

Additionally, Petitioner's reliance on Poole does not overcome this deficiency. Petitioner suggests applying Poole's two-step thinning process to Bertin '754 to achieve the "predictable result of a thin substrate with a planar surface having minimal defects which is desired in Bertin '754 to facilitate the formation of reliable vertical interconnects and bonds between substrates." Pet. 27. Petitioner has not made a sufficient case for why one of ordinary skill would have applied Poole's process to the structures of Bertin '754. Further, Petitioner has not made the case for why doing so would have satisfied the "substantially flexible" claim requirements.

Dr. Franzon's testimony is also unhelpful in this regard. Dr. Franzon states that "the [substantially flexible] term has an uncertain meaning" and

that he simply applied the Petitioner's three different construction in his analysis.[10] Ex. 1002 ¶¶ 76–77. However, none of the applied constructions provided by Petitioner takes into account the ordinary and customary meaning of "substantially flexible" integrated circuit/circuit substrate, which we have adopted.

Accordingly, based on the complete record, we determine that Petitioner also has not demonstrated by a preponderance of the evidence that the proposed combination of Bertin '754, Poole, and Leedy '695 would have conveyed to one of ordinary skill in the art the "substantially flexible" integrated circuit (claims 1–3, 30, 31, 33, 40, 41, and 44) and circuit substrate (claims 40, 41).

b) Low Tensile Stress Dielectric Substitution

Additionally, for all of the challenged claims, Petitioner asserts that "[i]t would have been obvious to one of ordinary skill in the art at the time of the alleged invention . . . to modify the processes and device in Bertin such that each of the dielectric layer 60 and the interconnect insulators

[10] Petitioner provided Dr. Franzon with three alternative proposed constructions of "substantially flexible integrated circuit/circuit substrate." These being: (1) "an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed, and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm^2 tensile or less"; (2) "an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of less than 50 μm, and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm^2 tensile or less"; and (3) "an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of 150 μm or less." Ex. 1002 ¶¶ 76–77.

constitute a dielectric characterized by a tensile stress of about 5×10^8 dynes/cm^2 or less, based on the disclosure of Leedy '695. Pet. 22 (citing Ex. 1002 ¶¶ 104–114, 124[11]); *see id.* at 32–35, 36–37 (claim 2 recites and requires "a low stress dielectric."). Although claim 1 does not recite a low stress dielectric, Petitioner's proposed construction of a "substantially flexible" integrated circuit includes a dielectric material with a stress of 5×10^8 dynes/cm^2 tensile or less." Dependent claims 2, 3, 30, 31, 33, 40, and 41 require a "low stress dielectric."

For the reasons that follow, we determine that Petitioner has not demonstrated by a preponderance of the evidence that one of ordinary skill in the art would have had a reason to combine the references in the manner proposed by Petitioner to arrive at the claimed invention and would have had a reasonable expectation of success.

1. Reason to Substitute

To start, Petitioner first contends that the Office already found that the combination of Bertin '754 and Leedy '695 teaches or suggests these features during prosecution of related applications. Pet. 22 (citing Ex. 1033–1036). Petitioner, however, does not acknowledge, much less address adequately, the significant difference in the record before the Office, which lacked the testimonial evidence of the Petitioner's expert, Paul D. Franzon,

[11] Notably, Petitioner merely cites Dr. Franzon's twenty-one page claim chart for this element, without otherwise discussing or summarizing it. Board rules prohibit incorporating by reference arguments from one document into another document. 37 C.F.R. § 42.6(a)(3); *see Cisco Sys., Inc. v. C-Cation Techs., LLC*, Case IPR2014-00454, slip op. at 7–10 (PTAB August 29, 2014) (Paper 12) (Informative) (not considering arguments in declaration that were not made in the Petition but only incorporated by reference).

Ph.D. (Ex. 1002 (declaration); Ex. 2164 (deposition transcript)) and testimonial evidence of Patent Owner's expert, Alexander D. Glew, Ph.D. (Ex. 2166 (declaration)). Thus, we are not persuaded that the prosecution history of related applications is controlling here.

Next, Petitioner refers to many general benefits and advantages of Leedy '695's disclosed dielectric, but does not explain how these advantages apply to the specific dielectric materials in Bertin '754. For example, Petitioner asserts that

> Leedy '695 provides express motivations for modifying Bertin's processes and device to incorporate Leedy '695's low tensile stress dielectric material. *See KSR*, 550 U.S. at 415-421. Leedy '695 explains that low tensile stress is important because otherwise "surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane." *See, e.g.*, Ex. 1006 at 5:63-6:5; Ex. 1002 at ¶ 110. Accordingly, as discussed above, Leedy '695 describes processes for depositing silicon oxide or silicon nitride dielectric material, preferably having a tensile stress of 1 x 10^7 dynes/cm^2. *See, e.g.*, Ex. 1006 at 11:33-37. Leedy '695 explains that the described low tensile stress dielectrics can advantageously be used to insulate circuit devices and interconnect metallization, while at the same time increasing structural integrity and durability. See, e.g., Id. at Abstract, 1:53-62, 2:9-31, 2:66-3:3, 3:56-4:13, 30:36-42, 45:49-46:26, 46:52-47:33, Figs. 32a-32d. Leedy '695 also explains that such dielectrics advantageously have lower stress than thermally grown oxides, like those used in Bertin. Id. at 6:30-33.

Pet. 23–24.

We first observe that Petitioner incorrectly attributes benefits of the entire Membrane Dielectric Isolation (MDI) process to the single low stress dielectric component. *See* Pet. 24 (citing Ex. 1006, 2:9–31, 2:66–3:3, 3:56–

4:13, 30:36–42, 45:49–46:26). For example, column 2, lines 9 through 31 of Leedy '695 provides

> [t]he primary objectives of the MDI fabrication technology disclosed herein are the cost effective manufacture of high performance, high density integrated circuits and integrated circuit interconnect with the elimination or reduction of detrimental electrical effects on the operation of individual circuit devices (e.g. diodes, transistors, etc.) *by completely isolating with a dielectric material* each such circuit device from the common substrate upon which they are initially fabricated, and therefore, from each other, and to provide a more versatile and efficient physical form factor for the application of integrate circuits. Some of the benefits of the *MDI IC fabrication process* are the elimination or reduction of substrate current leakage, capacitive coupling and parasitic transistor effects between adjoining circuit devices. The *MDI IC fabrication process* benefits extend to several other categories of IC fabrication such as lower IC processing costs due to fewer IC isolation processing steps, greater IC transistor densities through the capability to use established IC processing techniques to fabricate interconnect metallization on both sides of a MDI IC circuit membrane, and greater IC performance through novel transistor structures.

Ex. 1006, 2:9–31 (emphasis added). Here, Leedy '695 indicates that these advantages are due to the MDI fabrication processes (e.g., Method #1 and Method #2), which are multi-step processes that include, but are not limited to, the formation of a low stress dielectric and optional isolation with a dielectric material. Ex. 1006, 7:1–11:24; *see also id.* at 2:66–3:3 ("It is the *combination* of the use of low stress free standing dielectric films with the appropriate processing qualities and membrane or thin film single crystalline (monocrystalline), polycrystalline or amorphous semiconductor substrate formation that provides much of the advantage of the MDI IC fabrication

process.") (emphasis added); *see, eg.*, *id.* at 3:56–4:13 (Listing benefits to fabricating an IC with the *MDI process*).

Looking to another passage cited by Petitioner, column 30, lines 36 through 42 of Leedy '695 also refers to the MDI IC process in its entirety for the ability to form a flexible and elastic membrane structure. Ex. 1006, 30:36–42. Thus, rather than supporting Petitioner's position that the *low stress dielectric* provides flexibility, this cited passage also refers to the MDI process as a whole and does not support Petitioner's assertion that Leedy '695's low stress dielectric alone imparts these benefits.

Additionally, other citations by Petitioner discuss advantages of its low tensile stress dielectric flexible *membrane* or its *membrane dielectric isolation fabrication* techniques. *See*, *e.g.*, Ex. 1006, Abstract ("In another version, the flexible membrane is used as support and electrical interconnect for conventional integrated circuit die bonded thereto, with the interconnect formed in multiple layers in the membrane."); 1:53–62 ("In accordance with the invention, an integrated circuit is formed on a tensile low stress dielectric membrane comprised of one layer or a partial layer of semiconductor material in which are formed circuit devices and several layers of dielectric and interconnect metallization. Also, a structure in accordance with the invention is a tensile member of semiconductor material in which are formed circuit devices with multiple layers of tensile low stress dielectric and metallization interconnect on either side of the semiconductor membrane."); *see id.* at 46:52–47:33 (teaching that the dielectric circuit *membranes* are optically transparent and thin, allowing the circuit membranes to be aligned very accurately prior to bonding; and MDI circuit membrane can be cut from the circuit membrane due to the net low stress of the circuit membrane).

Thus, the probative value of Petitioner's argument is diminished because Leedy '695 does not support Petitioner's position that the low stress dielectric alone imparts the advantages described in the cited passages directed to the membrane structure or membrane isolation techniques.

Further, Petitioner's reliance on express reasons that low tensile stress is important for Leedy '695's process for constructing Leedy '695's low tensile stress dielectric membranes (e.g., surface flatness) has minimal probative value in supporting Petitioner's proposed substitution of Bertin '754's dielectric material, which is fabricated in a different process relying on a conventional, rigid substrate. This is because Petitioner does not explain sufficiently why or how the importance of low tensile stress for Leedy '695's process for constructing low tensile stress dielectric membranes bears on why one of ordinary skill in the art would have substituted Leedy '695's dielectric material for Bertin '754's dielectric layer 60 and interconnect insulators. Indeed, Petitioner does not explain why a person of ordinary skill in the art would replace Bertin '754's dielectric 60 and interconnect insulators with a low stress dielectric where the dielectric material disclosed in Bertin '754 already insulates and interconnects the circuit structure. Tr. 85:11–12 ("So I think at a fundamental level all dielectric layers perform an insulating function."). For example, Petitioner does not argue that Bertin '754's *dielectric 60* or *interconnect insulators* experience surface flatness or other structural problems that would be improved by the use of a low stress dielectric, or how this substitution would be accomplished in light of the fabrication processes disclosed in Leedy '695. *See* Pet. 22–24.

Petitioner additionally argues that

> Bertin and Leedy ’695 are both directed to the improvement of integrated circuits and recognize the central role the fabrication process plays in facilitating this improvement. See, e.g., Ex. 1004at 1:7-2:31; Ex. 1006 at 1:38-67, 3:56-4:13. In fact, both disclosures specifically seek to achieve high density integrated circuits, including 3D integrated circuits. See, e.g., Ex. 1004 at 1:7-15, 1:55-2:31; Ex. 1006 at Abstract, 2:9-14, 45:49-59, 47:31-33. Therefore, one of ordinary skill in the art would have been encouraged to look to the teachings in Leedy ’695 to improve the teachings in Bertin. See KSR Int’l Co. v. Teleflex Inc., 550 U.S. 398, 415-421 (2007); Ex. 1002 at ¶ 114.

Pet. 23. We understand Petitioner’s position to be that Bertin ’754 and Leedy ’695 were directed generally to similar general goals and problems in the semiconductor fabrication arts, and a skilled artisan would have looked at both references to improve upon fabrication processes. However, based on the complete record here, Petitioner’s “reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.” *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017). While the references need not explicitly provide a reason for the asserted substitution, Petitioner must, nevertheless, explain why a person of ordinary skill in the art would have substituted Leedy ’695’s low stress dielectric for the specific dielectrics in Bertin ’754. “[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk–Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015).

We recognize that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill" (*KSR*, 550 U.S. at 417). Here, however, Petitioner's testimony is conclusory without explaining what types of improvements in 3D integrated circuits would have motivated one of ordinary skill in the art to make Petitioner's proposed substitution of Leedy '695's dielectric in Bertin '754's device. *In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) ("The factual inquiry whether to combine references must be thorough and searching.")).

In addition, Petitioner cites to paragraph 114 of Dr. Franzon's declaration testimony without further discussing or explaining the relevance of the testimony. Pet. 23 (citing Ex. 1002 ¶ 114). Dr. Franzon's testimony in paragraph 114 is conclusory. Ex. 1002 ¶ 114 (asserting "[a] person of ordinary skill in the art would have been encouraged to combine Leedy '695 with each of Bertin (alone or in combination with Poole) and Hsu because they are in the same technological field of three-dimensional integration and address similar challenges relating to the stacking of integrated circuit devices." (citing Exs. 1004, 1006, 1008)). Although "any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed" (*KSR*, 550 U.S. at 420), Dr. Franzon's single sentence assertion lacks specifics as to what those similar challenges are, and he only provides a list of citations to various references without further explanation or

analysis as to how those citations support his assertion. Thus, we weigh Dr. Franzon's testimony accordingly. *See In re Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); *see also* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

Petitioner further argues that the replacement of one dielectric for another is a matter of simple substitution because Leedy '695 uses a plasma-enhanced chemical vapor deposition ("PECVD") to deposit the low tensile stress dielectrics, and "PECVD was a well-known and widely used technique that provided conformal deposition at lower substrate temperatures and at faster rates compared to other depositions techniques." Pet. 24 (citing Ex. 1006, 11:28–63; Ex. 1039; Ex. 1040, 171). Petitioner adds that "dielectrics can easily be used in place of other dielectrics, including thermal oxide insulators, like the interconnect insulators disclosed in Bertin, which Leedy '695 indicates have high stress." Pet. 24 (citing Ex. 1006, 6:30–33, 8:59–64; Ex.1002 ¶ 113).

Petitioner further relies on other prior art references to support its position that PECVD was compatible with various stages in the fabrication process. *See* Reply 10–15. On this point, Petitioner's position is that Bertin '754's thermally grown oxide dielectric could have been simply substituted with the PECVD dielectric in Leedy '695. *Id.; see also id.* at 3 (Heading: "3D IC Dielectrics Could Have Been Replaced with Leedy '695's PECVD LTSDS"). However, again, Petitioner argues a substitution *could* be made, which is not sufficient to show that a substitution *would* have been made.

Additionally, paragraph 113 of Dr. Franzon's declaration indicates that "Leedy '695 discloses using [plasma-enhanced chemical vapor deposition], which was a commonly available deposition technique that *could have been used* in place of the techniques for growing or depositing dielectrics described in Bertin and Hsu to obtain the predictable result of stacked integrated circuits having low tensile stress dielectrics." Ex. 1002 ¶ 113 (emphasis added). Testimony that one of ordinary skill in the art *could have used* the techniques is not sufficient to support Petitioner's contention that one of ordinary skill in the art would have had a reason to combine the references as proposed by Petitioner in the manner of the claimed invention. *In re Giannelli*, 739 F.3d 1375, 1380 (Fed. Cir. 2014) (indicating that the Board should have determined whether it would have been obvious to modify the prior art apparatus to arrive at the claimed invention and finding the mere capability to do so insufficient).

In Reply, Petitioner contends, without support of expert or citation to law, that "the lack of disclosure of 'tensile' dielectrics or how to make a [low tensile stress dielectric, aside from incorporating a § 102(b) reference, indicates that it was trivial to substitute Leedy '695's [low tensile stress dielectrics] in place of other dielectrics. Reply 2. We disagree with Petitioner—one does not necessarily follow from the other.

Similarly, we disagree with Petitioner's conclusory position that the technical obstacles to incorporating Leedy '695's dielectric into prior art integrated circuits (such as Bertin's) are not "real or the challenged claims would not be enabled." Pet. Reply 2–3; *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements.").

Leedy ’695 sets forth sixty-four pages of figures and more than forty-six columns of text to describe his membrane dielectric isolation integrated circuit fabrication techniques and did not also need to explain in detail specific ways to substitute its techniques for those in a conventional integrated circuit fabrication process to obtain the patent. Notably, Petitioner’s position is based on attorney argument. Accordingly, we determine Petitioner’s conclusory assertions in its Reply are insufficient to overcome Patent Owner’s well-reasoned and supported arguments.

2. Expected Success

In addition, it is Petitioner’s burden to demonstrate both “that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” *Intelligent Bio-Systems, Inc. v. Illumina Cambridge LTD.*, 821 F.3d 1359, 1368–1369 (Fed. Cir. 2016) (citing *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.* 688 F.3d 1342, 1360 (Fed.Cir.2012). In considering the record before us, we take into account the complexity of integrated circuit fabrication. Without question, fabrication of integrated circuits is complex technology. No less than four prior art text books, ranging from 600 pages to nearly 850 pages and describing the fabrication of integrated circuits, have been provided as background references, principally in support of the declaration testimony ofAlexander D. Glew, Ph.D., Patent Owner’s expert. Ex. 1040 (Wolf et al., *Processing for the VLSI Era, Volume 1–Process Technology* (1986)); Ex. 2146 (Wolf, Silicon Processing for the VLSI Era, Volume 2 – Process Integration (1990)); Ex. 2159 (W. R. Runyan & K. E. Bean, Semiconductor Integrated Circuit Processing Technology (1990)); Ex. 2162 (Multi-Chip

Module Technologies and Alternatives: The Basics (Daryl Ann Doane & Paul D. Franzon eds., 1993)). Also of record are two other background references of around 100 pages and 650 pages. Ex. 2169 (Handbook of Semiconductor Manufacturing Technology (Robert Doering & Yoshio Nishi eds., 2nd ed. 2008); Ex. 2158 (Peter van Zant, Microchip Fabrication (4th ed., 2000)).

Patent Owner, with liberal citations to those references, other prior art references, and declaration testimony of its expert explaining the same, explains how integrated circuits are fabricated to illustrate the complexity of the process and the detailed planning and decisions required for fabrication. PO Resp. 3–30. According to Dr. Glew integrated circuit fabrication is a "complex manufacturing process . . . that can be generally divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. Ex. 2166 ¶ 23 (citing Ex. 2158, 13[12,13]); *see also* PO Resp. 5 (citing Ex. 2166 ¶ 23; Ex. 2158, 13). In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and then sliced into thin disks called

[12] We follow Patent Owner's practice of citing to page numbers of the text, rather than the pagination of Exhibit 2158.

[13] We recognize that the text cited by Dr. Glew (Ex. 2158) is the fourth edition and has publication dates of 1984, 1997, and 2000. Dr. Glew relies on this text as supporting his testimony and recognizes the earliest effective filing date claimed by the challenged patent of April 4, 1997. Ex. 2166 ¶ 104. Petitioner does not contend that Dr. Glew's reliance on this text is in error or that Dr. Glew's summary of integrated circuit fabrication is faulty. Nor does Petitioner contend that the general explanation of integrated circuit fabrication found in the text, and used by Dr. Glew to support his testimony, changed between the 1997 edition of the text and the later editions.

"wafers." PO Resp. 6 (citing Ex. 2166 ¶ 25; Ex. 2158, 13–14). Most helpful is the explanation of different techniques for producing and layering dielectrics (PO Resp. 16–30), including growing dielectrics using thermal oxidation (PO Resp. 18–19), depositing dielectrics (PO Resp. 19), and a comparison of thermal chemical vapor deposition (PO Resp. 20) with plasma-enhanced chemical vapor deposition (PO Resp. 21).

We understand from the testimony of Dr. Glew and reference citations that a typical fabrication of a semiconductor integrated circuit may include thousands of process steps (Ex. 2166 ¶ ¶ 29–30 (citing Ex. 2158, 14, 29–31, 71)). Explaining different techniques for producing and layering dielectrics, Dr. Glew explains that "different dielectric materials are layered throughout the fabrication process, with each dielectric layer having a different location, each being created at a different stage, and each serving a different specific purpose." Ex. 2166 ¶ 61 (citing Ex. 2158, 72–73, 79, 81–82); *see generally* PO Resp. 16–30 (discussing different techniques for producing and layering dielectrics). Dr. Glew continues:

> These dielectrics can be produced and layered using a large number of techniques, and the particular technique used will greatly impact the properties of the resulting dielectric (and, therefore, its usefulness for any particular dielectric layer and purpose). For example, dielectric silicon dioxide layers can be produced and applied in hundreds of different ways, each resulting in a silicon dioxide with different properties (and potential uses). (Ex. 2158 at 154; Ex. 2146 at 225, 306; Ex. 2159 at 55).

Ex. 2166 ¶ 62. Thus, selecting a dielectric material involves choosing particular fabrication techniques that are part of an overall fabrication process for a particular integrated circuit.

Turning again to the Petition, Petitioner asserts that

> [g]iven Leedy '695's explanation that such dielectrics are versatile, in that they are able "to withstand a wide range of IC processing techniques and processing temperatures (of at least 400 C.) without noticeable deficiency in performance" (Ex. 1006 at 2:37-40; *see also id.* at 1:50-52, 5:32-33), one of ordinary skill in the art would have reasonably expected success combining the teachings of Bertin and Leedy '695. *See KSR*, 550 U.S. at 415-421. In addition, as mentioned above, Leedy '695 discloses using PECVD, which was a commonly available deposition technique that could have been used in place of the techniques for growing dielectrics described in Bertin to obtain the predictable result of stacked integrated circuits having low tensile stress dielectrics. *Id.*; Ex. 1002 at ¶¶ 110-113.

Pet. 25.

Based on the complete record, we determine that Petitioner's arguments and conclusion are insufficiently supported. The fact that plasma-enhanced chemical vapor deposition was well-known, commonly available, and has recognized advantages does not sufficiently support Petitioner's conclusion in view of the complexities of integrated circuit fabrication. Furthermore, Petitioner's assertion that "dielectrics can be easily used in place of other dielectrics" (Pet. 22) is not supported by the record. Petitioner's citations to Leedy '695 (Ex. 1006, 6:30–33, 8:59–64) do not on their face, without explanation, support Petitioner's position. Petitioner's citation to column 6 indicates: "[t]hermally formed silicon dioxide forms as a strongly compressive film and most deposited dielectics current in use form typically with compressive surface stress." Ex. 1006, 6:30–33. Petitioner's citation to column 8 similarly requires further explanation regarding how it supports Petitioner's assertion that "dielectrics can be easily used in place of other dielectrics" (Pet. 22): "[t]he thermal

oxide isolation created by the LOCOS[14] method may change the net tensile surface stress of the semiconductor (substrate) membrane layer. The deposition of low stress dielectric films on either side of the semiconductor layer prior to LOCOS processing will offset most compressive effects of the oxide formation." Ex. 1006, 8:59–64. The fact that Leedy '695 discloses that the use of a particular method—LOCOS—could be used in either of its two recipes for membrane dielectric isolation fabrication does not, without more, suggest that Leedy '695's dielectrics "could be easily" used in place of other dielectrics.

Even setting aside the fact that Petitioner cites but does not discuss its expert's testimony that Petitioner cites in its Petition,[15] Dr. Franzon does not explain how the cited portions of Leedy '695 show "its dielectrics can be easily used." The fact that plasma-enhanced chemical vapor deposition was a well-known process capable of providing TSV insulation (Ex. 1002 ¶ 111) does not in itself indicate that Leedy '695's alternative processes "could have been easily used" in place of Bertin '754's techniques, particularly in view of the complexities of integrated circuit fabrication.

Dr. Franzon further testifies that Leedy '695 explains its *membrane* can be used with "most of the established integrated processing methods for the fabrication of circuit devices and interconnect metallization" or its membrane "is compatible with most higher temperature [integrated circuit] processing techniques." Ex. 1002 ¶ 113. Again, for purposes of addressing Petitioner's arguments, we overlook the fact that Petitioner cites to this

[14]LOCOS (LOCal Oxidation of Silicon) isolation method." Ex. 1006, 8:43.
[15] 37 C.F.R. § 42.6(a)(3) (prohibiting incorporation by reference from one document to another).

testimony without discussing it in its Petition. Dr. Franzon's testimony, while indicating Leedy '695's *membrane* can be used with some conventional methods, does not adequately support Petitioner's contention that "dielectrics can be easily used in place of other dielectrics" (Pet. 22); see also Ex. 1006, 2:37–40 ("The ability to make a large area flexible thin film free standing dielectric *membrane*, typically framed or suspended or constrained at its edges by a substrate frame or ring, or bonded frame or ring. This *membrane* is able to withstand a wide range of IC processing techniques and processing temperatures (of at least 400° C.) without noticeable deficiency in performance."). Thus, we conclude that Petitioner's citation to Dr. Franzon's testimony is unavailing. Pet. 22 (citing Ex. 1002 ¶¶ 99–102).

Moreover, as discussed in detail below, both Dr. Franzon and Dr. Glew agree that dielectrics have different properties and different methods of forming dielectrics in integrated circuit fabrication result in dielectrics having different properties. *See, e.g.*, Ex. 2164 (Dr. Franzon deposition transcript), 69:17–19 (Q. Do the different methods result in different properties of the dielectrics? A. Yes."); Ex. 2166 (Dr. Glew's declaration) ¶ 139 (Identifying eighteen properties[16] of dielectrics; testifying

[16] Dr. Glew identifies the following properties of dielectrics: dielectric constant, breakdown of field strength, leakage, surface conductance, moisture absorption or permeability to moisture, stress, adhesion to aluminum, adhesion to other dielectric layers, stability, etch rate, permeability to hydrogen, amount of incorporated electrical charge or dipoles, amount of impurities, quality of step coverage, thickness and uniformity of the film, ability to provide good doped uniformity across a wafer, defect density, and amount of residual constituents that "outgas" during later processing. Ex. 2166 ¶ 139.

that one of ordinary skill in the art would consider many of those factors when choosing a dielectric); *see also* PO Resp. 59–60 (discussing Dr. Franzon's and Dr. Glew's testimony); *see also* Ex. 2146 (Wolf Volume 2), 195 (Table 4.4 listing eighteen desired properties of interlevel dielectrics); PO Resp. 33 (citing Ex. 2146, 195); Tr. 125:12–17 (Patent Owner's counsel referencing Ex. 2146, 195 (table of eighteen properties). Dr. Franzon acknowledges dielectric properties should be considered when selecting a dielectric. Ex. 2164 (Dr. Franzon deposition transcript), 59:25–60:2, 61:10–13, 79:25–80:3, 91:8–12); Ex. 2164, 78:23–79:1 (Dr. Franzon testifies that "[t]here is likely quite a long list of factors that go into choosing between them [dielectrics], and an engineer would weigh those using his knowledge and skills."). This weighs against a finding that one of ordinary skill in the art would have reasonably expected success in substituting Leedy '695's low tensile stress dielectric material for Bertin '754's dielectric layer 60 and interconnect insulators.

In reviewing Dr. Franzon's testimony, we are mindful of the sentiment that "[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton." KSR, 550 U.S. at 421. However, in his deposition, Dr. Franzon responded to many questions about dielectrics by indicating research would be needed to answer the particular question and he did not consider how the different processes would affect dielectric properties, which weighs against a finding that one of ordinary skill would have a reasonable expectation of success in substituting Leedy '695's dielectric. *See* Ex. 2164, 133:5–135:5. For example, an excerpt of Dr. Franzon's testimony is provided below:

> Q. What are some of the differences in the properties of a silicon dioxide grown through plasma-enhanced CVD as opposed to grown through oxidation?
>
> A. I haven't researched a detailed answer to that question. There is many variations on the formulas for these CVDs.
>
> Q. But you understand that there is a difference. Right?
>
> THE WITNESS: There may be differences, depending on the details of the formulations and the processing parameters and so forth.
>
> Q. What are some of the details of the formulation parameters that you would need to know in order to answer that question?
>
> A. I haven't researched the answer to that question in general, so I would need a variety of references that I can't anticipate in order to properly answer that question.

Ex. 2164, 133:8–134:3; *see, e.g.*, Ex. 2164, 71:9–73:17 ("Q. Do you consider oxidation to be a growth or a deposition?" A. I haven't researched that answer to the question. Thermal oxidation [requires] oxygen atoms in contact with the surface, at least, in order to grow the thermal oxide. But there's a lot of variance on thermal oxide techniques that I haven't researched. Q. And can you give me an example of some variants in thermal oxide techniques? A. One example that comes to mind is a wet oxide deposition versus a dryer one. Q: And does a wet oxide deposition versus a drier one cause different arrangements of the bonds in silicon dioxide? A: I haven't researched the answer to that question. . . . Q: Do you know if wet oxide versus dry oxide would affect the dielectric constant of silicon dioxide? A. I haven't researched the answer to that question. Q. Do you know if PDCVD [sic] would result in a different dielectric constant than thermal oxide? A. I haven't researched the answer to that question.").

We are not suggesting that a reasonable expectation of success in the complex field of integrated circuit fabrication would preclude one of ordinary skill in the art from researching aspects of making the combination. Rather, we find the number of Dr. Franzon's responses that research is required weighs against Petitioner's conclusory assertions in this regard, which were discussed previously. *See, e.g.,* Ex. 2164, 71:9–73:17, 73:18–74:4, 24:6–22, 65:10–14, 129:7–9, 130:17–25, 134:20–25; Pet. 19– 20. Thus, considering the complex field of integrated circuit fabrication and taking into account the level of ordinary skill in that art as set forth by Petitioner, there is insufficient evidence of record to conclude that ordinary creativity would support a conclusion that one of ordinary skill in the art would have had expected success of substituting Leedy '695's dielectric material for Bertin '754's dielectric layer 60 and interconnect insulators. This is particularly true in view of the significant differences in the Leedy '695's membrane dielectric isolation process and Bertin '754's process using thermal oxidation and conventional, rigid substrates to fabricate integrated circuits.

3. Expert Testimony

In general, we weigh Dr. Glew's testimony concerning the reasons why one of ordinary skill in the art would not have reason to combine the references in the manner proposed by Petitioner more heavily than Dr. Franzon's declaration testimony that one of ordinary skill in the art would have done so and would have had a reasonable expectation of success.

Dr. Franzon's testimony, in large measure, is that Leedy '695 identifies advantages of "the disclosed dielectric deposition techniques (Ex.

1002 ¶ 110); that plasma-enhanced chemical vapor deposition was commonly available and was known to "advantageously provide" various benefits; and the references are in the same technological field and "address similar challenges relating to the stacking of integrated circuit devices." *See* Ex. 1002 ¶¶ 111, 114; Pet. 22–25 (citing Ex. 1002 ¶¶ 104–114, 124). Dr. Franzon's testimony, however does not adequately address why one of ordinary skill in the art would specifically use Leedy '695's fabrication process to make Bertin '754's integrated circuit having Leedy '695's low tensile stress dielectric as layer 60 and interconnect insulators, which is the combination on which Petitioner relies for the recited dielectric material characterized by the particular tensile stress claimed. *See id.*

Notably, too, Dr. Franzon does not specify or otherwise explain the "similar challenges relating to the stacking of integrated circuit devices" he refers to in his testimony. Ex. 1002 ¶ 114. We, however, recognize that "any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *KSR*, 550 U.S. at 420. Noting, however, that references are in the same general field and address similar unnamed challenges in the circumstances of this case—involving complex technology of integrated circuit fabrication, we conclude that Dr. Franzon's testimony about the benefits of Leedy '695's general process is insufficient to support Petitioner's position regarding dielectric substitution of particular structures in Bertin '754. *See In re Nuvasive*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) ("The factual inquiry whether to combine references must be thorough

and searching.")); *InTouch Techs., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014) ("While an analysis of any teaching, suggestion, or motivation to combine elements from different prior art references is useful in an obviousness analysis, the overall inquiry must be expansive and flexible.").

In contrast, Patent Owner relies on Dr. Glew's testimony, which is specific as to reasons why one of ordinary skill in the art would not have combined Leedy '695's fabrication process to make Bertin '754's integrated circuit having Leedy '695's low tensile stress dielectric as layer 60 and insulated interconnecting structures. Specifically, for example, Patent Owner relies on Dr. Glew's testimony that Bertin '754's "dielectric layer 60" was grown using thermal oxidation and could not be produced using plasma-enhanced chemical vapor deposition used by Leedy '695. PO Resp. 41–45. More specifically, Dr. Glew explains that, because Bertin '754's dielectric layer is *grown* as silicon dioxide (rather than deposited using a chemical vapor deposition process), one of ordinary skill in the art would understand that Bertin '754's dielectric layer 60 was produced "using thermal oxidation to grow exposed silicon components into silicon dioxide." PO Resp. 42–43 (citing Ex. 2166 ¶ 127 (Dr. Glew's testimony citing Ex. 1004, 3:60–62, Ex. 2158 (Zant text), 102–103).

In addition, Dr. Glew testifies that "because Bertin describes the silicon dioxide dielectric layer 60 as being grown directly over active silicon components (such as a silicon source, gate, or drain), one of ordinary skill also would understand that the dielectric layer 60 needs to be highly pure, which again would mean it was grown at high temperatures using thermal oxidation." PO Resp. 43 (citing Ex. 2166 ¶ 128; Ex. 1004, 3:60–4:3; Ex.

2158, 68–70; Ex. 2159, 54, 139). Dr. Glew further testified that one of ordinary skill in the art would understand that Bertin '754's dielectric layer 60 could not be deposited using plasma-enhanced chemical vapor deposition described by Leedy '695 "because the resulting dielectric would not (1) be sufficiently pure; (2) have the ability to adhere sufficiently to the semiconductor wafer; and (3) be able to withstand high temperatures of the remaining . . . steps[17] without changing its form." Ex. 2166 ¶ 130 (citing Ex. 2169, 29–30). Notably, Dr. Glew testifies that plasma-enhanced chemical vapor deposition (a known technique used by Leedy '695) cannot be used with Bertin '754's techniques because "positive ions present in the plasma can strike and damage the wafer and the exposed active components in and on its surface." Ex. 2166 ¶ 130 (citing Ex. 2159, 139).

Furthermore, Dr. Glew's testimony is supported by his well-reasoned explanation, citations to background references and asserted prior art. For example, Dr. Glew's declaration testimony cites three pages of the Zant text (Ex. 2158) and a page of the Runyan text (Ex. 2159) to support his statement that "if a silicon dioxide dielectric contacts circuit components, the silicon dioxide must be high-purity to not damage the circuit components." Ex. 2166 ¶ 128 (citing Ex. 2158, 68–70; Ex. 2159, 54). That statement, supported by two reference citations, in turn, supports Dr. Glew's conclusion: "[t]herefore, because Bertin describes the silicon dioxide

[17] Petitioner and Patent Owner dispute what is meant by front-end and back-end processing steps, we are not persuaded that resolving this issue is necessary to determine whether a skilled artisan would have had reason to combine the asserted references in the manner proposed by Petitioner to arrive at the claimed invention, and whether one of ordinary skill in the art would have had a reasonable expectation of success of doing so.

dielectric layer 60 as being grown directly over active silicon components (such as a silicon source, gate, or drain), one of ordinary skill also would understand that the dielectric layer 60 needs to be highly pure, which again would mean it was grown at high temperatures using thermal oxidation." Ex. 2166 ¶ 128.

We also note the absence of further declaration testimony by Dr. Franzon opposing Dr. Glew's position or otherwise supporting Petitioner's Reply to Patent Owner's Response. For the reasons noted previously, because of the complexity of integrated circuit fabrication, expert testimony is critical to explaining why one of ordinary skill in the art would have had a reason to combine the references as the claims require. *Kinetic Concepts,* 688 F.3d at 1369. This is particularly true in view of Dr. Glew's well-reasoned and supported testimony. Petitioner's attorney-argument in its Reply consists of conclusory statements with insufficiently explained citations to Leedy '695 and other references and is insufficient to establish that one of ordinary skill in the art would have had reason to combine the references in the manner proposed by Petitioner. *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (a petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements").

For example, in Reply to Dr. Glew's testimony supporting Patent Owner Response, Petitioner's attorneys assert that plasma-enhanced chemical vapor deposition dielectrics are compatible with silicon substrates and high temperature processes. Reply 11–16 (citing Ex. 1082, 1006, 1088)). We recognize that sometimes expert testimony is not always necessary. *See, e.g., Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688

F.3d 1342, 1369 (Fed. Cir. 2012) (indicating expert technology is not always required) (citing *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1240 n.5 (Fed. Cir. 2010) ("However, as we [have] noted . . . 'expert testimony regarding matters beyond the comprehension of layperson is sometimes essential,' particularly in cases involving complex technology. In such cases, expert testimony may be critical, for example, to establish . . . the existence (or lack thereof) of a motivation to combine references." (internal citations omitted)) (alteration in original)). Accordingly, because of the complexity of integrated circuit fabrication discussed above, however, attorney-argument addressing Dr. Glew's well-reasoned and supported testimony does not persuade us that one of ordinary skill in the art would have had reason to combine the references in the manner proposed by Petitioner or would have had a reasonable expectation of success.

4. Conclusion

As described above, Petitioner in its Petition made arguments as to why one of ordinary skill in the art would have been motivated to combine Bertin '754, Poole, and Leedy '695 to achieve the purported claimed invention, and why a skilled artisan would have had a reasonable expectation of success. Patent Owner provided well-reasoned arguments based on testimonial evidence, background references, and prior art references identifying shortcomings in Petitioner's position. There is evidence from both sides regarding the presence or absence of a reason to combine Bertin '754 and Leedy '695 in the manner proposed by Petitioner to arrive at the claimed invention and regarding whether one of ordinary skill in the art would have had a reasonable expectation of success.

Here, Petitioner has the burden to show, by a preponderance of the evidence, a reason why one of ordinary skill in the art would have combined the prior art references to arrive at the invention and why one of ordinary skill in the art would have had a reasonable expectation of success of combining the references to meet the limitations of the claimed invention. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) ("The reasonable expectation of success requirement refers to the likelihood of success in combining the references to meet the limitations of the claimed invention. . . . [O]ne must have a motivation to combine [the references] accompanied by a reasonable expectation of achieving what is claimed in the patent-at-issue."). "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")).

It is well-settled that identifying a reason to combine references is not confined to a "rigid or mandatory formula[]." *KSR*, 550 U.S. at 419; *see In re Nuvasive*, 842 F.3d 1376, 1383(Fed. Cir. 2016). Moreover, "[w]hile an analysis of any teaching, suggestion, or motivation to combine elements from different prior art references is useful in an obviousness analysis, the overall inquiry must be expansive and flexible." *InTouch Techs., Inc. v. VGO Commc'ns, Inc.*, 751 F.3d 1327, 1347 (Fed. Cir. 2014).

Furthermore, the inquiry cannot be met by conclusory statements but rather must be "thorough and searching." *See In re Nuvasive,* 842 F.3d

1376, 1383 (Fed. Cir. 2016) (holding conclusory statements insufficient if not supported by a reasoned explanation) (citing *In re Lee*, 277 F.3d 1338, 1342 (Fed. Cir. 2002) ("The factual inquiry whether to combine references must be thorough and searching.")). Additionally, we must be careful not to allow hindsight reconstruction of references to reach the claimed invention without adequate explanation as to how or why the references would be combined to produce the claimed invention. *See, e.g., Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1368 (Fed. Cir. 2012) (quoting *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 n.3 ("We must still be careful not to allow hindsight reconstruction of the references to reach the claimed invention without any explanation as to how or why the references would be combined to produce the claimed invention.")).

We find Petitioner's arguments regarding its proposed combination to be incomplete. In the context of these cases, it is insufficient to propose incorporating "the material" of Leedy '695 without providing sufficient detail as to the combined process to produce the claimed combination. We recognize that it is axiomatic that bodily incorporation is not required. *See, e.g., In re Mouttet,* 686 F.3d 1322, 1332 (Fed. Cir. 2012) ("It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of the elements."). To be clear, we are not suggesting that Petitioner must explain how Leedy '695's entire membrane dielectric isolation process would or could be included with Bertin '754's integrated circuit fabrication process. Rather, we find Petitioner's explanation to be incomplete because it does not adequately explain how Bertin '754's fabrication process would be changed to use Leedy '695's dielectric material, which is formed in quite different a

manner than Bertin ’754’s dielectric layer 60. This is necessary, at least, to support a conclusion that one of ordinary skill in the art would have had reasonable expectation of success of using Leedy ’695’s dielectric material in place of Bertin ’754’s layer 60 and interconnect insulators.

For these reasons above, we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 1–3, 30, 31, 33, 40, 41, and 44 would have been unpatentable over the asserted combination of Bertin ’754, Poole, and Leedy ’695. In particular, we determine that Petitioner has not met its burden in demonstrating by a preponderance of the evidence that: (1) the proposed combination of Bertin ’754, Poole, and Leedy ’695 would have conveyed to one of ordinary skill in the art the “substantially flexible semiconductor substrate” or “substantially flexible” integrated circuit/circuit substrate as recited in the challenged claims; and (2) a person of ordinary skill in the art would have had reason to combine the asserted references to arrive at the claimed invention, or that a person of ordinary skill would have had a reasonable expectation of success in achieving the combination proposed by Petitioner.

4. Claims 1 and 44 – Obvious over Bertin ’754 and Poole

i. Analysis

Petitioner argues that independent claim 1 and dependent claim 44 are unpatentable over the combination of Bertin ’754 and Poole under 35 U.S.C. § 103(a). Pet. 58. For this challenge, Petitioner takes the position that under a broader construction of “substantially flexible semiconductor substrate/integrated circuit/circuit substrate,” claims 1 and 44 are unpatentable for the same reasons presented for the asserted combination of

Bertin ’754, Poole, and Leedy ’695. Petitioner adds that if “substantially flexible integrated circuit/circuit substrate” is construed to mean “an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of 150 μm or less,” then Leedy ’695 is not required in combination with Bertin ’754 and Poole for claims 1 and 44, which would then not require a low stress dielectric. *Id.* at 58.

Based on the complete record, including our construction of “substantially flexible semiconductor substrate” and “substantially flexible integrated circuit,” we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 1 and 44 are unpatentable over Bertin ’754 and Poole. As discussed above, independent claim 1 and dependent claim 44 require a “substantially flexible” semiconductor substrate and integrated circuit. For these limitations, Petitioner relies on the same arguments based on thinness for the proposed alternative claim construction. Pet. 58. For the same reasons discussed above, we determine Petitioner has not demonstrated by a preponderance of the evidence that Bertin ’754 and Leedy ’695 teaches these features.

5. *Claims 1–3, 30, 31, 33, 40, 41, and 44 – Obvious over Hsu and Leedy ’695*

i. Hsu (Ex. 1008)

Hsu relates generally to a “method of connecting three-dimensional integrated circuit chips using trench technology.” Ex. 1008 at Abstract, 1:8–11. Referring to Figures 2–8, Hsu’s fabrication process starts with etching deep trenches 16 on silicon substrate 10, which Hsu indicates can be composed of monocrystalline silicon. *Id.* at 2:50–61. According Hsu, the master chip and subordinate chip each consist of a semiconductor substrate,

preferably composed of monocrystalline silicon. *Id.* at 2:51–54, 3:42–45. These chips can be "stacked by interconnection through [a] pad window . . . during integrated circuit processing." *Id.* at 1:28–31. Hsu further describes that the "bottom surface of the [subordinate] substrate is ground and polished so that only a thin portion of the substrate remains." *Id.* at 3:21–23.

ii. Analysis

Petitioner argues that claims 1–3, 30, 31, 33, 40, 41, and 44 are obvious over the combination of Hsu and Leedy '695. *See* Pet. 3, 43–56. For this challenge, Petitioner argues that

> Hsu discloses stacked chips each having a "silicon dioxide film 18 . . . formed on the entire surface of the substrate" including on the vertical walls of Hsu's vertical interconnects (Ex. 1008 at 2:63-67, Figs. 2-7), but does not explicitly disclose that the dielectric layer 18 constitutes a "low stress" dielectric characterized by a tensile stress of about 5×10^8 dynes/cm^2 or less, as recited in the challenged claims.

Pet. 43–44.

Additionally, with respect to independent claim 1, Petitioner asserts that Hsu discloses a master chip with semiconductor substrate 40 (e.g., circuit substrate) and an integrated circuit subordinate chip (first integrated circuit) with semiconductor substrate 10, where the back surface of the subordinate chip is bonded to the front surface of the master chip. Pet. 48–49 (citing Ex. 1003, 3:41–4:2, Figs. 10–12). Petitioner further argues that Hsu discloses its process of fabricating and bonding the master chip and the subordinate chip, shown in Figures 2–10, can be used to connect "another subordinate chip" to the integrated circuit chip illustrated in Figure 12. *Id.* at 50 (citing Ex. 1008, 4:7–14).

With respect to the "substantially flexible semiconductor substrate"

recited in claim 1, Petitioner argues that Hsu teaches that substrate 10 is "preferably composed of monocrystalline" and "is ground and polished so that only a thin portion of the substrate remains over trenches 20, which have a depth of more than about 10 microns." Pet. 50 (Ex. 1008, 2:51–54, 2:60–63). Petitioner contends that because "more than about 10 microns" includes a thickness of less than 50 μm (*i.e.*, everything between more than about 10 μm and less than 50 μm), *Hsu* teaches or suggests that the semiconductor substrate 10 is substantially flexible because it is thinned to a thickness of less than 50 μm and subsequently polished. *Id.* at 50–51.

Petitioner further argues that Leedy '695 similarly teaches or suggests a substantially flexible substrate, as construed by Petitioner, by disclosing a single crystal semiconductor layer which is "etched or polished away" to form a semiconductor layer having a thickness of less than 50 μm (*e.g.*, 2 μm). Pet. 51 (citing Ex. 1006, Abstract, 2:56–60, 5:24–32, 5:41–68).

For a "substantially flexible" integrated circuit, Petitioner asserts that the combination of Hsu and Leedy '695 teaches or suggests a substantially flexible integrated circuit, "as construed by Petitioner, because the combination teaches or suggests a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed, and that dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm^2 tensile or less." Pet. 51.

Again, Petitioner's arguments regarding the "substantially flexible" limitations recited in claim 1 are premised on a proposed construction of "substantially flexible" that we have not adopted. *See supra* Section II.A.1. As discussed above with respect to Petitioner's challenges based on Bertin '754, Poole, and Leedy '695, we are not persuaded that thinning or thinness

is the same as flexibility. Moreover, also discussed above, Petitioner has not sufficiently explained otherwise how the asserted combination teaches "substantially flexible" semiconductor substrate or integrated circuit. See *generally Reply*.

Additionally, we are not persuaded that Petitioner has articulated reasoning with some rational underpinning to support its obviousness challenge based on the substitution of Hsu's dielectric 18 with Leedy '695's low stress dielectric. *See* Pet. 43–47. Petitioner relies on many of the same arguments discussed with regard to Petitioner's challenge based on Bertin '754, Poole, and Leedy '695, including that Hsu and Leedy '695 are both directed to improvement of integrated circuits; and Leedy '695 provides express motivations to incorporate its low stress dielectric into Hsu structure. Pet. 44–45 (citing Ex. 1006, 1:53–62, 2:9–31, 2:66–3:3, 3:56–4:13, 5:63–6:5, 11:33–37, 30:36–42, 45:49–46:26, 46:52–47:33, Figs. 32a–32d; Ex. 1002 ¶¶ 109–114).

Based on the complete record, for the same reasons discussed above, we are not persuaded by Petitioner's arguments. First, as discussed above, the fact that Hsu and Leedy '695 are directed to similar technology, or even that one of ordinary skill in the art was aware of the references, does not in itself establish that one of ordinary skill in the art *would* have replaced Hsu's dielectric 18 with Leedy '695's low stress dielectric. Further, in the complicated technology field of integrated circuit fabrication, Dr. Franzon's testimony in paragraph 114 is too general in asserting the reason of "they are in the same technological field of three-dimensional integration and address similar challenges relating to the stacking of integrated circuit devices" without discussing, for instance, what particular challenges are addressed.

Ex. 1002 ¶ 114. Although Dr. Franzon lists a string of citations, he does not explain or otherwise reference those citations. We find Petitioner's contention here to be insufficient for substantially similar reasons we found parallel arguments to be insufficient with regard to Bertin '754 and Leedy '695.

Second, while we agree that Leedy '695 may disclose advantages of its described MDI fabrication process and low stress dielectric membrane, Petitioner has not explained how these purported benefits apply to Hsu's dielectric 18, or, why one of ordinary skill in the art would have been motivated by these advantages to replace that specific dielectric 18 in Hsu's structure. In other words, Petitioner does not explain sufficiently why or how the importance of low tensile stress for Leedy '695's process for constructing low tensile stress dielectric membranes bears on why one of ordinary skill in the art would have substituted Leedy '695's dielectric material for Hsu's layer 18. Moreover, as discussed in detail previously, Petitioner characterizes Leedy '695's teaching to be about low tensile stress dielectrics. The citations by Petitioner, however, discuss advantages of its low tensile stress dielectric flexible membrane or its membrane dielectric isolation fabrication techniques. Here, too, the probative value of Petitioner's argument is diminished because Petitioner credits Leedy '695's low tensile stress dielectric material with the benefits disclosed by Leedy '695 for its membrane dielectric isolation process for fabricating integrated circuits.

Petitioner further asserts that "considerable similarities between Leedy '695 and Hsu's teachings . . . indicate that those of skill in the art were aware of the use of silicon dioxide dielectric layers and their placement

over silicon substrates in the fabrication of integrated circuits." Pet. 47. Petitioner argues that Leedy '695's well-known PECVD process "***could*** have been used in place of the techniques for growing dielectrics described in Bertin to obtain the predictable result of stacked integrated circuits having low tensile stress dielectrics." Pet. 46 (emphasis added).

Again, Petitioner argues that the similarities between Leedy '695 and Hsu indicate that a skilled artisan ***could*** have substituted one dielectric for another, or one process for another. However, we are not persuaded that could have combined the references is sufficient to demonstrate that one of ordinary skill in the art would have had a reason to do so.

Further, we observe that Dr. Franzon's testimony that different chemical vapor deposition methods result in different dielectric properties weighs against Petitioner's argument that one dielectric deposition process is easily interchangeable with another process. Ex. 2164, 69:3–19. The cited portion of Dr. Franzon's testimony (Ex. 1002 ¶¶ 104–114) does not discuss Hsu's use of APVCD, the implications of Hsu's disclosure on one of ordinary skill in the art's awareness of using use of silicon dioxide dielectric layers, or a purported motivation to look to other references as Petitioner contends. As discussed previously, in this complex technology area of integrated circuit fabrication, expert testimony is critical. *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1369 (Fed. Cir. 2012) (indicating expert technology is not always required) (citing *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1240 n.5 (Fed. Cir. 2010) ("However, as we [have] noted . . . 'expert testimony regarding matters beyond the comprehension of layperson is sometimes essential,' particularly in cases involving complex technology. In such cases, expert testimony may be critical, for example, to

establish . . . the extistence (or lack thereof) of a motivation to combine references." (internal citations omitted)) (alteration in original)). Thus, we find Petitioner's contention to have minimal probative value.

In addition, Petitioner's reasoning that the similarity of the references "constitutes a motivation to look to other references" seems inadequate on its face. Even if true, that statement does not provide a reason would pick out these particular references and combine them to arrive at the claimed invention. *Cf. Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993–94 (Fed. Cir. 2017) (concluding "that reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they could be combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention (citing *Belden Inc. v. Berk–Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention."))).

Similarly, in view of the complex technology involved in integrated circuit fabrication and, particularly and the agreement of both experts that dielectrics have different properties and different methods of forming dielectrics in integrated circuit fabrication result in dielectrics having different properties (as discussed previously), we determine that Petitioner's contentions and Dr. Franzon's broad conclusions (Pet. 45–47; Ex. 1002 ¶¶ 104–114) of success to be insufficient to meet its burden, which requires a preponderance of evidence. For example, as discussed previously, we find Petitioner's contention that "Leedy '695 thus discloses that its dielectrics

can be easily used in place of other dielectrics" to be insufficiently supported by the evidence of record.

Accordingly, for these, we determine Petitioner has not demonstrated by a preponderance of the evidence that Hsu in combination with Leedy '695 teaches these features.

6. Claims 1 and 44 – Obvious over Hsu

i. Analysis

Petitioner argues that independent claim 1 and dependent claim 44 are unpatentable over the combination of Hsu and Poole under 35 U.S.C. § 103(a). Pet. 58. For this challenge, Petitioner takes the position that under a broader construction of "substantially flexible semiconductor substrate/integrated circuit/circuit substrate," claims 1 and 44 are unpatentable for the same reasons presented for the asserted combination of Hsu and Leedy '695. *Id.* Petitioner adds that if "substantially flexible integrated circuit/circuit substrate" is construed to mean "an integrated circuit [circuit substrate] having a semiconductor substrate that has been thinned to a thickness of 150 μm or less," then Leedy '695 is not required in combination with Hsu for claims 1 and 44 because a low stress dielectric is not part of the construction. *Id.* at 58.

Based on the complete record, including our construction of "substantially flexible semiconductor substrate" and "substantially flexible integrated circuit," we determine that Petitioner has not demonstrated by a preponderance of the evidence that claims 1 and 44 are unpatentable over Hsu. As discussed above, independent claim 1 and dependent claim 44 require a "substantially flexible" semiconductor substrate and integrated circuit. For these limitations, Petitioner relies on the same arguments based

on thinness discussed above (e.g., challenges based on Hsu and Leedy '695 and Bertin '754, Poole, and Leedy '695), which we have determined are not sufficient to satisfy Petitioner's burden. Pet. 58. For the same reasons discussed above, we determine Petitioner has not demonstrated by a preponderance of the evidence that Hsu alone teaches these features.

III. CONCLUSION

We conclude, based on a preponderance of the evidence, that Petitioner has not established that claims 1–3, 30, 31, 33, 40, 41, and 44 of the '542 patent are unpatentable.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–3, 30, 31, 33, 40, 41, and 44 of the '542 patent have not been shown by a preponderance of the evidence to be unpatentable; and

FURTHER ORDERED that this is a Final Written Decision under 35 U.S.C. § 318(a), and that parties to the proceeding seeking judicial review of the decision under 35 U.S.C. § 319 must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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