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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX, INC.,
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00390
Patent 8,629,542 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and FRANCES L. IPPOLITO, *Administrative Patent Judges*.

IPPOLITO, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively "Petitioner") filed a Petition on December 28, 2015, requesting an *inter partes* review of claims 1–3, 30, 31, 33, 40, 41, and 44 of U.S. Patent No. 8,629,542 B2 (Ex. 1001, "the 542 patent"). (Paper 4, "Pet."). Patent Owner, Elm 3DS Innovations, LLC, filed a Preliminary Response to the Petition on April 6, 2016 (Paper 10, "Prelim. Resp.").

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

Upon consideration of the information presented in the Petition and Preliminary Response, and for the reasons explained below, we determine that Petitioner has demonstrated that there is a reasonable likelihood that the challenged claims 1–3, 30, 31, 33, 40, 41, and 44 of the '542 patent are unpatentable. Accordingly, we institute an *inter partes* review of claims 1–3, 30, 31, 33, 40, 41, and 44 of the '542 patent based on the grounds identified in the Order section of this decision.

A. Related Proceedings

Petitioner indicates that the '542 patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

Additionally, patents related to the '542 patent are also the subjects of petitions filed in IPR2016-00386 (US Patent No. 8,653,672); IPR2016-00387 (US Patent No. 8,841,778); IPR2016-00388 and IPR2016-00393 (US Patent No. 7,193,239); IPR2016-00389 (US Patent No. 8,035,542); IPR2016-00391 (US Patent No. 8,796,862); IPR2016-00394 (US Patent No. 8,410,617); IPR2016-00395 (US Patent No. 7,504,732); IPR2016-00687 (US Patent No. 8,928,119); IPR2016-00691 (US Patent No. 7,474,004); IPR2016-00703 (US Patent No. 8,791,581); IPR 2016-00706 (US Patent No. 8,791,581); IPR 2016-00786 (US Patent No. 8,933,570); IPR 2016-00708 (US Patent No. 8,907,499); and IPR 2016-00770 (US Patent No. 8,907,499).

B. Time Bar under 35 U.S.C. § 315(b)

Patent Owner argues that Petitioner is time-barred under 35 U.S.C. § 315(b) because two of the real-parties-in-interest, Samsung Austin Semiconductor LLC ("SAS") and Samsung Semiconductor Inc. ("SSI") were served with a complaint alleging infringement of the '542 patent on December 24, 2014. Prelim. Resp. 5–10. Patent Owner contends that the Petition was filed on December 28, 2015, which was four days after the statutory one year period for SAS and SSI had expired. *Id.*

In the Petition, Petitioner explained that it filed its Petition on December 28, 2015, because the Office considered December 22–24, 2015, to be a "Federal holiday within the District of Columbia" pursuant to 35 U.S.C. § 21. Pet. 3 n.2. On December 22, 2015, the Office experienced a major power outage at its headquarters in Alexandria, Virginia, resulting in damaged equipment that required the subsequent shutdown of many USPTO online and information technology systems. On December 28, 2015, the Office announced that

> [i]n light of this ***emergency situation***, the USPTO will consider each day from Tuesday, December 22, 2015, through Thursday, December 24, 2015, to be a "Federal holiday within the District of Columbia" under 35 U.S.C. § 21 and 37 C.F.R. §§ 1.6, 1.7, 1.9, 2.2(d), 2.195, and 2.196. Any action or fee due on these days will be considered as timely for the purposes of, e.g., 15 U.S.C. §§ 1051(b), 1058, 1059, 1062(b), 1063, 1064, and 1126(d), or 35 U.S.C. §§ 119, 120, 133, and 151, if the action is taken, or the fee paid, on the next succeeding business day on which the USPTO is open (37 C.F.R. §§ 1.7(a) and 2.196).

Ex. 3001 (emphasis added). Section 21(b) states that "[w]hen the day, or the last day, for taking any action or paying any fee in the United States Patent and Trademark Office falls on Saturday, Sunday, or a federal holiday within the District of Columbia, ***the action may be taken, or the fee paid, on the next succeeding secular or business day***" (Emphasis added). Thus, we are persuaded that Petitioner complied with the requirements of section 315(b) given the circumstances of the power outage during the December 22–24, 2015 time-frame and the announcements by the Office regarding the same. December 28, 2015 was the next succeeding business day after December 24, 2015. Moreover, we disagree with Patent Owner's arguments that the Office lacks the authority to treat December 22–24, 2015 as federal holidays. *See* Prelim. Resp. 7–8.

C. The '542 Patent

The '542 patent is directed generally to a "three-dimensional structure (3DS)" for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1*a* is reproduced below.

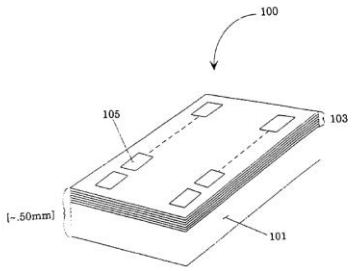


Figure 1a

Figure 1*a* shows 3DS memory device 100 having a stack of integrated circuit layers with a "fine-grain inter-layer vertical interconnect" between all circuit layers. *Id.* at 4:10–13. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:30–32. The '542 patent discloses that "each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 µm and typically less than 10 µm in thickness." *Id.* at 4:35–37. The '542 patent further discloses that the "thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication." *Id.* at 8:58–63.

Figure 1*b* is reproduced below.

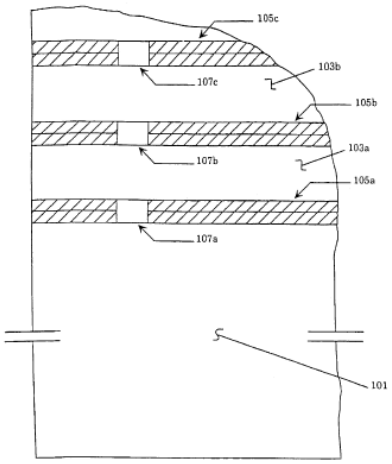


Figure 1b

Referring to Figure 1*b*, the ’542 patent shows a cross-section of a 3DS DRAM integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:51–53. Bond and interconnect layers 105a, 105b, etc. are shown between circuit layers 103a and 103b. *Id.* at Fig. 1*b*. The ’542 patent discloses that pattern 107a, 107b, etc. in the bond and interconnect layers 105a, 105b, etc. defines the vertical interconnect contacts between the integrated circuit layers and serves to electrically isolate these contacts from each other and the remaining bond material. *Id.* at 4:24–28. Additionally, the ’542 patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:29–29.

Further, the ’542 patent teaches that the “term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 µm.” *Id.* at 4:14–17. The fine-grain inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:18–20.

D. Illustrative Claim

Of the challenged claims, claim 1 (reproduced below) is independent and illustrative of the subject matter of the '542 patent:

> 1. A stacked integrated circuit comprising:
>
> a circuit substrate;
>
> a first integrated circuit having circuitry formed on a front surface thereof, the front surface or a back surface being bonded to the circuit substrate; and
>
> one or more additional integrated circuits each having circuitry formed on respective front surfaces thereof, each additional integrated circuit having the front surface or a back surface thereof adjacent to the front surface or a back surface of an adjacent integrated circuit;
>
> wherein at least one of the first integrated circuit and the one or more additional integrated circuits is substantially flexible and comprises a substantially flexible semiconductor substrate of one piece made from a semiconductor wafer thinned by at least one of abrasion, etching and parting, and subsequently polished to form a polished surface.

E. The Asserted Grounds

Petitioner asserts that the challenged claims are unpatentable on the following grounds (Pet. 3):

Reference(s)	Basis	Claim(s) Challenged
Bertin[1], Poole[2], and Leedy[3]	§ 103	1–3, 30, 31, 33, 40, 41, and 44
Hsu[4] and Leedy	§ 103	1–3, 30, 31, 33, 40, 41, and 44

[1] US Patent No. 5,202,754, issued April 13, 1993 (Ex. 1004, "Bertin").
[2] US Patent No. 5,162,251, issued Nov. 10, 1992 (Ex. 1005, "Poole").
[3] US Patent No. 5,354,695, issued Oct. 11, 1994 (Ex. 1006, "Leedy").
[4] US Patent No. 5,627,106, issued May 6, 1997 (Ex. 1008, "Hsu").

Reference(s)	Basis	Claim(s) Challenged
Hsu and Kowa[5]	§ 103	1–3, 30, 31, 33, 40, 41, and 44
Bertin and Poole	§ 103	1 and 44
Hsu	§ 103	1 and 44

II. ANALYSIS

A. Claim Construction

We interpret claims of an unexpired patent using the "broadest reasonable construction in light of the specification of the patent in which [the claims] appear[]." 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee,* No. 15-446, slip op. at 9 (U.S. June 20, 2016) (concluding the broadest reasonable construction "regulation represents a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office"). The Board, however, may not "construe claims during IPR so broadly that its constructions are unreasonable under general claim construction principles. . . . '[T]he protocol of giving claims their broadest reasonable interpretation . . . does not include giving claims a legally incorrect interpretation.'" *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2016). "Rather, 'claims should always be read in light of the specification and teaching in the underlying patent'" and "[e]ven under the broadest reasonable interpretation, the Board's construction

[5] JP Patent Application Publication No. H3-151637, published June 27, 1991 (Ex. 1007, "Kowa"). Petitioner has provided a certified English translation. Ex. 1007, 13.

'cannot be divorced from the specification and the record evidence.'" *Id.* (citations omitted).

Petitioner asks that we construe "substantially flexible" as a modifier for each of "semiconductor substrate" and "integrated circuit." Pet. 9−17. Patent Owner takes the position that these Petitioner-requested constructions are irrelevant to this proceeding, indicating that Petitioner has acknowledged that these claim terms are not determinative in this case. Prelim. Resp. 15.

For purposes of this decision, we preliminarily construe "low stress dielectric" and "substantially flexible semiconductor substrate."

1. "substantially flexible semiconductor substrate" (claim 1)

The term "substantially flexible semiconductor substrate" is a term of degree that lacks clear meaning absent context. *See Playtex Prods., Inc. v. Procter & Gamble Co.*, 400 F.3d 901, 908 (Fed. Cir. 2005) ("'Substantially flattened surface' is clearly a comparative term. Comparison requires a reference point. Therefore, to flatten something, one must flatten it with respect to either itself or some other object.").

Petitioner urges that in light of the intrinsic record, the broadest reasonable construction of "substantially flexible" when used to modify "semiconductor substrate" is "a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed." Pet. 10.

Petitioner argues that Patent Owner acted as its own lexicographer in defining "substantially flexible" when used to describe how to make a semiconductor substrate:

> Grind the backside or exposed surface of the second circuit substrate to a thickness of less than 50 μm and then polish or

> smooth the surface. The thinned substrate is now a substantially flexible substrate.

Id. (citing Ex. 1001, 9:16–19; *see also id.* at 3:18–21, 4:35–37).

Petitioner further argues that Patent Owner (then, Applicant) confirmed this definition during prosecution of related patents and applications. For example, during prosecution of related U.S. Patent No. 8,907,499 ("the '499 patent"), the Examiner objected to certain claims for including the term "substantially flexible" as indefinite. Pet. 11 (citing Ex. 1018, 4). Petitioner notes that Applicant overcame the objection by arguing that "substantially flexible" is unambiguous because it is "clearly explained in the specification." *Id.* at 10–11 (citing Ex. 1019, 9; *see also* Ex. 1020 at 18:1–3). Thus, according to Petitioner, Applicant clearly and unmistakably set forth a definition of the term "substantially flexible" when used to modify semiconductor substrate and expressed an intent to define the term. *Id.* at 12.

Looking to the Specification, we note that the Summary of the Invention section in the '542 patent does not limit the meaning of a "substantially flexible" substrate to those substrates that have been polished. In particular, the '542 patent teaches that "*[t]hinning of the memory circuit to less than about 50 µm in thickness forming a substantially flexible substrate* with planar processed bond surfaces and bonding the circuit to the circuit stack while still in wafer substrate form . . . ." Ex. 1001, 3:18–21 (emphasis added). In other words, polishing is not required for "forming a substantially flexible substrate." *Id.* Moreover, we note that claim 1 recites "a substantially flexible semiconductor substrate of one piece made from a semiconductor wafer thinned . . . , and subsequently *polished to form a*

polished surface." Emphasis added. Thus, a construction of "substantially flexible semiconductor substrate" that includes polishing would effectively read "and subsequently polished to form a polished surface" out of claim 1. *See also Stumbo v. Eastman Outdoors, Inc.*, 508 F.3d 1358, 1362 (Fed. Cir. 2007) (rejecting claim constructions that render phrases in claims superfluous). Thus, given the claim language and statements in the Specification and the prosecution history for a related patent, we preliminarily construe "substantially flexible semiconductor substrate" as "a semiconductor substrate that has been thinned to a thickness of less than 50 μm." *Cf. Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015) ("The PTO should also consult the patent's prosecution history in proceedings in which the patent has been brought back to the agency for a second review.").

Claim constructions may change as a result of the record developing during trial. We note, for example, that Patent Owner has not yet filed its response under 37 C.F.R. § 42.120 or any new testimonial evidence.

2. "low stress dielectric" (claim 2)

The parties do not propose express constructions for the term "low stress dielectric." Pet. 9–17; Prelim. Resp. 15–16. Nonetheless, Petitioner presents separate theories of unpatentability based on alternative constructions of the term "low stress dielectric." Pet. 36 n.10, 57–58. Specifically, Petitioner argues that for its challenges based on Leedy, the recited "low stress dielectric" must be disclosed by Leedy because Patent Owner relied on Leedy "as specific support for these limitations (*e.g.*, Ex. 1001, 8:63–66), whatever is meant by those limitations is *per se* disclosed in prior art under 35 U.S.C. § 102(b)." *Id.* at 36 n.10. Separately, Petitioner's

obviousness challenge based on Kowa, relies on a different construction of "low stress dielectric" that requires stress-balancing multiple dielectrics. *Id.* at 58. However, Petitioner expressly disavows such a construction and relies on Patent Owner to propose and support this position. Prelim. Resp. 57–58. Patent Owner does not present these claim construction arguments in its Preliminary Response. Prelim. Resp. 15–16.

At the outset, we note that 37 C.F.R. § 104(b)(3) requires that the ***Petition***, not the Patent Owner's preliminary response or response, set forth "[h]ow the challenged claim is to be construed." Thus, it is Petitioner's burden to establish in the Petition, its proposed construction(s) and accompanying support for any claim construction necessary to its challenges. Petitioner, not Patent Owner, must provide the basis for those proposed constructions in the Petition.

Based on the current record, Petitioner has identified portions of the Specification that provide some guidance on the meaning of "low stress dielectric," which we understand to be a term of degree. While it is permissible to use terms of degree (e.g., "low") in patent claims, the patent specification must provide a standard for measuring that degree. *Enzo Biochem, Inc. v. Applera Corp.*, 599 F.3d 1325, 1332 (Fed. Cir. 2010); *Seattle Box Co., Inc. v. Indus. Crating & Packing, Inc.*, 731 F.2d 818, 826 (Fed. Cir. 1984).

Here, the Specification teaches that dielectrics in low stress include those that have a stress of less than 5×10^8 dynes/cm^2 and "low stress dielectrics discussed at length in U.S. Pat. No. 5,354,695." Ex. 1001, 8:60–9:2. Looking to the disclosure of Leedy, US Patent No. 5,354,695, the reference teaches "[l]ow stress is defined relative to the silicon dioxide and

silicon nitride deposition made with the Novellus equipment as being *less than 8 x 10^8 dynes/cm^2 (preferably 1 x 10^7 dynes/cm^2) in tension*." Ex. 1006, 11:33–37 (emphasis added).

Additionally, the '542 patent compares the use of "intrinsically low stress deposited films," such as those disclosed in Leedy, to an alternative method of achieving net low stress through balancing the stress of "dielectrics with *conventional stress levels*." Ex. 1001, 8:66–9:11 (emphasis added). In other words, dielectrics that are not "intrinsically low stress" may be deposited to achieve the effect of a "net balanced lower stress," which results from the use of the "intrinsically low stress" dielectrics. *Id.* The Specification therefore distinguishes "low stress dielectrics" (e.g., having less than 8 x 10^8 dynes/cm^2 stress) from dielectrics with "conventional stress levels" that must be stress-balanced to achieve a net lower stress.

Based on this disclosure, and the current record, we interpret "low stress dielectric" to mean a dielectric having a stress of less than 8 x 10^8 dynes/cm^2. We, further, do not construe the term "low stress dielectric" to require the stress-balancing of multiple dielectrics because the Specification of the '542 patent has distinguished "low stress dielectrics" from those of "conventional stress levels" that require stress-balancing to achieve a similar result. *Id.*

B. Claims 1–3, 30, 31, 33, 40, 41, and 44 – Obvious over Bertin, Poole, and Leedy

1. Bertin (Ex. 1006)

Bertin relates generally to "[a] fabrication method and resultant three-dimensional multichip package having a densely stacked array of semiconductor chips." Ex. 1004 at Abstract. Figure 3a is reproduced below.

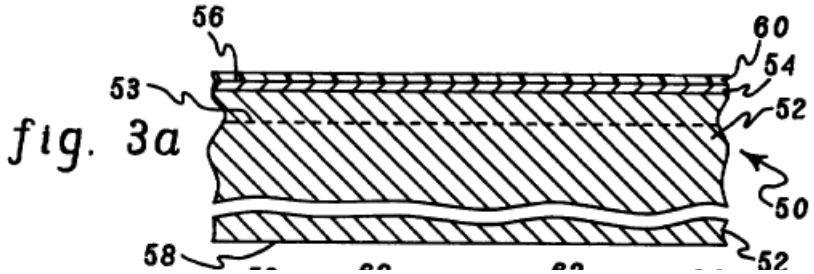


fig. 3a

Figure 3a depicts semiconductor device 50 having substrate 52 and active layer 54. Ex. 1004, 3:50–52. Layer 54 is adjacent to a first, upper planar surface 56 of device 50. *Id.* at 3:57–58. A second, lower planar surface 58 of device 50 is positioned substantially parallel to first planar surface 56. *Id.* at 3:59–60. Each stacked chip 50 includes a semiconductor "substrate 52" (*id.* at 3:50–4:3), which is thinned to 20 μm or less (*id.* at 3:25–46, 5:10–22). Bertin further teaches that "dielectric layer 60, for example, SiO_2, is grown over active layer 54 of device 50." *Id.* at 3:60–62, Fig. 3a.

Figure 2b, reproduced below, illustrates another example of a multichip package fabricated pursuant to the method described in Bertin. Ex. 1004, 2:45–49.

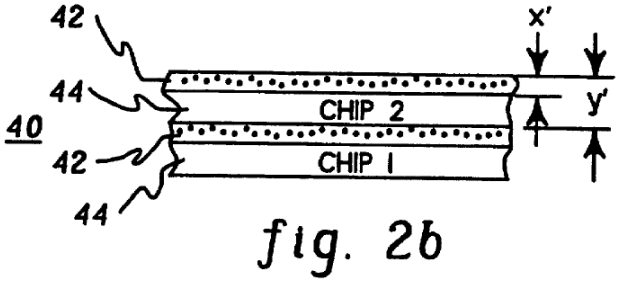


fig. 2b

Figure 2b shows two thin semiconductor chips, chip 1 and chip 2, stacked in package 40. *Id.* at 3:28–30. Active layer 42 of each chip in package 40 has a thickness "x" which, as shown, is a portion of the chip thickness "y." *Id.* at 3:30–33. Thickness "x" may be in the 5–20 micrometers range, while the

overall thickness "y" of each device may be only 20 micrometers or less. *Id.* at 3:35–38.

Additionally, Bertin teaches that the multichip package includes vertical electrical interconnections (e.g., metallized trenches 66) that pass completely through substrates 52. Ex. 1004, Abstract, 1:62–2:12, 4:11–52, Figs. 3c, 3b, 3e, 3g). Referring to Figure 3e, Bertin provides that trenches 62 are filled with metal to create metallized trenches 66 that extend through etch stop layer 53. *Id.* at 4:43–48. Contact pads 68 interconnect the appropriate wiring on the chip to vertically disposed wiring 66 in trenches 62. *Id.* at 4:48–52.

2. Summary of Poole (Ex. 1005)

Poole is directed to a method for making thinned charge-coupled devices, which are thinned to allow illumination of the backside of the device to improve quantum efficiency and UV spectral response. Ex. 1005, Abstract, 1:8–11. In one example, Poole teaches that a standard thick silicon charge-coupled device (Fig. 1A) has its pixel face mounted to a transparent, optically flat glass substrate using a thin layer of thermoset epoxy. *Id.* at Abstract. The backside silicon of the charge-coupled device is thinned to 10 ±0.5 μm using a two-step chemi-mechanical process. *Id.* The bulk silicon is thinned to 75 μm with a 700 micro-grit aluminum oxide abrasive and is then thinned and polished to 10 μm using 80 nm grit colloidal silica. *Id.*

3. Summary of Leedy (Ex. 1006)

Leedy relates to the fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and semiconductor materials. Ex. 1006, 1:38–41. In the Abstract, Leedy indicates that the disclosed integrated circuits are fabricated from flexible membranes "formed

of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers." *Id.* at Abstract. Leedy also discloses forming a "tensile low stress dielectric membrane" on a semiconductor layer as part of its integrated circuit structure. *Id.* at 1:53–58. Leedy further defines "[l]ow stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8 x 10^8 dynes/cm^2 (preferably 1 x 10^7 dynes/cm^2) in tension." *Id.* at 11:33–37. Additionally, Leedy discloses two chemical vapor deposition (CVD) process recipes for manufacturing "structurally enhanced low stress dielectric circuit membranes." *Id.* at 11:51–65.

Referring to Figure 8, Leedy discloses a three dimensional circuit membrane. *Id.* at 4:43. Figure 8 is reproduced below.

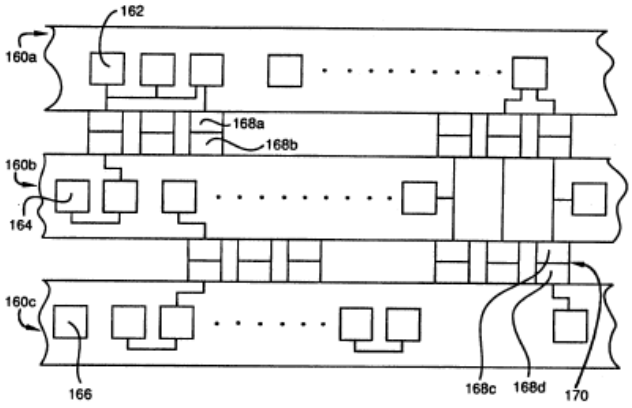


Fig_8

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three dimensional circuit structure. *Id.* at 16:38–40. Interconnection between circuit membranes 160a, 160b, 160c including SDs 162, 164, 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between

4 μm and 25 μm in diameter) on the surface of two circuit membranes 160b, 160c and using a mechanical or gas pressure source to press bond pads 168c, 168d together. *Id.* at 16:43–49.

4. Analysis

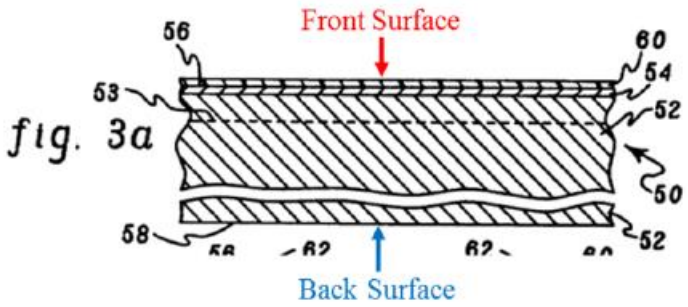
Petitioner argues that claims 1–3, 30, 31, 33, 40, 41, and 44 are obvious over the combination of Bertin, Poole, and Leedy. *See* Pet. 3. Below we discuss independent claim 1, which is illustrative of the subject matter of claims 2, 3, 30, 31, 33, 40, 41, and 44.

Claim 1 relates to a stacked integrated circuit that includes a "circuit substrate." For this limitation, Petitioner argues that Bertin teaches each stacked chip of the multichip package is "a semiconductor device 50 (preferably comprising a wafer) having a substrate 52 and an active layer 54." Pet. 29 (citing Ex. 1004, 3:50–62, 1:55–62, Figs. 2b, 3a–3i). Petitioner argues that because the active layer 54 of substrate 52 includes circuitry, each stacked chip 50 is a "circuit substrate." *Id.* at 29 (citing Ex. 1004, 4:1–3, 6:43–8:36, Figs. 5a, 5b). Petitioner adds that Bertin further discloses that the first stacked chip 50 may be bonded to a base integrated circuit chip with circuitry. *Id.* (citing Ex. 1004, 4:63–5:9, Abstract, 1:68–2:5, 8:50–10:21, Figs. 3f–3i). Based on the current record, Petitioner's position is persuasive.

Claim 1 further recites "a first integrated circuit having circuitry formed on a front surface thereof, the front surface or a back surface being bonded to the circuit substrate."

For this limitation, Petitioner argues that substrate 52 of each stacked device 50 of the multichip package has an upper planar surface 56 and a lower planar surface 58. Pet. 30 (citing Ex. 1004, 3:50–60). Petitioner provides an annotated Figure 3a, reproduced below, which Petitioner argues

shows active layer 54 on the front surface of substrate 52.



Petitioner further argues that in Figures 3e and 3h, Bertin discloses that the front and back surfaces of each stacked device 50 includes contact pads for bonding and electrical interconnection. Pet. 31. With reference to Figure 3i of Bertin, Petitioner explains that "the first device 50 (claimed 'integrated circuit') incorporated into the multichip package is flipped over and its front surface is bonded to 'a suitable carrier 70,' or alternatively 'a base integrated circuit chip,' which is a circuit substrate." Pet. 31 (Ex. 1004, 4:63–5:9, Figs. 2b, 3f–3i). Petitioner further argues that another device 50 (e.g., another integrated circuit) can be added to the stack in a similar manner. *Id.* (citing Ex. 1004, 2:7–12, 4:26–29, 4:63–5:38, 10:28–31, Figs. 2b, 3f–3i). Based on the current record, Petitioner's arguments are persuasive.

> Additionally, claim 1 requires that
>
> one or more additional integrated circuits each having circuitry formed on respective front surfaces thereof, each additional integrated circuit having the front surface or a back surface thereof adjacent to the front surface or a back surface of an adjacent integrated circuit

For this limitation, Petitioner argues that Bertin teaches the "stacking process is repeated by the respective addition of integrated circuit devices

one on top of the other, each having its active layer positioned adjacent to the last thinned exposed surface of the stack with contact pads 68 contacting at least some of the exposed metallized trenches 66 therein." Pet. 32 (citing Ex. 1004, 5:30–36, Abstract, 1:10–15, 1:55–62, 2:7–12, 2:24–29, 3:25–31, 9:3–10:12, Figs. 2b, 3a–3i, 5b). Based on this disclosure, Petitioner argues that each additional device 50 incorporated into the multichip package, each having circuitry formed on its front surface, is flipped over and its front surface bonded to the back of the previous device 50 incorporated into the multichip package. Pet. 32. Based on the current record, Petitioner's arguments are persuasive.

Claim 1 further recites:

> wherein at least one of the first integrated circuit and the one or more additional integrated circuits is substantially flexible and comprises a substantially flexible semiconductor substrate of one piece made from a semiconductor wafer thinned by at least one of abrasion, etching and parting, and subsequently polished to form a polished surface.

For these limitations, Petitioner argues that Bertin teaches or suggests a "substantially flexible semiconductor substrate of one piece made from a semiconductor wafer thinned by at least one of abrasion, etching and parting" because Bertin discloses that each device 50 may be 20 micrometers or less. Pet. 33. In particular, Petitioner argues that Bertin's substrate 52 is thinned to 20 μm or less by a conventional wet etching process, which begins "'with a semiconductor device 50 (preferably comprising a wafer) having a substrate 52' thickness of 'approximately 750-800 micrometers (15 mils).'" Pet. 33 (citing Ex. 1004, 3:50–65, Figs. 3a–3e). Further, Petitioner argues Bertin teaches that "[a]fter thinning, the

stacked 'semiconductor chips . . . have only a thin layer of substrate for support of the active layer,' such that the overall thickness of each chip is '20 micrometers or less.'" *Id.* at 34 (citing Ex. 1004, 3:25–38, Fig. 2b). Petitioner adds that Bertin teaches a substrate of "one piece" because substrate 52 "corresponds to a standard wafer that is bulk silicon, which is diced before or after packaging." *Id.* at 34 (citing Ex. 1004, 4:30–33, 4:52–62).

Petitioner acknowledges that Bertin does not explicitly disclose that substrate 52 is polished. Pet. 34–36. Petitioner relies upon Poole's description of a two-step thinning process, which includes a grinding (or lapping) step followed by a chemical mechanical polishing ("CMP") step: "The bulk silicon is thinned to 75 μm with a 700 micro-grit aluminum oxide abrasive and is then thinned and polished to 10 um using 80 nm grit colloidal silica." Pet. 34–35 (citing Ex. 1005, 3:12−47, Abstract, 4:21−25, 5:60−7:2, 7:51−68, 8:21−24).

Petitioner argues that it would have been obvious to modify Bertin to replace its wet etching process with Poole's two-step thinning process for several reasons. Pet. 26–28 (citing Ex. 1002 ¶¶ 97–100, 124, 126). For example, both Bertin and Poole generally relate to processing of semiconductor circuit substrates. *Id.* at 26 (citing Ex. 1004, Abstract, 1:55–2:31; Ex. 1005, Abstract, 3:12–25). In addition, both Bertin and Poole address a similar need—a process by which a silicon circuit substrate is thinned from the backside to less than about 20 μm with a resulting surface that is planar and has minimal defects. Pet. 27 (citing Ex. 1004, 3:25–46, 3:57–60, 4:4–10; Ex. 1005, Abstract, 2:15–24, 2:35–45, 2:55–58, 3:20–25). Petitioner notes that Poole's two-step thinning process results in a substrate

with a thickness of 10 μm, which falls within the "5–20 micrometers range" desired in Bertin. *Id.* (citing Ex. 1004, 3:35–38). Therefore, according to Petitioner, Poole's two-step thinning process achieves the predictable result of a thin substrate with a planar surface having minimal defects, which is desired in Bertin to facilitate the formation of reliable vertical interconnects and bonds between substrates. *Id.*

Petitioner notes that in addition to wet etching, like that described in Bertin, there were only a handful of known methods for thinning semiconductor substrates recognized in the semiconductor processing community at the time of the alleged invention. Pet. 27–28 (citing Ex. 1002 ¶ 124). According to Petitioner, given that there were only a few available primary methods for thinning semiconductor substrates, all of which provided the predictable result of a thin substrate, it would have been obvious to try Poole's well-known two-step thinning process in place of Bertin's wet etching process with a reasonable expectation of success. Pet. 27–28 (citing Ex. 1002 ¶¶ 97–100).

Additionally, Petitioner argues that the combination of Bertin and Leedy teaches and suggests the "substantially flexible" integrated circuits recited in claim 1 because Leedy discloses dielectrics having a stress of 5×10^8 dynes/cm^2 tensile or less. Pet. 35. According to Petitioner, "substantially flexible" when used to modify integrated circuits means "an integrated circuit having a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed, and where the dielectric material used in processing the semiconductor substrate must have a stress of 5×10^8 dynes/cm^2 tensile or less." Pet. 33. Under this construction, Petitioner asserts that, based on Leedy's disclosure, it would

have been obvious to one of ordinary skill in the art to modify Bertin's dielectric layer 60 and interconnect insulators to have a stress of 5×10^8 dynes/cm^2 tensile or less. Pet. 35. Petitioner asserts that Leedy describes processes for depositing silicon oxide or silicon nitride dielectric material, preferably having a tensile stress of 1 x 10^7 dynes/cm^2. Pet. 24 (citing Ex. 1006, 11:33–37).

Furthermore, Petitioner provides several reasons why it would have been obvious to one of ordinary skill in the art to substitute Leedy's low tensile stress dielectric material for the dielectrics disclosed in Bertin. Pet. 22–24. These include that Leedy expressly teaches that low tensile stress is important because otherwise "surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane." Pet. 23–24 (citing Ex. 1006, 5:63–6:5). Petitioner argues that Leedy teaches its low tensile stress dielectrics can advantageously be used to insulate circuit devices and interconnect metallization, while at the same time increasing structural integrity and durability. *Id.* at 24 (citing Ex. 1006, Abstract, 1:53–62, 2:9–31, 2:66–3:3, 3:56–4:13, 30:36–42, 45:49–46:26, 46:52–47:33, Figs. 32a–32d). Petitioner adds that Leedy teaches that its described dielectrics advantageously have lower stress than thermally grown oxides, like those used in Bertin. *Id.* (citing Ex. 1006, 6:30–33).

Petitioner further asserts that Leedy's disclosed "PECVD" was a commonly available deposition technique that could have been used in place of the techniques for growing dielectrics described in Bertin to obtain the predictable result of stacked integrated circuits having low tensile stress dielectrics. Pet. 25 (citing Ex. 1002 ¶¶ 110–113). Petitioner further argues

that because Leedy teaches that its dielectrics are versatile and can "withstand a wide range of IC processing techniques and processing temperatures (of at least 400 C) without noticeable deficiency in performance," one of ordinary skill in the art would have reasonably expected success combining the teachings of Bertin and Leedy. *Id.* at 25 (citing Ex. 1006, 2:37–40, 1:50–52, 5:32–33; Ex. 1002 ¶¶ 110–113).

In response, Patent Owner first argues that Leedy's disclosure lacks "critical" information regarding its dielectric and "[g]iven Leedy '695's dearth of information about these properties, it is implausible that one of skill would select the Leedy '695 dielectric for inclusion in an IC at all, much less that one would be "motivated" to do so." Prelim. Resp. 30–31 (citing Ex. 1006, 6:44–47, 11:33–64, 12:27–29; Ex. 1040, 109, 192).

Based on the current record, Patent Owner's arguments are not persuasive. As Petitioner points out, Leedy discloses two "typical recipes used to produce the dielectric membranes of silicon dioxide or silicon nitride required by the MDI process." Ex. 1006, 11:40–42, 1:51–64. Leedy further teaches that its "dielectric membrane is compatible with most higher temperature IC processing techniques." *Id.* at 5:32–33. In light of this disclosure, we agree with Petitioner, for the purposes of this Decision, that one of ordinary skill in the art would apply Leedy's disclosure of a low stress dielectric to IC fabrication generally. Moreover, even assuming Patent Owner is correct that Leedy does not disclose the electrical and material properties of its dielectrics, Patent Owner has not explained adequately why one with ordinary skill in the art would not be able to use Leedy's dielectric in an IC for this reason. Prelim. Resp. 30–31. Indeed, a disclosure can be enabling even though some experimentation is necessary.

Hybritech Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1384 (Fed. Cir. 1986).

Next, Patent Owner argues that the prior art teaches away from the use of Leedy's "unconventional" tensile dielectrics. Prelim. Resp. 31–32. Patent Owner argues that a journal article from IBM teaches away from using tensile dielectrics with PECVD and a declaration from Dr. Alain Harrus indicates that it was "unconventional" for customers of Novellus to request low tensile stress dielectrics. *Id.* (citing Ex. 1040, 114–115; Ex. 1045, 8; Ex. 2133, 447; Ex. 2137, 3).

A reference teaches away from a claimed invention if it "criticizes, discredits, or otherwise discourages" modifying the reference to arrive at the claimed invention. *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). However, we will not "read into a reference a teaching away from a process where no such language exists." *Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1364 (Fed. Cir. 2006).

We are not persuaded by Patent Owner's teaching away arguments. The passage that Patent Owner cites from the IBM article discusses "[a]dvances in dielectric processes in 0.35-μm CMOS manufacturing and development" that have been implemented in IBM manufacturing and development lines. Ex. 2133, 447. In that particular "PECVD process," the article discusses degradation of film properties at lower power; "e.g., film stress becomes tensile." *Id.* However, based on the current record, Patent Owner has not explained sufficiently how the process discussed in the IBM article detracts from Leedy's express disclosure of using low stress dielectrics in *conventional* integrated circuits. *See* Ex. 1006, Abstract ("[T]he flexible membrane is used as support and electrical interconnect for

conventional integrated circuit die bonded thereto . . . ."). Moreover, we are not persuaded by Dr. Harrus's characterization of customer's requests as "unconventional." Specifically, Patent Owner has not explained sufficiently how an "unconventional" customer request "criticizes, discredits, or otherwise discourages" the combination of Leedy's and Bertin's teachings. *See Fulton*, 391 F.3d at 1201.

Patent Owner further argues that Petitioner's arguments lack expert support because paragraphs 104–114 of Dr. Franzon's declaration do not provide facts, data, or analysis to support the opinion stated. Prelim. Resp. 37. We do not agree with Patent Owner's arguments. For example, in paragraph 104 of his declaration, Dr. Franzon supports his testimony with citations to Leedy's disclosure. Ex. 1002 ¶ 104. While Patent Owner may disagree with Dr. Franzon's testimony, we are not persuaded, based on the current record, that Dr. Franzon's testimony lacks facts, data, analysis, etc. We note, however, Patent Owner will have ample opportunity to develop the record further through cross-examination of Dr. Franzon's testimony.

Additionally, Patent Owner argues that: (1) Petitioner does not identify a need or problem in Bertin regarding its dielectrics; (2) Petitioner mischaracterizes Leedy in suggesting that the disclosed dielectric could provide benefits in the context of a conventional stacked-IC device; and (3) Petitioner ignores the complexity of what they propose, and the numerous reasons that one of ordinary skill would not even attempt what Petitioner proposes. Prelim. Resp. 33–34, 38–47. With respect to Poole's disclosure, Patent Owner argues that Bertin does not discuss any problem with its wet etch process and Petitioner has not explained adequately how a skilled artisan would modify Bertin's method to use Poole's specialized tools.

Prelim. Resp. 47–50.

First, Patent Owner's argument that Petitioner does not identify a need or problem in Bertin is unpersuasive. *See* Prelim. Resp. 38, 47. This argument misstates the requirements of *KSR Int'l v. Teleflex Inc.*, 550 US 398 (2007). An obviousness analysis does not require the prior art references themselves to explicitly state a reason (including identifying a need or problem) for the combination of the disclosed teachings. A reason to combine teachings from the prior art "may be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved." *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1355 (Fed. Cir. 1999) (citing *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998)); *see also KSR*, 550 US at 419 ("The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents.").

Second, based on the current record, we are not persuaded that Petitioner has mischaracterized the teachings of Leedy. Petitioner described numerous "benefits" of Leedy, (*e.g.*, Pet. 23–24), which include those discussed in Dr. Franzon's declaration. For example, Dr. Franzon testifies that

> 110. *Leedy '695* identifies several advantages of the disclosed dielectric deposition techniques, including improved surface flatness, improved ability to cope with later higher temperature processing steps, lower dielectric film stress, and improved structural integrity. *See, e.g.*, Ex. 1006 at 2:9-31, 2:37-40 ("This membrane is able to withstand a wide range of IC processing techniques and processing temperatures (of at least 400° C.)

> without noticeable deficiency in performance."), 3:56-4:13, 5:63-6:5 ("If the membrane is not in tensile stress, but in compressive stress, surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane."), 6:48-58, 45:49-46:26. *Leedy '695* also explains that dielectric material deposited using the disclosed processes have a stress lower than dielectric material deposited using oxidation. *See, e.g., id.* at 6:30-33. In addition, *Leedy '695* discusses matching the "coefficient of thermal expansion of the semiconductor material and the various dielectric materials . . . in order to minimize the extrinsic net surface stress of the membrane." *Id.* at 6:26-30.

Ex. 1002 ¶ 110. Thus, based on the current record, Petitioner's arguments are persuasive.

Third, based on the current record, Patent Owner's arguments in its Preliminary Response largely constitute bare statements lacking sufficient supporting evidence or technical reasoning. For example, Patent Owner argues that

> the cited ability of Leedy '695's dielectric "to withstand a wide range of IC processing techniques and process temperatures (of at least 400 C.) without noticeable deficiency in performance" (*id.*) provides no benefit in the context of Bertin, where the Leedy '695 dielectric would be replacing a **thermal** oxide. Numerous moderate- and high-stress dielectrics can also withstand a wide range of IC processing techniques. For example, thermal oxidation produces a silicon dioxide layer often formed early in the fabrication process for delimiting transistor regions, and thus, the layer must withstand a very wide range of subsequent high-temperature IC processing techniques. Ex. 1040 at 198-99.

Prelim. Resp. 43–44. While pages 198 through 199 of Exhibit 1040 describe "Thermal Oxidation of Single Crystal Silicon," Patent Owner has not persuasively explained how this reference teaches that Leedy's dielectric

would provide "no benefit" in the context of Bertin.

As a further example, Patent Owner contends that

> Petitioners rely entirely on their assertion that Leedy '695 discloses known PECVD techniques using "a commonly available deposition technique" to support their contention that substituting Leedy '695's dielectric for the dielectrics in Bertin would yield predictable results. Pet. at 23-25. But to say that a person of ordinary skill knows how to perform a specific process does not speak to whether that particular process would work in a series of hundreds of complex processes that are performed during the fabrication of a complex semiconductor device.

Prelim. Resp. 45. However, Patent Owner's statements are conclusory and lack citation to supporting evidence. Therefore, based on the current record, Patent Owner has not explained persuasively how Petitioner has mischaracterized Leedy or failed to explain sufficiently how the combination of Bertin, Poole, and Leedy teach or suggest the limitations of claim 1. We reiterate, however, that Patent Owner may further develop the record regarding these issues during the proceeding.

Additionally, Patent Owner argues that Petitioner's challenges based on Bertin, Poole, Hsu, and Leedy are redundant with rejections considered during the prosecution of separate, but related Patent Application No. 10/672,961 (the '961 application). Prelim. Resp. 11–15. Specifically, Patent Owner argues that "Bertin and Hsu are being cited for substantially the same facts as Sugiyama, then being combined with Leedy '695 in substantially the same way for substantially the same purported purpose of increasing structural integrity and durability in a stacked 3D IC device." *Id.* at 14.

Patent Owner's arguments are unpersuasive. Petitioner's challenge

relies on the combinations of Bertin, Poole, Hsu, and Leedy, which were not the basis (e.g., Sugiyama, Watanabe, and Leedy) for the Examiner's rejection in the prosecution of the related patent application. *See* Prelim. Resp. 11–15. Moreover, even assuming that substantially the same art for substantially the same claims were considered previously by the Office, we are not required to deny the Petitioner's challenge on this basis. Section 325(d) provides: "[i]n determining whether to institute . . . a proceeding . . . , the Director ***may*** take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." Emphasis added. Having considered the record before the Office during examination, as well as the parties' arguments and present record, we decline to exercise our discretion to deny the Petition based on the prosecution of a related patent application. Additionally, we are not persuaded that all the issues presented by the Petitioner's combinations of Bertin, Poole, Hsu, and Leedy have been considered previously by the Office. We note, for example, that the Petition relies on testimony of Dr. Franzon (Ex. 1002), which was not before the Office previously. Accordingly, based on a review of the developed record, Petitioner has demonstrated that there is a reasonable likelihood that challenged claim 1 is unpatentable over the combination of Bertin, Poole, and Leedy. We have also considered the parties' arguments and evidence regarding dependent claims 2, 3, 30, 31, 33, 40, 41, and 44. *See* Pet. 36–43. Based on the current record, we are persuaded that there is a reasonable likelihood that Petition would prevail on its assertion that these claims are unpatentable over the combination of Bertin, Poole, and Leedy.

C. Claims 1–3, 30, 31, 33, 40, 41, and 44 – Obvious over Hsu and Leedy

1. Hsu (Ex. 1008)

Hsu relates generally to a "method of connecting three-dimensional integrated circuit chips using trench technology." Ex. 1008 at Abstract, 1:8-11. Referring to Figures 2–8, Hsu's fabrication process starts with etching deep trenches 16 on silicon substrate 10, which Hsu indicates can be composed of monocrystalline silicon. *Id.* at 2:50–61. According Hsu, the master chip and subordinate chip each consist of a semiconductor substrate, preferably composed of monocrystalline silicon. *Id.* at 2:51–54, 3:42–45. These chips can be "stacked by interconnection through [a] pad window . . . during integrated circuit processing." *Id.* at 1:28–31. Hsu further describes that the "bottom surface of the [subordinate] substrate is ground and polished so that only a thin portion of the substrate remains." *Id.* at 3:21–23.

2. Analysis

Petitioner argues that claims 1–3, 30, 31, 33, 40, 41, and 44 are obvious over the combination of Hsu and Leedy. *See* Pet. 3, 43–56. For this challenge, Petitioner argues that

> Hsu discloses stacked chips each having a "silicon dioxide film 18 . . . formed on the entire surface of the substrate" including on the vertical walls of Hsu's vertical interconnects (Ex. 1008 at 2:63-67, Figs. 2-7), but does not explicitly disclose that the dielectric layer 18 constitutes a "low stress" dielectric characterized by a tensile stress of about 5×10^8 dynes/cm^2 or less, as recited in the challenged claims.

Pet. 43–44. Additionally, with respect to claim 1, Petitioner asserts that Hsu discloses a master chip with semiconductor substrate 40 (e.g., circuit substrate) and an integrated circuit subordinate chip (first integrated circuit) with semiconductor substrate 10, where the back surface of the subordinate

chip is bonded to the front surface of the maser chip. Pet. 48–49 (citing Ex. 1003, 3:41–4:2, Figs. 10–12). Petitioner further argues that Hsu discloses its process of fabricating and bonding the master chip and the subordinate chip, shown in Figures 2–10, can be used to connect "another subordinate chip" to the integrated circuit chip illustrated in Figure 12. *Id.* at 50 (citing Ex. 1008, 4:7–14). Petitioner adds that Hsu teaches that substrate 10 is "preferably composed of monocrystalline and is ground and polished so that only a thin portion of the substrate remains over trenches 20, which have a depth of more than about 10 microns." *Id.* at 50 (Ex. 1008, 2:51–54, 2:60–63).

Petitioner further argues that it would have been obvious to modify Hsu's device with Leedy's dielectric based on the disclosure in Leedy. *Id.* at 44 (citing Ex. 1002 ¶¶ 104–114). Petitioner provides several reasons for this proposed combination, including many of those discussed above for the combination of Bertin, Poole, and Leedy. Pet. 43–47. For example, Petitioner argues that Leedy expressly teaches that "the described low tensile stress dielectrics can advantageously be used to insulate circuit devices and interconnect metallization, while at the same time increasing structural integrity and durability. *See, e.g.*, *id.* at Abstract, 1:53-62, 2:9-31, 2:66-3:3, 3:56-4:13, 30:36-42, 45:49-46:26, 46:52-47:33, Figs. 32a-32d." Pet. 45.

In its Preliminary Response, Patent Owner presents essentially the same or similar arguments against the combination of Hsu and Leedy that have been discussed with respect to the combination of Bertin, Poole, and Leedy. Prelim. Resp. 50–58. In particular, Patent Owner's arguments include that (1) Petitioner ignores the differences between dielectrics; (2) Petitioner's arguments lack expert support; (3) Petitioner does not identify a need in Hsu for the combination; (4) Petitioner mischaracterizes Leedy; and

(5) Petitioner ignores the complexity of the proposed combination and the reasons a skilled artisan would not have attempted the combination. *Id.*

For the same reasons discussed above, based on the current record, we are persuaded that Petitioner has demonstrated a reasonable likelihood that Petitioner would prevail with respect to this challenge against claims 1–3, 30, 31, 33, 40, 41, and 44.

D. Claims 1 and 44 – Obvious over Bertin and Poole; Obvious over Hsu

Petitioner includes these challenges in the event that the terms "substantially flexible" substrate and "integrated circuit"/"circuit substrate" are construed "more broadly." Pet. 58. Petitioner adds that even under a broader construction, claims 1 and 44 would be unpatentable in view of the combination of Bertin and Poole for the same reasons discussed with regard to the combination of Bertin, Poole, and Leedy. *Id.* Similarly, Petitioner argues that claims 1 and 44 would be unpatentable over Hsu for the same reasons discussed with regard to the combination of Hsu and Leedy. *Id.* at 58–59. Having reviewed the developed record at this stage in the proceeding, we conclude there is a reasonable likelihood Petitioner would prevail and institute these challenges for the same reasons discussed previously with respect to the challenges based on Bertin, Poole, and Leedy, and Hsu and Leedy respectively..

E. Claims 1–3, 30, 31, 33, 40, 41, and 44 – Obvious over Hsu and Kowa

Petitioner argues that claims 1–3, 30, 31, 33, 40, 41, and 44 are unpatentable over the combination of Hsu and Kowa. *See* Pet. 4. Kowa discloses "provid[ing] an excellent semiconductor device having a controlled stress direction" by controlling the chemical vapor deposition ("CVD") technique used to apply silicon nitride thin films. Ex. 1007, 7.

Petitioner argues that if claim features relating to a low stress dielectric is determined to require stress-balancing multiple dielectrics, Kowa discloses this feature. Pet. 56–58. Petitioner does not propose this construction and, further, does not provide any support for this construction in the Petition. *Id.* at 56 ("Petitioner presents Ground 3 to the extent Patent Owner incorrectly argues that the claim features relating to low tensile stress dielectrics can be satisfied by" stress balancing."). Nonetheless, our construction of "low stress dielectric" does not require stress-balancing, (*supra* Claim Construction), and, as such, we are not persuaded by Petitioner's arguments that Kowa's alleged disclosure of stress-balancing teaches or suggests a "low stress dielectric," which we have construed to mean a dielectric having a stress of less than 8×10^8 dynes/cm^2. Moreover, while Petitioner argues that Kowa discloses a "zero or very slightly tensile net stress can be achieved" with stress-balancing, Petitioner has not explained sufficiently how such a zero or slight net stress discloses a "low stress dielectric." *See* Pet. 59. As discussed above, in the context of describing a "low stress dielectric," the '542 patent distinguishes between a dielectric having low stress and those having conventional or high stress, including silicon nitride and silicon oxide dielectrics. Ex. 1001, 8:66–9:11.

Accordingly, we are not persuaded that Petitioner has established there is a reasonable likelihood that Petitioner would prevail with respect to this challenge.

III. CONCLUSION

For the foregoing reasons, we are persuaded that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail with respect to its challenge as to the patentability

of claims 1–3, 30, 31, 33, 40, 41, and 44.

The Board has not made a final determination on the patentability of any challenged claims or the construction of any claim terms.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the ’542 patent is hereby instituted on the following asserted grounds:

A. Claims 1–3, 30, 31, 33, 40, 41, and 44 as unpatentable under 35 U.S.C. § 103 over Bertin, Poole, and Leedy;

B. Claims 1–3, 30, 31, 33, 40, 41, and 44 as unpatentable under 35 U.S.C. § 103 over Hsu and Leedy;

C. Claims 1 and 44 as unpatentable under 35 U.S.C. § 103 over Bertin and Poole; and

D. Claims 1 and 44 as unpatentable under 35 U.S.C. § 103 over Hsu;

FURTHER ORDERED that the trial is limited to the grounds identified above and no other grounds are authorized; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial commences on the entry date of this decision.

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