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Paper 11
Entered: July 1, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX, INC.,
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00388
Patent 7,193,239 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and FRANCES L. IPPOLITO, *Administrative Patent Judges*.

BENOIT, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively "Petitioner") filed a Petition for *inter partes* review of claims 1, 10–13, 18–20, 60–63, 67, 70–73, and 77 ("the challenged claims") of U.S. Patent No. 7,193,239 B2 (Ex. 1001, "the '239 patent" or "the challenged patent"). (Paper 4, "Pet."). Patent Owner, Elm 3DS Innovations, LLC, filed a Preliminary Response to the Petition (Paper 8, "Prelim. Resp.").

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

Upon consideration of the information presented in the Petition and Preliminary Response, we determine that the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of claims 10–12, 18–20, 60–63, 67, 70–73, and 77 ("the remaining challenged claims"). For reasons explained below, we do not institute an *inter partes* review with respect to claims 1 and 13, which have been disclaimed by the Patent Owner.

A. Related Proceedings

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 1–2; Paper 7 (Patent Owner's Mandatory Notices). Petitioner indicates that the challenged patent is involved in the

following United States District Court proceedings: *Elm 3DS Innovations, LLC v. Samsung Elecs. Co.*, No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK Hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

Additionally, the challenged patent also is the subject of a petition filed in IPR2016-00393, and patents related to the challenged patent are the subjects of petitions filed in IPR2016-00386 (U.S. Patent No. 8,653,672); IPR2016-00387 (U.S. Patent No. 8,841,778); IPR2016-00389 (U.S. Patent No. 8,035,233); IPR2016-00390 (U.S. Patent No. 8,629,542); IPR2016-00391 (U.S. Patent No. 8,796,862); IPR2016-00394 (U.S. Patent No. 8,410,617); IPR2016-00395 (U.S. Patent No. 7,504,732); IPR2016-00687 (U.S. Patent No. 8,928,119); IPR2016-00691 (U.S. Patent No. 7,474,004); IPR2016-00703 (U.S. Patent No. 8,791,581); IPR2016-00706 (U.S. Patent No. 8,791,581); IPR 2016-00786 (U.S. Patent No. 8,933,570); IPR2016-00708 (U.S. Patent No. 8,907,499); and IPR2016-00770 (U.S. Patent No. 8,907,499).

B. Statutory Disclaimer of Challenged Claims 1 and 13

"The patent owner may file a statutory disclaimer under 35 U.S.C. 253(a) in compliance with § 1.321(a) of this chapter, disclaiming one or more claims in the patent. No *inter partes* review will be instituted based on disclaimed claims." 37 C.F.R. § 42.107(e). After Petitioner filed its Petition, Patent Owner filed a statutory disclaimer of challenged claims 1 and 13 under 35 U.S.C. § 253(a). Prelim. Resp. 12; Ex. 2139. The disclaimer, Exhibit 2139, is in compliance with 37 C.F.R. § 1.321(a).

Accordingly, we do not institute an *inter partes* review of disclaimed claims 1 and 13.

C. Time Bar under 35 U.S.C. § 315(b)

Patent Owner argues that Petitioner is time-barred under 35 U.S.C. § 315(b) because two of the real-parties-in-interest, Samsung Austin Semiconductor, LLC ("SAS") and Samsung Semiconductor, Inc. ("SSI"), were served with a complaint alleging infringement of the challenged patent on December 24, 2014. Prelim. Resp. 6–10; *see* Pet. 1 (identifying real parties-in-interest). Patent Owner contends that the Petition was filed on December 28, 2015, which was four days after the statutory one year period for SAS and SSI had expired. *Id.* at 7; *see* Paper 5 (According filing date of December 28, 2015 to the Petition).

In the Petition, Petitioner explained that it filed its Petition on December 28, 2015 because the Office considered December 22–24, 2015, to be a "Federal holiday within the District of Columbia" pursuant to 35 U.S.C. § 21. Pet. 3. On December 22, 2015, the Office experienced a major power outage at its headquarters in Alexandria, Virginia, resulting in damaged equipment that required the subsequent shutdown of many USPTO online and information technology systems. On December 28, 2015, the Office announced that

> [i]n light of this *emergency situation*, the USPTO will consider each day from Tuesday, December 22, 2015, through Thursday, December 24, 2015, to be a "Federal holiday within the District of Columbia" under 35 U.S.C. § 21 and 37 C.F.R. §§ 1.6, 1.7, 1.9, 2.2(d), 2.195, and 2.196. Any action or fee due on these days will be considered as timely for the purposes of, e.g., 15 U.S.C. §§ 1051(b), 1058, 1059, 1062(b), 1063, 1064, and 1126(d), or 35 U.S.C. §§ 119, 120, 133, and 151, if the action is taken, or the fee paid, on the next succeeding business day on which the USPTO is open (37 C.F.R. §§ 1.7(a) and 2.196).

Ex. 3001 (emphasis added). Section 21(b) states that "[w]hen the day, or the last day, for taking any action or paying any fee in the United States Patent and Trademark Office falls on Saturday, Sunday, or a federal holiday within the District of Columbia, *the action may be taken, or the fee paid, on the next succeeding secular or business day*." Emphasis added.

Petitioner has complied with the requirements of § 315(b) given the circumstances of the power outage during the December 22–24, 2015 period and the announcements by the Office regarding the same. December 28, 2015, which was a Monday, was the next succeeding business day after December 24, 2015, because Friday, December 25, 2015, was a federal holiday. Moreover, we disagree with Patent Owner's arguments that the Office lacks the authority to treat December 22–24, 2015 as federal holidays. *See* Prelim. Resp. 7–9.

D. The Challenged Patent

The challenged patent relates generally to a three-dimensional structure (3DS) for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1a is reproduced below.

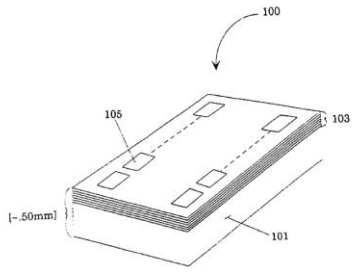

Figure 1a

Figure 1a shows 3DS memory device 100 having a stack of integrated circuit layers with a "fine-grain inter-layer vertical interconnect" between all circuit layers. *Id.* at 4:10–13. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:30–32. The challenged patent discloses that "each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness." *Id.* at 4:35–38. The challenged patent further discloses that the "thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication." *Id.* at 8:66–9:4.

Figure 1b is reproduced below.

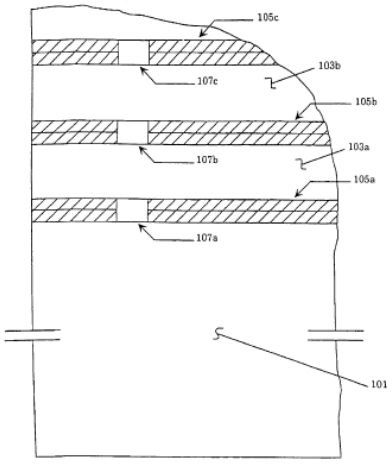

Figure 1b

Figure 1b of the challenged patent shows a cross-section of a 3DS integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:50–52. Bond and interconnect layers 105a, 105b, 105c are

shown between circuit layers 103a and 103b. *Id.* at Fig. 1b. The challenged patent discloses that pattern 107a, 107b, 107c in the bond and interconnect layers 105a, 105b, 105c defines the vertical interconnect contacts between the integrated circuit layers and serves to electrically isolate these contacts from each other and the remaining bond material. *Id.* at 4:24–29. Additionally, the challenged patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:28–29.

Further, the challenged patent teaches that the "term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 µm. . . ." *Id.* at 4:13–19. The fine-grain inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:19–20.

E. Illustrative Claim

Of the remaining challenged claims, claims 60 and 70 are independent. Claim 60 is illustrative of the claimed subject matter:

> 60. An integrated circuit structure comprising:
>
> a plurality of semiconductor dice, each die having an integrated circuit formed thereon, said dice being stacked in layers, wherein at least one of the plurality of dice is substantially flexible, and wherein at least one of the plurality of dice has at least one of polycrystalline active circuitry formed thereon, reconfiguration circuitry formed thereon, and passive circuitry formed thereon; and
>
> between adjacent dice, a bonding layer bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice, with at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice.

F. Asserted Ground of Unpatentability

Petitioner contends that claims 1, 10–13, 18–20, 60–63, 67, 70–73, and 77 of the challenged patent are unpatentable under 35 U.S.C. § 103 as obvious over Yu[1] and Leedy '695.[2] Pet. 3, 19–53.

II. DISCUSSION

A. Claim Construction

We interpret claims of an unexpired patent using the "broadest reasonable construction in light of the specification of the patent in which [the claims] appear[]." 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, No. 15-446, 2016 WL 3369425, at *12 (U.S. June 20, 2016) (concluding the broadest reasonable construction "regulation represents a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office"). Under that standard, claim terms are presumed to be given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Further, "[t]he PTO should also consult the patent's prosecution history in proceedings in which the patent has been brought back to the agency for a second review." *Microsoft Corp. v.*

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[1] Yu, et al., *Real-Time Microvision System with Three-Dimensional Integration Structure*, Proc. of the 1996 IEEE/SICE/RSJ Int'l Conf. on Multisensor Fusion and Integration for Intelligent Systems, 1996 (Ex. 1009, "Yu").

[2] U.S. Patent No. 5,354,695, issued Oct. 11, 1994 (Ex. 1006, "Leedy '695").

Proxyconn, Inc., 789 F.3d 1292, 1298 (Fed. Cir. 2015). Moreover, the Board may not "construe claims during IPR so broadly that its constructions are unreasonable under general claim construction principles." *Id.*

Petitioner proposes a construction for (i) "'a substantially flexible' semiconductor substrate" (Pet. 9–13) and (ii) "substantially flexible" when modifying the terms "semiconductor die" or "semiconductor dice" (*id.* at 13–16). Patent Owner contends that Petitioner's proposed construction is irrelevant to this proceeding and that Petitioner has acknowledged that these claim terms are not determinative in this case. Prelim. Resp. 15–16.

For purposes of this decision, we construe "substantially flexible substrate" and "die is substantially flexible." These preliminary claim constructions may change as a result of the record developing during trial. We note, for example, that Patent Owner has not yet filed its response under 37 C.F.R. § 42.120 or any new testimonial evidence. We determine that no other terms require express construction for this decision.

1. "substantially flexible substrate"

Independent claims 1 and 13, from which challenged claims 10–12 and 18–20 directly or indirectly depend, respectively recite "a substantially flexible substrate" and "a substantially flexible . . . substrate." The term "substantially flexible" is a term of degree that lacks clear meaning absent context because the words "substantially flexible" do not provide any measure to compare against prior art and potentially infringing substrates. *See Playtex Prods., Inc. v. Procter & Gamble Co.*, 400 F.3d 901, 908 (Fed. Cir. 2005) ("'Substantially flattened surface' is clearly a comparative term.

Comparison requires a reference point. Therefore, to flatten something, one must flatten it with respect to either itself or some other object.").

Petitioner urges that in light of the intrinsic record, the broadest reasonable construction of "substantially flexible semiconductor substrate" is "a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed." Pet. 9. Petitioner argues that the Patent Owner, acted as its own lexicographer in defining "substantially flexible" in the written description of the challenged patent when ""substantially flexible" is used to describe a semiconductor substrate or how to make a substantially flexible substrate:

> Grind the backside or exposed surface of the second circuit substrate to a thickness of less than 50 μm and then polish or smooth the surface. The thinned substrate is now a substantially flexible substrate.

Id. (citing Ex. 1001, 9:25–28; *see also id.* at 3:18–21, 4:33–38).

Petitioner further argues that Patent Owner (then, Applicant) confirmed this definition during prosecution of related patents and applications. *Id.* at 10. For example, during prosecution of related U.S. Patent No. 8,907,499 ("the '499 patent"), the Examiner objected to certain claims as indefinite for including the term "substantially flexible." *Id.* (citing Ex. 1018, 4). Petitioner notes that Applicant overcame the objection by arguing that "substantially flexible" is unambiguous because it is "clearly explained in the specification." *Id.* at 10–11 (citing Ex. 1019, 9; Ex. 1020, 18:1–3 (Portion of the Application that issued as the '499 patent corresponding to Ex. 1001, 9:3–6). Thus, according to Petitioner, Applicant clearly and unmistakably set forth a definition of the term "substantially

flexible" when used to modify semiconductor substrate and Applicant expressed an intent to define the term. *Id.* at 11.

On this record, we agree in large part with Petitioner's proposed construction. Looking to the Specification, however, we note that the Summary of the Invention section in the challenged patent does not limit the meaning of a "substantially flexible substrate" to those substrates that have been polished. More specifically, the challenged patent teaches *"[t]hinning of the memory circuit to less than about 50 μm in thickness forming a substantially flexible substrate* with planar processed bond surfaces and bonding the circuit to the circuit stack while still in wafer substrate form." Ex. 1001, 3:18–21 (emphasis added). In other words, the Specification does not require polishing for "forming a substantially flexible substrate." *Id.*

Accordingly, given the claim language and statements in the Specification and considering the prosecution history for a related patent, we preliminarily construe "substantially flexible substrate" as "a substrate that has been thinned to a thickness of less than 50 μm." *Cf. Microsoft*, 789 F.3d at 1298 ("The PTO should also consult the patent's prosecution history in proceedings in which the patent has been brought back to the agency for a second review.").

2. "die is substantially flexible"

Claims 60–67, 70–73, and 77 include "substantially flexible" limitations relating to a semiconductor die rather than to a substrate. For example, independent claim 60 recites "at least one of the plurality of dice is substantially flexible," and independent claim 70 recites "the die is substantially flexible."

Petitioner proposes that we construe "die is substantially flexible" in much the same manner as it proposes to construe "substantially flexible semiconductor substrate" and makes similar arguments for its proposed construction. Pet. 14–17. For the same reasons as stated above, we similarly construe "die is substantially flexible" as "die having a semiconductor substrate that has been thinned to a thickness of less than 50 μm."

B. Asserted Ground of Obviousness over Yu and Leedy '695

Petitioner contends that claims 1, 10–13, 18–20, 60–63, 67, 70–73, and 77 of the challenged patent are unpatentable under 35 U.S.C. § 103 as obvious over Yu and Leedy '695. Pet. 3, 19–53. Petitioner supports its contentions with citations to the references and with declaration testimony of Paul D. Franzon, Ph.D. (Ex. 1102). *Id*. Patent Owner opposes. *See*, *e.g.*, Prelim. Resp. 1–6, 16–58.

Because Patent Owner has statutorily disclaimed independent claims 1 and 13 (Ex. 2139), we will not institute an *inter partes* review of claims 1 and 13 over Yu and Leedy '695. *See* 37 C.F.R. § 107(e). Each of claims 10–12, however, depends directly or indirectly from independent claim 1 and, therefore, each requires all the limitations recited in disclaimed claim 1. Similarly, each of claims 18–20 depends directly or indirectly from disclaimed claim 13 and requires all the limitations recited by that claim. Accordingly, we will include the limitations recited in disclaimed claims 1 and 13 as necessary to our discussion of this asserted ground.

A claim is unpatentable as obvious "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention

was made to a person having ordinary skill in the art." 35 U.S.C. § 103. "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")).

1. Summary of Yu

Yu describes a three-dimensional integrated circuit structure for implementing a real-time microvision system. Ex. 1009, 831–832. "The system consists of a number of 2D LSIs vertically stacked using 3D LSI technology. . . ." *Id.* at 832. Yu's Figure 1 is reproduced below.

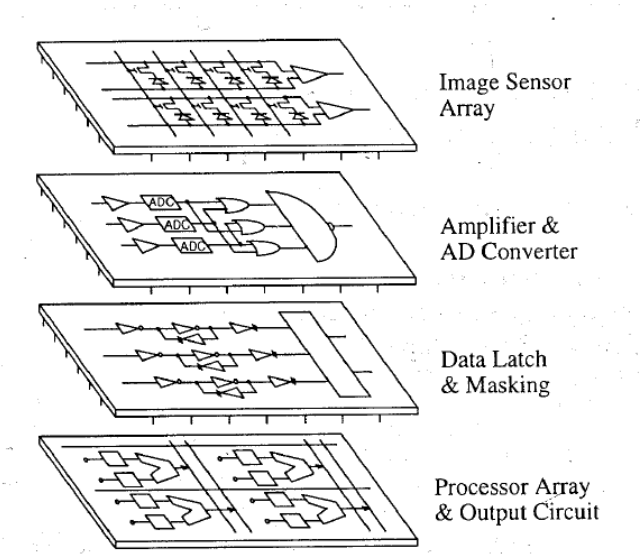


Figure 1: Basic concept of real-time microvision system with 3D integration structure

Figure 1 shows a basic concept of a real-time microvision system with a 3D integration structure.

In Yu's microvision system, substrates are ground and polished to thin the substrates to about 30 microns. *Id.* at 831–832 ("The Si substrate of the 2D-LSI which has the basic circuits is ground and polished to make thin wafer."); *id.* at Abstract ("In fabrication, the grinding and chemical-mechanical polishing techniques are used to thin the wafer to 30 μm."). Wafers then are bonded together using a combination of conductive microbumps and a UV-hardening adhesive. *Id.* at 834–835 ("The thinned wafer is bonded to a thick wafer using In/Au micro-bumps with the minimum size of 5 μm x 5 μm and UV hardening adhesive layer with thickness of 1 μm by forcing the z direction pressure after careful wafer alignment."). The microbumps connect to buried interconnect structures that form vertical interconnects between vertically stacked circuitry. *Id.* at Fig. 8.

2. Summary of Leedy '695

Leedy '695 is a United States Patent that relates to the fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and semiconductor materials. Ex. 1006, 1:38–41. In its Abstract, Leedy '695 indicates that the disclosed integrated circuits are fabricated from flexible membranes "formed of very thin low stress dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers." *Id.* at Abstract. Leedy '695 also discloses forming a "tensile low stress dielectric membrane" on a semiconductor layer as part of its integrated circuit structure. *Id.* at 1:53–58. Leedy '695 defines "low stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8×10^8 dynes/cm^2 (preferably 1×10^7 dynes/cm^2) in tension." *Id.* at 11:33–37. Additionally,

Leedy '695 discloses two chemical vapor deposition (CVD) process recipes for manufacturing "structurally enhanced low stress dielectric circuit membranes." *Id.* at 11:51–65.

Referring to Figure 8, Leedy '695 discloses a three dimensional circuit membrane. *Id.* at 4:43. Figure 8 is reproduced below.

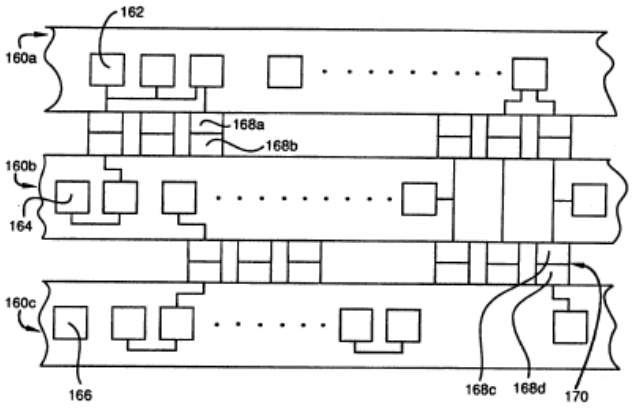


Fig_8

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three dimensional circuit structure. *Id.* at 16:38–40. Interconnection between circuit membranes 160a, 160b, 160c including SDs 162, 164, 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between 4 μm and 25 μm in diameter) on the surface of two circuit membranes 160b, 160c and using a mechanical or gas pressure source to press bond pads 168c, 168d together. *Id.* at 16:43–49.

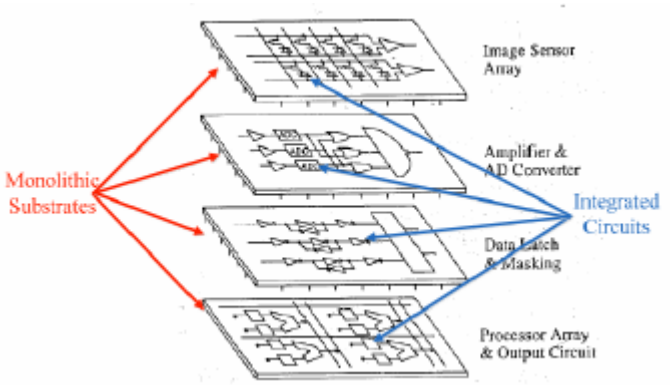
3. Petitioner's Contentions

Petitioner provides, with support of its declarant, analysis purporting to explain how the combination of Yu and Leedy '695 would have conveyed to one of ordinary skill in the art the limitations recited in the challenged

claims. *See* Pet. 22–50; *see also id.* at 50–53 (providing "a detailed explanation of grounds under alternative constructions," including the preliminary claim construction in section II.A.1). Also with support of its declarant, Petitioner provides reasons why one of ordinary skill in the art would have combined the teachings of the references in the manner proposed by Petitioner. *See, e.g., id.* at 19–22.

a. Limitations Recited in Claim 10

Turning first to the limitations recited in the remaining challenged claims, Petitioner relies on Yu's microvision system with a 3D integration structure as describing most of the limitations recited in the remaining challenged claims. *Id.* at 19 ("Yu teaches or suggests all but a few of the features recited in the Challenged Claims."). For example, regarding claim 10, which depends from independent claim 1, Petitioner relies on Yu's description of a "number of two-dimensional LSI (2D-LSI) layers each of which comprises the claimed monolithic substrate." *Id.* at 22 (citing Ex. 1009, 831–832). According to Petitioner, Yu teaches that the layers are monolithic and stacked, integrated circuits are formed on the layers, and each layer comprises one substrate. *Id.* at 23 (citing Ex. 1009, 831–832, 834; Ex. 1102 ¶ 99). Petitioner annotates Yu's Figure 1 to illustrate Petitioner's position and is reproduced below.



As shown in Petitioner's annotation of Yu's Figure 1, Yu's two-dimensional LSI layers correspond to the recited "monolithic substrates" and each LSI layer includes an integrated circuit, as required by the claim. *Id.* at 23 (showing and describing Petitioner's annotation of Yu's Fig. 1).

For the recited substantially flexible substrate, Petitioner relies on Yu's description of grinding and polishing one of the substrates "to make a thin wafer." *Id.* at 23 (citing Ex. 1009, 831–832). Petitioner indicates, with support of its declarant, Dr. Franzon, that Yu's thinned wafer is thinned to a "thickness of around 30 μm," and, thus, is a substantially flexible substrate, as required by claim 10, because each thinned wafer "meets the thickness requirement of the claim." *Id.* at 24–25 (citing Ex. 1009, 831–832; Ex. 1102 ¶ 99).

Claim 10 recites a limitation not found in independent claim 1—"the circuitry is formed with a low stress dielectric." Petitioner acknowledges that Yu does not disclose expressly that "its dielectric material . . . has a tensile stress of about 5 x 10^8 dynes/cm^2 tensile or less, which the '239 patent confirms would satisfy the claimed 'low stress' dielectric." *Id.* at 28–29 (citing Ex. 1001, 8:66–9:1, Ex. 1102 ¶ 100). For that limitation, Petitioner relies on Leedy '695. *See, e.g., id.* at 29. According to Petitioner,

Leedy '695 "discloses processes for depositing silicon oxide having a low tensile stress of preferably 1 x 10^7 dynes/cm^2 for insulating circuit devices and vertical interconnect metallization." *Id.* (citing Ex. 1006, 11:33–37, 45:49–46:26; *see also id.* at 1:53–58, 2:40–45, 3:9–11, 7:1–9:63, 9:28–31, 11:25–65, 47:46–51, 48:45–50, Fig. 32b). Thus, according to Petitioner the combination of Yu and Leedy '695 would have conveyed to one of ordinary skill in the art forming Yu's circuitry with a low stress dielectric disclosed by Leedy '695.

b. Rationale for Combining Yu and Leedy '695

Petitioner provides, with support of Dr. Franzon, several reasons why "it would have been obvious to one of ordinary skill in the art . . . to modify the processes and device in Yu such that the dielectrics used therein would be characterized by a tensile stress of about 5 x 10^8 dynes/cm^2 or less, based on the disclosure of Leedy '695. Pet. 19–20 (citing Ex. 1102 ¶¶ 92–97). For example, with support from Dr. Franzon, Petitioner contends that Leedy '695 provides express motivations for modifying Yu's processes and device to incorporate Leedy '695's low tensile stress dielectric material, in that Leedy '695 explains that low tensile stress is important because otherwise "surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane." Pet. 20 (citing Ex. 1006 at 5:63–6:5; Ex. 1102 ¶ 94).

4. Patent Owner's Contentions

In response, Patent Owner contends that there is not a reasonable likelihood that Petitioner's proposed combination would have rendered obvious the challenged claims. *See generally* Prelim. Resp.

In general, Patent Owner notes that the central premise of the Petition is its contention that it would have been obvious to substitute the dielectric of Leedy '695 in place of the dielectrics used in Yu. *Id.* at 4. According to Patent Owner, Petitioner's stated reasons why one of ordinary skill would make the suggested dielectric substitution "gloss over" technical details and lack sufficient factual or expert support. *Id.* at 4, 16–21. Patent Owner argues that semiconductor fabrication development is a complex and unpredictable, and that one of ordinary skill cannot simply substitute one dielectric with another dielectric and have a reasonable expectation of success. *Id.* at 4. Rather, one must use the "new" dielectric when fabricating the integrated circuit, which requires dealing with the different parameters associated with the various materials to be used. *Id.*

More specifically, Patent Owner first argues that the dielectric in Leedy '695 is unconventional and "is inapplicable to the dielectric in conventional integrated circuits," such as the dielectric in Yu. *Id.* at 17–36. Patent Owner asserts that, as a general matter, in conventional semiconductor devices, a dielectric's role is to provide insulation, which is the role of dielectrics in Yu. *Id.* at 17. In contrast, Leedy '695's low tensile stress dielectric also provides an insulative effect, but the primary problem being solved was to provide structural support for a device that has no semiconductor substrate. *Id.* According to Patent Owner, this is not the case in Yu, which provides support during processing from a rigid carrier.

Id. (citing Ex. 1009 at 834). Patent Owner argues that Petitioner does not explain why one of ordinary skill, when fabricating a silicon substrate integrated circuit, would look to the unorthodox dielectrics in Leedy '695 instead of conventional dielectrics—particularly when Leedy '695 does not suggest any benefit for the low tensile stress dielectrics beyond the ability to form free-standing membranes. *Id.* at 30–31. Patent Owner contends that Petitioner has "failed to establish a credible reason . . . that would justify the adoption of the low tensile stress dielectric of Leedy '695 into the structure disclosed in Yu" because the passages relied on by Petitioner "describe the use of a low tensile stress dielectric for fabricating a free-standing circuit membrane." *Id.* at 55.

According to Patent Owner, (i) Leedy '695 lacks critical information regarding its dielectric (*id.* at 31–33), (ii) the prior art teaches away from Petitioner's combination involving the use of Leedy '695's "unconventional" tensile dielectrics (*id.* at 33–34), and (iii) the benefits identified in Leedy '695 on which Petitioner's relied do not relate to low tensile stress dielectrics (*id.* at 34–36).

Patent Owner further specifically contends that one of ordinary skill in the art would not have had reason to combine Leedy '695 with Yu because (i) Petitioner does not identify a need or problem in Yu (*id.* at 40), (ii) Petitioner allegedly mischaracterizes the benefits Leedy '695 would provide (*id.* at 40–46), (iii) Petitioner fails to prove "predictability" of the combination (*id.* at 46–48), (iv) Petitioner ignores "the complexity" of the combination (*id.* at 48–51), (v) many of the substitutions proposed by Petitioner "would not work" (*id.* at 51–53), and (vi) Petitioner "ignores the

reasons one of ordinary skill would not even attempt what Petitioner[] propose[s]" (*id*. at 53–55).

For support of these arguments, Patent Owner relies on a declaration from Dr. Alain Harrus that indicates that it was "unconventional" for customers of Novellus to request low tensile stress dielectrics. Id. at 33–34 (citing Ex. 2137, 3). In addition to the Harrus declaration, Patent Owner relies on a citations to a 600-page book describing the process of fabricating integrated circuits. *See, e.g., id.* at 33 (citing Ex. 1040). Patent Owner also relies on a 1995 journal article noting that with the chemical vapor deposition process PECVD "film properties degrade at lower power; e.g., film stress becomes tensile" as teaching away from using tensile dielectrics. *Id*. at 332 (citing Ex. 2133, 447).

5. Analysis

On the present record and for purposes of institution, we determine that Petitioner has made a sufficient showing that the combination of Yu and Leedy '695 would have conveyed to one of ordinary skill in the art the limitations of claim 10. As described above (Petitioner's Contentions), Petitioner has described sufficiently its proposed combination, with citations to the references and supported by the declaration testimony of Dr. Franzon.

Regarding Petitioner's proffered rationale for combining the references in the manner proposed by Petitioner and Patent Owner's

challenge of the purported rationale, we recognize that Patent Owner has not yet had an opportunity to submit new testimonial evidence.[3]

After weighing Patent Owner's arguments and evidence as currently developed in its Preliminary Response against the Petition with its citations to declaration testimony of Dr. Franzon, we determine that, based on the current record and for the purposes of institution, Petitioner has explained sufficiently with support of Dr. Franzon that one of ordinary skill in the art would have understood that it would be beneficial to make the proffered substitution of Leedy '695's dielectric for Yu's dielectric. Pet. 19–22 (citing Ex. 1102). *See, e.g.*, *Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding the Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so"); *In re Am. Acad. of Sci. Tech Ctr*., 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.").

Moreover, we do not agree with Patent Owner's arguments that Petitioner do not identify a need or problem in Yu. An obviousness analysis does not require the prior art references themselves to explicitly state a reason (including identifying a need or problem) for the combination of the disclosed teachings. A reason to combine teachings from the prior art "may be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of

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[3] *See* 37 C.F.R. § 42.107(c) (July 1, 2013) ("The preliminary response shall not present new testimony evidence beyond that already of record, except as authorized by the Board.").

the problem to be solved." *WMS Gaming*, 184 F.3d at 1355 (citing *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998)); *see also KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 419 (2007) ("[t]he obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents.").

Furthermore, on the present record, we do not agree that a prior art journal article or the Harrus declaration teaches away from the combination, as Patent Owner contends. A reference teaches away from a claimed invention if it criticizes, discredits, or otherwise discourages modifying the reference to arrive at the claimed invention. *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004).

The journal article discusses "[a]dvances in dielectric processes in 0.35-µm CMOS manufacturing and development" that have been implemented in manufacturing and development lines. Ex. 2133, 447. In a particular process, the article discusses degradation of film properties at lower power—"e.g., film stress becomes tensile." *Id.* Based on the current record, however, Patent Owner has not explained sufficiently how the process discussed in the article detracts from Leedy '695's express disclosure of using low stress dielectrics in conventional integrated circuits. *See* Ex. 1006, Abstract ("[T]he flexible membrane is used as support and electrical interconnect for conventional integrated circuit die bonded thereto . . . .").

Similarly, regarding Patent Owner's teaching away argument concerning the Harrus declaration, Patent Owner has not explained sufficiently how an "unconventional" customer request criticizes, discredits,

or otherwise discourages the combination of Leedy '695 and Bertin '754's teachings. *See Fulton*, 391 F.3d at 1201.

We also disagree with Patent Owner's contention that Dr. Franzon's testimony, on which Petitioner relies, is insufficient for institution of an *inter partes* review because Dr. Franzon does not provide "any support" for his conclusion. *Id.* at 44–45 (apparently referring to Ex. 1102 ¶ 94); *see also id.* at 4. Dr. Franzon's testimony includes various citations to prior art references. *See* Ex. 1102 ¶ 94 (citing Ex. 1006, 11:28–32, 11:52–62).

For the foregoing reasons, we determine that Petitioner has provided adequate evidence to show a reasonable likelihood of prevailing in its assertions that at least one of the challenged claims would have been obvious over Yu and Leedy '695.

Nor do we agree with Patent Owner that Petitioner mischaracterize Leedy '695 and the benefits it can purportedly provide in the context of the Yu device. Petitioner described numerous "benefits" of Leedy '695 (e.g., Pet. 20–21), which include those discussed in Dr. Franzon's declaration. For example, Dr. Franzon testifies that:

> 93. First, according to *Leedy '695*, having a low tensile stress dielectric layer in a stacked integrated circuit device allows the layer "to withstand a wide range of IC processing techniques and processing temperatures (of at least 400 C.) without noticeable deficiency in performance." Ex. 1006 at 2:37-40. *Leedy '695* explains the alleged importance of having low tensile stress as follows: "If the membrane is not in tensile stress, but in compressive stress, surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane." *Id*. at 5:63-6:5. Thus, in light of the potential benefits disclosed by *Leedy '695*—improved surface flatness, improved ability to cope with later higher temperature processing

> steps, lower dielectric film stress, and improved structural integrity—a person of ordinary skill in the art would have been motivated to apply the low-stress dielectric deposition techniques disclosed in *Leedy '695* to the stacked integrated circuit structure disclosed in *Yu*. Moreover, the POSA would have had a reasonable expectation that doing so would result in the benefits described in Leedy '695.

Ex. 1102 ¶ 93.

For the foregoing reasons, we determine that Petitioner has provided adequate evidence to show a reasonable likelihood of prevailing in its assertions that at least one of the challenged claims would have been obvious over would have been obvious over Yu and Leedy '695.

C. Prosecution of Related Patent Applications

Patent Owner also contends that we should deny the Petition under 35 U.S.C. § 325(d). Prelim. Resp. 12–15. Patent Owner urges this action because Petitioner's asserted grounds use some references considered by the Examiner during prosecution of related patents and, according to Patent Owner, Petitioner's asserted grounds raise similar issues to those considered during prosecution. *Id*. For example, Patent Owner contends that "[a]t most, the proposed Ground swaps out a previously considered primary reference for a new one allegedly disclosing the same thing." *Id.* at 12. According to Patent Owner, "[t]he specific argument of the proposed [g]round is that it would have been obvious to replace the dielectrics of a 3D stacked [integrated circuit] disclosed by a primary reference with the Leedy '695 dielectric having a low tensile stress . . . to obtain benefits such as increased structural integrity and durability and thereby arrive a the claimed invention." *Id.* Patent Owner also contends that Leedy '695 and U.S. Patent No. 5,202,754 to Bertin ("Bertin '754"), which, like Yu,

discloses a 3d stacked integrated circuit, were considered by the Examiner during prosecution of a related patent application, but that the Examiner never raised the combination of Leedy '695 and Bertin '754. *Id.* at 14. Patent Owner seems to be arguing that, because the Examiner did not reject the pending claims in a related patent application during prosecution over the combination of Leedy '695 and Bertin '754, the Examiner did not consider the pending claims to be unpatentable over the combination of those references and so would not have considered the pending claims to be unpatentable over a purportedly similar combination—Yu and Leedy '695 as asserted by Petitioner.

First, to the extent that Patent Owner is arguing we should give deference to earlier determinations of allowability because of the Examiner's "explicit consideration" of a similar combination considered during examination (i.e., Leedy '695 and Sugiyama), there is no presumption of validity as to the challenged claims in an *inter partes* review.[4] Furthermore, under 35 U.S.C. § 325(d), "[i]n determining whether to institute or order a proceeding under . . . chapter 31 [*Inter Partes* Review], the Director *may* take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office" (emphasis added). The permissive language of the statute indicates that we may consider a petition that presents the same prior art or arguments previously presented to the Office.

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[4] Whereas a patent is presumed "valid" unless overcome by clear and convincing evidence before a district court, a petitioner's burden in an *inter partes* review is to prove "unpatentability" by a preponderance of the evidence. *Compare* 35 U.S.C. § 282(a), *with* § 316(e).

Moreover, Patent Owner argues that "[i]n the present Petition, Yu is being cited for substantially the same facts as Sugiyama, then being combined with Leedy '695 in substantially the same way for substantially the same purported purpose of increasing structural integrity and durability in a stacked 3D [integrated circuit] device." *Id.* at 14. Even assuming that substantially the same art for substantially the same claims had been considered previously by the Office, we are not persuaded that all the issues presented by the Petitioner's combinations of Yu and Leedy '695 have been considered previously by the Office. We note, for example, that the Petition relies on testimony of Dr. Franzon (Ex. 1102), which was not before the Office previously.

Having considered the record before the Office during examination, as well as the parties' arguments and present record, we decline to exercise our discretion to deny the Petition based on the prosecution of a related patent application.

III. CONCLUSION

For the foregoing reasons, we determine that there is a reasonable likelihood that Petitioner would prevail in showing that at least one of claims 10–12, 18–20, 60–63, 67, 70–73, and 77 of the challenged patent is unpatentable.

Any discussion of facts in this decision are made only for the purposes of institution and are not dispositive of any issue related to any ground on which we institute review. The Board has not made a final determination with respect to the patentability of any challenged claim. The Board's final determination will be based on the record as fully developed during trial.

IV. ORDER

After due consideration of the record before us, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the challenged patent is instituted on the following ground of unpatentability asserted in the Petition: claims 10–12, 18–20, 60–63, 67, 70–73, and 77 under 35 U.S.C. § 103 over Yu and Leedy '695;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial commences on the entry date of this decision; and

FURTHER ORDERED that the trial is limited to the grounds identified above and no other ground set forth in the Petition as to any challenged claim is authorized.

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