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Paper 14
Entered: July 1, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
MICRON TECHNOLOGY, INC., and SK HYNIX, INC.,
Petitioner,

v.

ELM 3DS INNOVATIONS, LLC,
Patent Owner.

Case IPR2016-00386
Patent 8,653,672 B2

Before GLENN J. PERRY, BARBARA A. BENOIT, and FRANCES L. IPPOLITO, *Administrative Patent Judges*.

BENOIT, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively "Petitioner") filed a Petition for *inter partes* review of claims 17, 18, 22, 84, 95, 129–132, 143–146, 151, and 152 of U.S. Patent No. 8,653,672 B2 (Ex. 1001, "the '672 patent" or "the challenged patent"). (Paper 4, "Pet."). Patent Owner, Elm 3DS Innovations, LLC, filed a Preliminary Response to the Petition (Paper 10, "Prelim. Resp.").

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

Upon consideration of the information presented in the Petition and Preliminary Response, we determine that the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of claims 17, 18, 22, 84, 95, 129–132, 145, 146, and 152 ("the challenged claims"). For reasons explained below, we do not institute an *inter partes* review with respect to claims 143, 144, and 151, which have been disclaimed by the Patent Owner.

A. Related Proceedings

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 1–2; Paper 9 (Patent Owner's Mandatory Notices). Petitioner indicates that the challenged patent is involved in the following United States District Court proceedings: *Elm 3DS Innovations,*

LLC v. Samsung Elecs. Co., No. 1:14-cv-01430 (D. Del.); *Elm 3DS Innovations, LLC v. Micron Tech., Inc.*, No. 1:14-cv-01431 (D. Del.); and *Elm 3DS Innovations, LLC v. SK Hynix Inc.*, No. 1:14-cv-01432 (D. Del.).

Additionally, patents related to the challenged patent are the subjects of petitions filed in IPR2016-00387 (U.S. Patent No. 8,841,778); IPR2016-00388 and IPR2016-00393 (U.S. Patent No. 7,193,239); IPR2016-00389 (U.S. Patent No. 8,035,233); IPR2016-00390 (U.S. Patent No. 8,629,542); IPR2016-00391 (U.S. Patent No. 8,796,862); IPR2016-00394 (U.S. Patent No. 8,410,617); IPR2016-00395 (U.S. Patent No. 7,504,732); IPR2016-00687 (U.S. Patent No. 8,928,119); IPR2016-00691 (U.S. Patent No. 7,474,004); IPR2016-00703 (U.S. Patent No. 8,791,581); IPR2016-00706 (U.S. Patent No. 8,791,581); IPR2016-00786 (U.S. Patent No. 8,933,570); IPR2016-00708 (U.S. Patent No. 8,907,499); and IPR2016-00770 (U.S. Patent No. 8,907,499).

B. Statutory Disclaimer of Claims 143, 144, and 151 of the Challenged Patent

"The patent owner may file a statutory disclaimer under 35 U.S.C. 253(a) in compliance with § 1.321(a) of this chapter, disclaiming one or more claims in the patent. No *inter partes* review will be instituted based on disclaimed claims." 37 C.F.R. § 42.107(e). After Petitioner filed its Petition, Patent Owner filed a statutory disclaimer of claims 143, 144, and 151 of the challenged patent under 35 U.S.C. § 253(a). Prelim. Resp. 50; Ex. 2140. The disclaimer, Exhibit 2140, is in compliance with 37 C.F.R. § 1.321(a).

Accordingly, we do not institute an *inter partes* review of disclaimed claims 143, 144, and 151.

C. Time Bar under 35 U.S.C. § 315(b)

Patent Owner argues that Petitioner is time-barred under 35 U.S.C. § 315(b) because two of the real-parties-in-interest, Samsung Austin Semiconductor, LLC ("SAS") and Samsung Semiconductor, Inc. ("SSI"), were served with a complaint alleging infringement of the challenged patent on December 24, 2014. Prelim. Resp. 5–10; *see* Pet. 1 (identifying real parties-in-interest). Patent Owner contends that the Petition was filed on December 28, 2015, which was four days after the statutory one year period for SAS and SSI had expired. *Id.* at 6; *see* Paper 5 (According filing date of December 28, 2015 to the Petition).

In the Petition, Petitioner explained that it filed its Petition on December 28, 2015 because the Office considered December 22–24, 2015, to be a "Federal holiday within the District of Columbia" pursuant to 35 U.S.C. § 21. Pet. 3. On December 22, 2015, the Office experienced a major power outage at its headquarters in Alexandria, Virginia, resulting in damaged equipment that required the subsequent shutdown of many USPTO online and information technology systems. On December 28, 2015, the Office announced that

> [i]n light of this *emergency situation*, the USPTO will consider each day from Tuesday, December 22, 2015, through Thursday, December 24, 2015, to be a "Federal holiday within the District of Columbia" under 35 U.S.C. § 21 and 37 C.F.R. §§ 1.6, 1.7, 1.9, 2.2(d), 2.195, and 2.196. Any action or fee due on these days will be considered as timely for the purposes of, e.g., 15 U.S.C. §§ 1051(b), 1058, 1059, 1062(b), 1063, 1064, and 1126(d), or 35 U.S.C. §§ 119, 120, 133, and

> 151, if the action is taken, or the fee paid, on the next succeeding business day on which the USPTO is open (37 C.F.R. §§ 1.7(a) and 2.196).

Ex. 3001 (emphasis added). Section 21(b) states that "[w]hen the day, or the last day, for taking any action or paying any fee in the United States Patent and Trademark Office falls on Saturday, Sunday, or a federal holiday within the District of Columbia, *the action may be taken, or the fee paid, on the next succeeding secular or business day*." Emphasis added.

Petitioner has complied with the requirements of § 315(b) given the circumstances of the power outage during the December 22–24, 2015 period and the announcements by the Office regarding the same. December 28, 2015, which was a Monday, was the next succeeding business day after December 24, 2015, because Friday, December 25, 2015, was a federal holiday. Moreover, we disagree with Patent Owner's arguments that the Office lacks the authority to treat December 22–24, 2015 as federal holidays. *See* Prelim. Resp. 6–8.

D. The Challenged Patent

The challenged patent relates generally to a three-dimensional structure (3DS) for integrated circuits that allows for physical separation of memory circuits and control logic circuits on different layers. Ex. 1001, Abstract. Figure 1a is reproduced below.

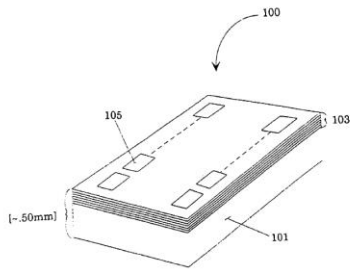

Figure 1a

Figure 1a shows 3DS memory device 100 having a stack of integrated circuit layers with a "fine-grain inter-layer vertical interconnect" between all circuit layers. *Id.* at 3:64–67. Layers shown include controller circuit layer 101 and memory array circuit layers 103. *Id.* at 4:17–19. The challenged patent discloses that "each memory array circuit layer is a thinned and substantially flexible circuit with net low stress, less than 50 μm and typically less than 10 μm in thickness." *Id.* at 4:22–24. The challenged patent further discloses that the "thinned (substantially flexible) substrate circuit layers are preferably made with dielectrics in low stress (less than 5×10^8 dynes/cm^2) such as low stress silicon dioxide and silicon nitride dielectrics as opposed to the more commonly used higher stress dielectrics of silicon oxide and silicon nitride used in conventional memory circuit fabrication." *Id.* at 8:45–50.

Figure 1b is reproduced below.

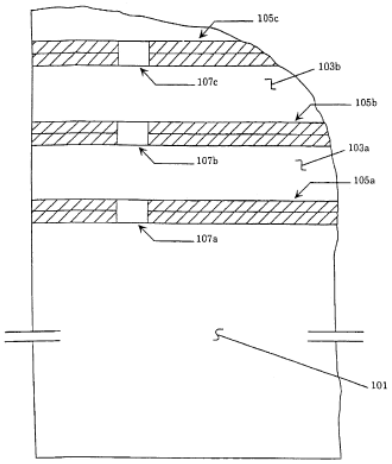

Figure 1b

Figure 1b of the challenged patent shows a cross-section of a 3DS integrated circuit with metal bonding interconnect between thinned circuit layers. *Id.* at 3:38–40. Bond and interconnect layers 105a, 105b, 105c are shown between circuit layers 103a and 103b. *Id.* at Fig. 1b. The challenged patent discloses that pattern 107a, 107b, 107c in the bond and interconnect layers 105a, 105b, 105c defines the vertical interconnect contacts between the integrated circuit layers and serves to electrically isolate these contacts from each other and the remaining bond material. *Id.* at 4:11–15. Additionally, the challenged patent teaches that the pattern takes the form of voids or dielectric filled spaces in the bond layers. *Id.* at 4:15–16.

Further, the challenged patent teaches that the "term fine-grained inter-layer vertical interconnect is used to mean electrical conductors that pass through a circuit layer with or without an intervening device element and have a pitch of nominally less than 100 µm. . . ." *Id.* at 3:67–4:4. The fine-grain inter-layer vertical interconnect functions to bond together various circuit layers. *Id.* at 4:5–7.

E. Illustrative Claim

Of the challenged claims, claims 17, 84, 129, and 143 are independent. Claim 17 is illustrative of the claimed subject matter:

> 17. An integrated circuit structure comprising:
>
> a first substrate having topside and bottomside surfaces, wherein the topside surface of the first substrate supports interconnect contacts;
>
> a substantially flexible semiconductor second substrate having topside and bottom-side surfaces, wherein at least one of the topside surface and the bottom-side surface of the second substrate supports interconnect contacts, and wherein the bottom-side surface of the second substrate is formed by removing semiconductor material from the second substrate and is smoothed or polished after removal of the semiconductor material; and
>
> conductive paths between the interconnect contacts supported by the topside surface of the first substrate and the interconnect contacts supported by the second substrate; wherein the first substrate and the second substrate overlap fully or partially in a stacked relationship; and
>
> wherein at least one of:
>
> i.) the first and second substrates are bonded together in fixed relationship to one another at least predominantly with metal, or at least predominantly with silicon- based dielectric material and metal; and
>
> ii.) the integrated circuit structure further comprises a low-stress silicon-based dielectric material having a stress of $5x10^8$ dynes/cm^2 tensile or less.

Ex. 1001, 14:57–15:12 (paragraphing added).

F. The Asserted Grounds of Unpatentability

Petitioner contends that claims 17, 18, 22, 84, 95, 129–132, 143–146, 151, and 152 of the challenged patent are unpatentable under 35 U.S.C. § 103 based on the following specific grounds (Pet. 17–60):

References	Claims Challenged
Bertin '754,[1] Poole,[2] and Leedy '695[3]	17, 18, 22, 84, 95, 129–132, 145, 146, and 152
Bertin '754 and Poole	143, 144, and 151
Yu[4] and Leedy '695	17, 18, 22, 84, 95, 129–132, 143–146, 151, and 152
Yu and Kowa[5]	17, 18, 22, 84, 95, 129–132, 143–146, 151, and 152

II. DISCUSSION

A. Claim Construction

We interpret claims of an unexpired patent using the "broadest reasonable construction in light of the specification of the patent in which [the claims] appear[]." 37 C.F.R. § 42.100(b); *see Cuozzo Speed*

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[1] U.S. Patent No. 5,202,754, issued April 13, 1993 (Ex. 1004, "Bertin '754").
[2] U.S. Patent No. 5,162,251, issued Nov. 10, 1992 (Ex. 1005, "Poole").
[3] U.S. Patent No. 5,354,695, issued Oct. 11, 1994 (Ex. 1006, "Leedy '695").
[4] Yu, et al., *Real-Time Microvision System with Three-Dimensional Integration Structure*, Proc. of the 1996 IEEE/SICE/RSJ Int'l Conf. on Multisensor Fusion and Integration for Intelligent Systems, 1996 (Ex. 1009, "Yu").
[5] JP Patent Application Publication No. H3-151637, published June 27, 1991 (Ex. 1007, "Kowa"). Petitioner has provided a certified English translation. Ex. 1007, 13.

Techs., LLC v. Lee, No. 15-446, 2016 WL 3369425, at *12 (U.S. June 20, 2016) (concluding the broadest reasonable construction "regulation represents a reasonable exercise of the rulemaking authority that Congress delegated to the Patent Office"). Under that standard, claim terms are presumed to be given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). Further, "[t]he PTO should also consult the patent's prosecution history in proceedings in which the patent has been brought back to the agency for a second review." *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015). Moreover, the Board may not "construe claims during IPR so broadly that its constructions are unreasonable under general claim construction principles." *Id.*

Petitioner proposes a construction for "substantially flexible semiconductor [] substrate." Pet. 9–13. Patent Owner contends that Petitioner's proposed construction is irrelevant to this proceeding and that Petitioner has acknowledged that these claim terms are not determinative in this case. Prelim. Resp. 15–16. For purposes of this decision, we construe "substantially flexible semiconductor [] substrate" and discuss "low-stress dielectric." We determine that no other terms require express construction for this decision.

1. "substantially flexible semiconductor [] substrate"

Each of challenged independent claims 17, 84, 129, and 143 recites "substantially flexible semiconductor [] substrate." The term "substantially flexible" is a term of degree that lacks clear meaning absent context because the words "substantially flexible" do not provide any measure to compare against prior art and potentially infringing substrates. *See Playtex Prods., Inc. v. Procter & Gamble Co.*, 400 F.3d 901, 908 (Fed. Cir. 2005) ("'Substantially flattened surface' is clearly a comparative term. Comparison requires a reference point. Therefore, to flatten something, one must flatten it with respect to either itself or some other object.").

Petitioner urges that in light of the intrinsic record, the broadest reasonable construction of "substantially flexible [] semiconductor substrate" is "a semiconductor substrate that has been thinned to a thickness of less than 50 μm and subsequently polished or smoothed." Pet. 9.

Petitioner argues that the Patent Owner, acted as its own lexicographer in defining "substantially flexible" in the written description of the challenged patent when ""substantially flexible" is used to describe a semiconductor substrate or how to make a substantially flexible substrate:

> Grind the backside . . . of the second circuit substrate to a thickness of less than 50 μm and then polish or smooth the surface. The thinned substrate is now a substantially flexible substrate.

Pet. 10 (citing Ex. 1001, 9:3–6; *see also id.* at 3:5–8, 4:20–24).

Petitioner further argues that Patent Owner (then, Applicant) confirmed this definition during prosecution of related patents and applications. For example, during prosecution of related U.S. Patent No. 8,907,499 ("the '499 patent"), the Examiner objected to certain claims

as indefinite for including the term "substantially flexible." Pet. 10 (citing Ex. 1018, 4). Petitioner notes that Applicant overcame the objection by arguing that "substantially flexible" is unambiguous because it is "clearly explained in the specification." *Id.* at 10–11 (citing Ex. 1019, 9; Ex. 1020, 18:1–3 (Portion of the Application that issued as the '499 patent corresponding to Ex. 1001, 9:3–6). Thus, according to Petitioner, Applicant clearly and unmistakably set forth a definition of the term "substantially flexible" when used to modify semiconductor substrate and Applicant expressed an intent to define the term. *Id.* at 11.

On this record, we agree in large part with Petitioner's proposed construction. Looking to the Specification, however, we note that the Summary of the Invention section in the challenged patent does not limit the meaning of a "substantially flexible substrate" to those substrates that have been polished. More specifically, the challenged patent teaches *"[t]hinning of the memory circuit to less than about 50 µm in thickness forming a substantially flexible substrate* with planar processed bond surfaces and bonding the circuit to the circuit stack while still in wafer substrate form." Ex. 1001, 3:5–8 (emphasis added). In other words, the Specification does not require polishing for "forming a substantially flexible substrate." *Id.* Moreover, we note that claim 17 recites "a substantially flexible semiconductor second substrate having topside and bottom-side surfaces . . . wherein the bottom-side surface of the second substrate is formed by removing semiconductor material from the second substrate and is smoothed or polished after removal of the semiconductor material." Thus, a construction of "substantially flexible semiconductor substrate" that includes

polishing effectively would read "is . . . polished after removal of the semiconductor material" out of claim 17. *See Stumbo v. Eastman Outdoors, Inc.*, 508 F.3d 1358, 1362 (Fed. Cir. 2007) (rejecting claim constructions that render phrases in claims superfluous).

Accordingly, given the claim language and statements in the Specification and considering the prosecution history for a related patent, we preliminarily construe "substrate is substantially flexible" as "a semiconductor substrate that has been thinned to a thickness of less than 50 μm." *Cf. Microsoft*, 789 F.3d at 1298 ("The PTO should also consult the patent's prosecution history in proceedings in which the patent has been brought back to the agency for a second review.").

Claim constructions may change as a result of the record developing during trial. We note, for example, that Patent Owner has not yet filed its response under 37 C.F.R. § 42.120 or any new testimonial evidence.

2. "low-stress dielectric"

The parties do not propose express constructions for the term "low-stress dielectric." Pet. 9–13; Prelim. Resp. 16 ("Patent Owner submits that the challenged claims should be given their plain and ordinary meaning for the purposes of this proceeding."); *see generally* Prelim. Resp. 15–16.

Petitioner, however, presents separate theories of unpatentability based on alternative constructions of the term "low-stress dielectric." Pet. 57–58. Specifically, for Petitioner's challenges based on Leedy '695, the Petitioner relies on Leedy '695 as disclosing the recited "low stress dielectric." *See, e.g.*, Pet. 30. Separately, Petitioner's obviousness challenge based on Kowa, however, relies on a different construction of "low-stress

dielectric" that requires stress-balancing multiple dielectrics. *Id.* at 57–58. Petitioner presents its obviousness challenge based on Kowa as an additional ground of unpatentability based on a possible claim construction by Patent Owner. *Id.* at 57. Prelim. Resp. 57–58.

Each of challenged independent claims 17, 84, and 129 recites "low-stress silicon-based dielectric material having a stress of $5x10^8$ dynes/cm^2 tensile or less." Similarly, challenged dependent claim 145 recites "low-stress dielectric material . . . having a stress of $5x10^8$ dynes/cm^2 tensile or less." Challenged dependent claim 145 depends from disclaimed independent claim 143, and challenged claims 146 and 145 each indirectly or directly depends from challenged dependent claim 145. Thus, each of the challenged claims requires "low-stress dielectric material" "having a stress of $5x10^8$ dynes/cm^2 tensile or less."

Also, we understand "low-stress [] dielectric material" to be a term of degree. We note, however, that each challenged claim modifies "low-stress [] dielectric material" with "having a stress of $5x10^8$ dynes/cm^2 tensile or less." Thus, at this preliminary juncture, we need not construe expressly "low- stress dielectric."

B. Asserted Ground of Obviousness over Bertin '754, Poole, and Leedy '695

Petitioner contends that claims 17, 18, 22, 84, 95, 129–132, 145, 146, and 152 of the challenged patent are unpatentable under 35 U.S.C. § 103 as obvious over Bertin '754, Poole, and Leedy '695. Pet. 17–43. Petitioner supports its contentions with citations to the references and with declaration

testimony of Paul D. Franzon, Ph.D. (Ex. 1002). *Id*. Patent Owner opposes. *See, e.g.*, Prelim. Resp. 2–4, 16–50.

A claim is unpatentable as obvious "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103. "In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")).

1. Summary of Bertin '754

Bertin '754 is a United States Patent that describes an improvement to a known multichip package as shown in its "prior art" Figure 1, reproduced below.

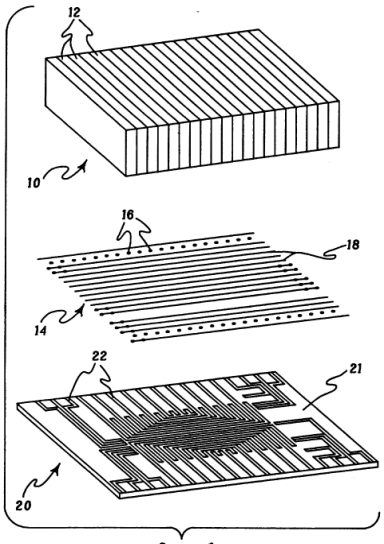


fig. 1
(PRIOR ART)

Bertin '754's Figure 1 is an exploded perspective view of a basic prior art multichip package. Ex. 1004, 2:43–44.

Bertin '754 describes "[a] fabrication method and resultant three-dimensional multichip package having a densely stacked array of semiconductor chips." *Id.* at Abstract. Figure 3a is reproduced below.

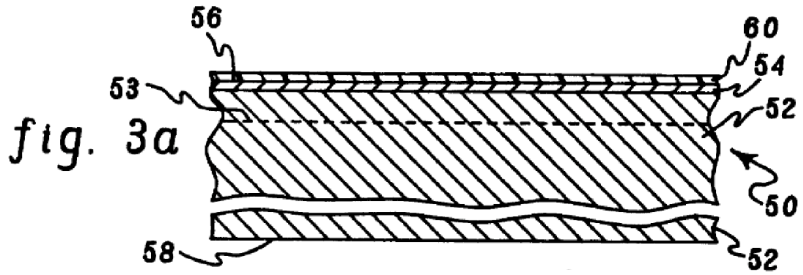


fig. 3a

Figure 3a depicts semiconductor device 50 having substrate 52 and active layer 54. *Id.* at 3:50–52. Layer 54 is adjacent to a first, upper planar surface 56 of device 50. *Id.* at 3:57–58. A second, lower planar surface 58 of stacked chip 50 is positioned substantially parallel to first planar surface 56. *Id.* at 3:59–60. Stacked chip 50 includes a semiconductor "substrate 52" (*id.* at 3:50–4:3), which is thinned to 20 μm or less (*id.* at 3:25–46, 5:10–22).

Bertin ’754 further teaches that “dielectric layer 60, for example, SiO_2, is grown over active layer 54 of device 50.” Ex. 1004, 3:60–62, Fig. 3a. Additionally, Bertin ’754 teaches that the multichip package includes vertical electrical interconnections (e.g., metallized trenches) that pass completely through substrates 52. *Id.* at Abstract, 1:62–2:12, 4:11–52, Figs. 3c, 3b, 3e, 3g.

2. Summary of Poole

Poole is a United States Patent that describes techniques for making thinned charge-coupled devices, which are thinned to allow illumination of the backside of the device to improve quantum efficiency and UV spectral response. Ex. 1005, Abstract, 1:8–11. More specifically, Poole describes a two-step method for thinning the backside of a silicon semiconductor substrate that includes integrated circuitry previously formed on the front side. *Id.* at Abstract, 1:7–18, 3:12–6. First, “[t]he bulk silicon is thinned to 75 μm with a 700 micro-grit aluminum oxide abrasive” (*id.* at 3:21–25; *see also id.* at Abstract, 3:33–34, 5:60–6:35), and “is then thinned and polished to 10 μm using 80 nm grit colloidal silica” (*id.* at 3:21–25; *see also id.* at Abstract, 3:33–34, 6:37–46). The result is a surface “almost totally free of work damage.” *Id.* at 5:64–65; *see also id.* at 3:44–46.

3. Summary of Leedy ’695

Leedy ’695 is a United States Patent that relates to the fabrication of integrated circuits and interconnect metallization structures from membranes of dielectric and semiconductor materials. Ex. 1006, 1:38–41. In its Abstract, Leedy ’695 indicates that the disclosed integrated circuits are fabricated from flexible membranes “formed of very thin low stress

dielectric materials, such as silicon dioxide or silicon nitride, and semiconductor layers." *Id.* at Abstract. Leedy '695 also discloses forming a "tensile low stress dielectric membrane" on a semiconductor layer as part of its integrated circuit structure. *Id.* at 1:53–58. Leedy '695 defines "[l]ow stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8 x 10^8 dynes/cm^2 (preferably 1 x 10^7 dynes/cm^2) in tension." *Id.* at 11:33–37. Additionally, Leedy '695 discloses two chemical vapor deposition (CVD) process recipes for manufacturing "structurally enhanced low stress dielectric circuit membranes." *Id.* at 11:51–65.

Referring to Figure 8, Leedy '695 discloses a three dimensional circuit membrane. *Id.* at 4:43. Figure 8 is reproduced below.

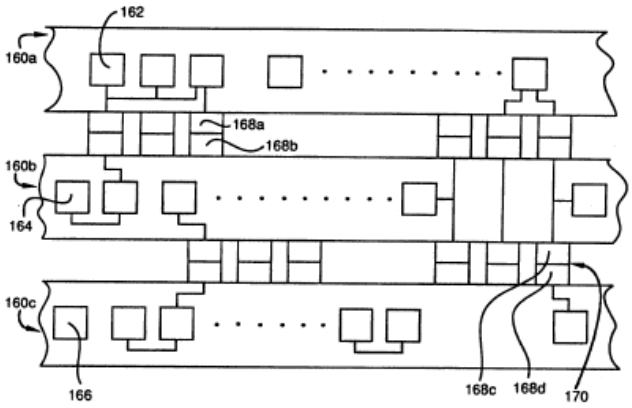


Fig_8

Figure 8 shows the vertical bonding of two or more circuit membranes to form a three dimensional circuit structure. *Id.* at 16:38–40. Interconnection between circuit membranes 160a, 160b, 160c including SDs 162, 164, 166 is by compression bonding of circuit membrane surface electrodes 168a, 168b, 168c, 168d (pads). *Id.* at 16:40–43. Bonding 170 between MDI circuit membranes is achieved by aligning bond pads 168c, 168d (typically between

4 μm and 25 μm in diameter) on the surface of two circuit membranes 160b, 160c and using a mechanical or gas pressure source to press bond pads 168c, 168d together. *Id.* at 16:43–49.

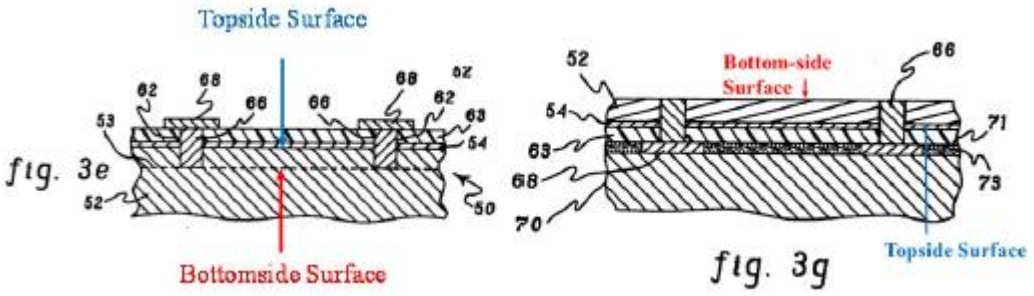
4. Petitioner's Contentions

Petitioner, with support of its declarant, Dr. Franzon, provides analysis purporting to explain how the combination of Bertin '754, Poole, and Leedy '695 would have conveyed to one of ordinary skill in the art the limitations recited in claims 17, 18, 22, 84, 95, 129–132, 145, 146, and 152. Pet. 17–43. Also with support of Dr. Franzon, Petitioner provides reasons why one of ordinary skill in the art would have combined the teachings of the references. *See, e.g., id.* at 17–23.

a. Limitations Recited in Independent Claim 17

Turning first to the limitations recited in the challenged claims, Petitioner relies on Bertin '754 for describing most of the limitations recited in the challenged claims. *Id.* at 17 ("Bertin teaches or suggests all but a few features recited in the Challenged Claims, as construed by Petitioner."). For example, regarding independent claim 17, Petitioner relies on one of the stacked chips of Bertin '754's "three-dimensional multichip package having a densely stacked array of semiconductor chips" as the recited "a first substrate having topside and bottomside surfaces, wherein the topside surface of the first substrate supports interconnect contacts." *Id.* at 23–24 (quoting Ex. 1004, 1:10–15). Petitioner provides the following annotated figures from Bertin '754 to explain its combination. *Id.* at 24 (depicting annotations of Bertin '754's Figs. 3e, 3f and noting that Fig. 3f depicts a

"flipped over" chip).



Petitioner indicates that Bertin '754's substrate 52 has top-side and bottom-side surfaces as shown in Figs. 3e and 3f. *Id.*

Petitioner relies on a combination of Bertin '754, Leedy '695, and Poole for conveying to one of ordinary skill in the art the recited "second substrate." *Id.* at 24–29. In particular, Petitioner relies on another one of Bertin '754's stacked chips 50 for most of the "second substrate" limitations. *Id.* Petitioner relies upon Poole's description of a two-step thinning process, which includes a grinding (or lapping) step followed by a chemical mechanical polishing ("CMP") step: "The bulk silicon is thinned to 75 µm with a 700 micro-grit aluminum oxide abrasive and is then thinned and polished to 10 µm using 80 nm grit colloidal silica." *Id.* at 26–27 (citing Ex. 1005 at 3:19−25, *see also id.* at Abstract, 3:12−47, 4:21−25, 5:60−7:2, 7:51−68, 8:21−24).

For the dielectric conforming to the stress limitation (5 x 10^8 dynes/cm^2) required by independent claim 17, Petitioner relies on Leedy '695. *Id.* at 30. Petitioner indicates that Leedy '695 describes forming a "tensile low stress dielectric membrane" on a semiconductor layer as part of its integrated circuit structure. *Id.* at 15 (quoting Ex. 1006, Abstract; *see also id.* at 1:53–58). Petitioner further contends that

Leedy '695 teaches that "[t]he dielectric may be 'silicon dioxide' or 'silicon nitride' deposited with a stress of 'less than 8 x 10^8 dynes/cm^2.'" *Id.* (citing Ex. 1006, 11:33–37 (stating "[l]ow stress . . . relative to the silicon dioxide and silicon nitride deposition made with the Novellus equipment as being less than 8 x 10^8 dynes/cm^2 (preferably 1 x 10^7 dynes/cm^2) in tension"); *see* Ex. 1006, 1:53–58, 2:40–45, 3:9–11, 7:1–9:63, 9:28–31, 11:25–65, 47:46–51, 48:45–50).

In noting that Bertin '754 describes stacked chips each having through-silicon metal interconnects insulated by oxidized sidewalls (Ex. 1004 at 3:60–62, 4:30–33), Petitioner acknowledges that Bertin '754 does not disclose explicitly that the interconnect insulator constitutes a "low-stress" dielectric characterized by a stress of about 5 × 10^8 dynes/cm^2 or less, as recited in claim 17. *Id.* at 30. For a dielectric of the tensile stress required by independent claim 17, Petitioner relies on Leedy '695's description. For further support of its position, Petitioner points to an Examiner's finding that the combination of Bertin '754 and Leedy '695 teaches or suggests these features. *Id.* at 16 (citing Exs. 1033–1036). The Examiner's finding was made during prosecution of applications related to the challenged patent. *Id.* The Applicant later expressly abandoned those applications. *Id.*

b. Rationale for Combining Bertin '754, Leedy '695, and Poole

As described above, Petitioner contends that it would have been obvious at the time of the invention (i) to substitute a dielectric described conforming to the stress limitation (5 x 10^8 dynes/cm^2) by Leedy '695 in place of the dielectric used in a conventional silicon substrate stacked

integrated circuit ("IC")[6] described by Bertin '754 and (ii) to modify the techniques described in Bertin '754 by replacing its well-known wet etching process with the two-step process described in Poole. *Id.* at 17–23.

When an obviousness determination relies on the combination of two or more references, as here, there must be some suggestion or motivation to combine the references. *WMS Gaming, Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1355 (Fed. Cir. 1999); s*ee also Dome Patent L.P. v. Lee*, 799 F.3d 1372, 1380 (Fed. Cir. 2015) ("If all elements of a claim are found in the prior art, as is the case here, the factfinder must further consider the factual questions of whether a person of ordinary skill in the art would be motivated to combine those references, and whether in making that combination, a person of ordinary skill would have had a reasonable expectation of success."). It is axiomatic that that an asserted ground of obviousness must demonstrate articulated reasoning with rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *see KSR Int'l v. Teleflex Inc.,* 550 U.S. 398, 418 (2007) (quoting *In re Kahn*). Mere conclusory statements are not sufficient. *In re Kahn*, 441 F.3d at 988. Furthermore, "[c]are must be taken to avoid hindsight reconstruction by using 'the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit.'" *Grain Processing Corp. v. Am. Maize-Prods. Co.*, 840 F.2d 902, 907 (Fed. Cir. 1988) (quoting *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1012 (Fed. Cir. 1983)).

[6] Ex.1002 ¶ 17 (indicating an abbreviation for integrated circuit is "IC").

With support of Dr. Franzon, Petitioner provides reasons why one of ordinary skill in the art would have combined the teachings of the references. *See, e.g., id.* at 17–23. For example regarding the combination of Leedy '695 and Bertin '754, Petitioner contends, with support of Dr. Franzon, that Leedy '695 provides express motivations for modifying Bertin '754's processes and device to incorporate Leedy '695's low tensile stress dielectric material. Pet. 18–19 (citing Ex. 1002 ¶¶ 98–99). Petitioner indicates Leedy '695 describes that low tensile stress is important because otherwise "surface flatness and membrane structural integrity will in many cases be inadequate for subsequent device fabrication steps or the ability to form a sufficiently durable free standing membrane." *Id.* at 18 (citing Ex. 1006 at 5:63–6:5; Ex. 1002 ¶ 98). Petitioner also indicates Leedy '695 explains that such dielectrics advantageously have lower stress than thermally grown oxides, like those used in Bertin '754. *Id.* at 19 (citing Ex. 1006 at 6:30–33).

Petitioner further reasons, with support of Dr. Franzon, that given Leedy '695's explanation that such dielectrics are versatile, in that they are able "to withstand a wide range of IC processing techniques and processing temperatures (of at least 400° C.) without noticeable deficiency in performance (Ex. 1006 at 2:37-40; *see also id.* at 1:50–52, 5:32–33), one of ordinary skill in the art would have expected success combining the teachings of Bertin and Leedy '695." *Id*. at 19–20 (citing Ex. 1002 ¶¶ 99–102).

Regarding the combination of Poole with Bertin '754, Petitioner contends, again with the support of Dr. Franzon, that it would have been

obvious to modify Bertin '754 to replace its wet etching process with Poole's two-step thinning process for several reasons. *Id.* at 20–21 (citing Ex. 1002 ¶¶ 87–80, 112, 17b). For example, both Bertin '754 and Poole generally relate to processing of semiconductor circuit substrates. *Id.* at 21 (citing Ex. 1004, Abstract, 1:55–2:31; Ex. 1005, Abstract, 3:12–25; Ex. 1002 ¶ 112, 17b). In addition, both Bertin '754 and Poole address a similar need—a process by which a silicon circuit substrate is thinned from the backside to less than about 20 μm with a resulting surface that is planar and has minimal defects. *Id.* (citing Ex. 1004, 3:25–46, 3:57–60, 4:4–10; Ex. 1005, Abstract, 2:15–24, 2:35–45, 2:55–58, 3:20–25; Ex. 1002 ¶ 112, 17b).

Relying on Dr. Franzon, Petitioner notes that Poole's two-step thinning process results in a substrate with a thickness of 10 μm, which falls within the "5–20 micrometers range" desired in Bertin '754. *Id.* (citing Ex. 1004, 3:35–38). Poole's two-step thinning process also results in a planar surface with a roughness that is "extremely low, in the low tens of Å." *Id.* (citing Ex. 1005, 6:68–7:2; *see also* 3:44–46). Therefore, according to Petitioner with support of Dr. Franzon, Poole's two-step thinning process achieves the predictable result of a thin substrate with a planar surface having minimal defects, which is desired in Bertin '754 to facilitate the formation of reliable vertical interconnects and bonds between substrates. *Id.* at 21–22 (citing Ex. 1002 ¶ 112; *KSR*, 550 U.S. at 415–421).

Continuing to rely on Dr. Franzon, Petitioner notes that in addition to wet etching, like that described in Bertin '754, there were only a handful of known methods for thinning semiconductor substrates recognized in the

semiconductor processing community at the time of the alleged invention. *Id.* at 22 (citing Ex. 1002 ¶ 112). According to Petitioner, one of those well-known methods is grinding (or lapping) and chemical mechanical processing ("CMP"), like that described in Poole. *Id.* Petitioner continues by asserting that, because there were only a few available primary methods for thinning semiconductor substrates and all of those primary methods provided the predictable result of a thin substrate, it would have been obvious to try Poole's two-step thinning process in place of Bertin '754's wet etching process with a reasonable expectation of success. *Id.* (citing *KSR*, 550 U.S. at 415–421).

5. Patent Owner's Contentions

In response, Patent Owner contends that there is not a reasonable likelihood that Petitioner's proposed combination would have rendered obvious claims 17, 18, 22, 84, 95, 129–132, 145, 146, and 152.

First, Patent Owner contends that Petitioner's reasons for making Petitioner's proposed dielectric substitution "gloss over" technical details and do not address technical reasons that would dissuade one of ordinary skill in the art form combining Leedy '695 with Bertin '754 in the manner proposed by Petitioner. Prelim. Resp. 16–34, 46–47. Patent Owner argues that semiconductor fabrication development is complex and unpredictable, and that one of ordinary skill cannot simply substitute one dielectric with another dielectric and have a reasonable expectation of success. Id. at 2–4, 16–34, 44–45.

Second, Patent Owner further contends that one of ordinary skill in the art would not have had reason to combine Leedy '695 with Bertin '754

because (i) Leedy '695 provides a solution to a problem that does not exist in conventional integrated circuits such as Bertin '754 (*id.* at 29–30), (ii) Leedy '695 lacks critical information regarding its dielectric (*id.* at 30–31), (iii) the prior art teaches away from Petitioner's combination involving the use of Leedy '695's "unconventional" tensile dielectrics (*id.* at 32–33), (iv) the benefits identified in Leedy '695 on which Petitioner's relied do not relate to low tensile stress dielectrics, and Petitioner allegedly mischaracterizes the benefits Leedy '695 would provide (*id.* at 33–34, 39–44), and (v) Petitioners do not identify a need or problem in Bertin '754 (*id.* at 38–39).

For support of these arguments, Patent Owner relies on a declaration from Dr. Alain Harrus indicates that it was "unconventional" for customers of Novellus to request low tensile stress dielectrics. *Id.* at 32–33 (citing Ex. 2137, 3). In addition to the Harrus declaration, Patent Owner relies on citations to a 600-page book describing fabricating integrated circuits. *Id.* at 18, 30–31 (citing Ex. 1040[7]). Patent Owner also relies on a 1995 journal article noting that with the chemical vapor deposition process PECVD "film properties degrade at lower power; e.g., film stress becomes tensile" as teaching away from using tensile dielectrics. *Id.* at 32 (citing Ex. 2133,[8] 447).

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[7] Wolf, et al., *Silicon Processing for the VLSI Era, Volume I – Process Technology*, Lattice Press, 1986 (Ex. 1040, "Wolf").

[8] Cote, et al., "Low-temperature chemical vapor deposition processes and dielectrics for microelectronic circuit manufacturing at IBM," *IBM Journal of Research Developments*, 437–464 July 1995 (Ex. 2133).

Third, Patent Owner argues that Petitioner does not meet its burden to show that it would have been obvious to combine Bertin '754 and Poole. *Id.* at 47–49. In particular, Patent Owner argues that Petitioner does not identify a problem in Bertin '754's etch. *Id.* at 47–48; *see, e.g., id.* at 48 ("Specifically, Petitioners do not direct the Board to statements in Berlin with respect to the sufficiency or insufficiency of the wet etch process described therein."). In addition, Patent Owner contends Petitioner does not explain adequately how the method described in Bertin '754 would work with Poole's specific device or that Poole's process would work in Bertin '754. *Id.* at 48–49.

6. Analysis

On the present record and for purposes of institution, we determine that Petitioner has made a sufficient showing that the combination of Bertin '754, Poole, and Leedy '695 would have conveyed to one of ordinary skill in the art the limitations of independent claim 17. As described in detail previously (*see* Petitioner's Contentions), Petitioner has described sufficiently its proposed combination, with citations to the references and supported by declaration testimony of Dr. Franzon.

Regarding Petitioner's proffered rationale for combining the references in the manner proposed by Petitioner and Patent Owner's

challenge of the purported rationale, we recognize that Patent Owner has not yet had an opportunity to submit new testimonial evidence.[9]

After weighing Patent Owner's arguments and evidence as currently developed in its Preliminary Response against the Petition with its citations to declaration testimony of Dr. Franzon, we determine that, based on the current record and for the purposes of institution, Petitioner has explained sufficiently with the support of Dr. Franzon that one of ordinary skill in the art would have understood that it would be beneficial to make the proffered substitution of Leedy '695's dielectric for Bertin '754's dielectric. Pet. 17–23 (citing Ex. 1002). *See, e.g., Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding the Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so"); *In re Am. Acad. of Sci. Tech Ctr*., 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.").

Moreover, we do not agree with Patent Owner's arguments that Petitioners do not identify a need or problem in Bertin. An obviousness analysis does not require the prior art references themselves to explicitly state a reason (including identifying a need or problem) for the combination of the disclosed teachings. A reason to combine teachings from the prior art "may be found in explicit or implicit teachings within the references

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[9] *See* 37 C.F.R. § 42.107(c) (July 1, 2013) ("The preliminary response shall not present new testimony evidence beyond that already of record, except as authorized by the Board.").

themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved." *WMS Gaming*, 184 F.3d at 1355 (citing *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998)); *see also KSR*, 550 U.S. at 419 ("[t]he obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents.").

Furthermore, on the present record, we do not agree that a prior art journal article or the Harrus declaration teaches away from the combination of Bertin '754 and Leedy '695, as Patent Owner contends. A reference teaches away from a claimed invention if it criticizes, discredits, or otherwise discourages modifying the reference to arrive at the claimed invention. *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004).

The journal article discusses "[a]dvances in dielectric processes in 0.35-µm CMOS manufacturing and development" that have been implemented in manufacturing and development lines. Ex. 2133, 447. In a particular process, the article discusses degradation of film properties at lower power—"e.g., film stress becomes tensile." *Id*. Based on the current record, however, Patent Owner has not explained sufficiently how the process discussed in the article detracts from Leedy's express disclosure of using low stress dielectrics in conventional integrated circuits. *See* Ex. 1006, Abstract ("[T]he flexible membrane is used as support and electrical interconnect for conventional integrated circuit die bonded thereto . . . .").

Similarly, regarding Patent Owner's teaching away argument concerning the Harrus declaration, Patent Owner has not explained sufficiently how an "unconventional" customer request criticizes, discredits, or otherwise discourages the combination of Leedy '695 and Bertin '754's teachings. *See Fulton*, 391 F.3d at 1201.

We also disagree with Patent Owner's contention that Dr. Franzon's testimony, on which Petitioner relies, is insufficient for institution of an *inter partes* review. *Id.* at 44–45 (apparently referring to Ex. 1002 ¶¶ 99–102). Dr. Franzon's testimony includes numerous citations to prior art references, including Exhibits 1004, 1006, 1039, 1040. *See* Ex. 1002 ¶¶ 99–102.

For the foregoing reasons, we determine that Petitioner has provided adequate evidence to show a reasonable likelihood of prevailing in its assertions that at least one of claims 17, 18, 22, 84, 95, 129–132, 145, 146, and 152 would have been obvious over Bertin '754, Poole, and Leedy '695.

C. Asserted Ground of Obviousness over Bertin '754 and Poole

Petitioner contends that claims 143, 144, and 151 of the challenged patent are unpatentable under 35 U.S.C. § 103 as obvious over Bertin '754 and Poole. Pet. 44–46. As noted previously, Patent Owner has statutorily disclaimed claims 143, 144, and 151 (Ex. 2140). Accordingly, we need not consider this asserted ground of unpatentability. *See* 37 C.F.R. § 107(e).

D. Asserted Ground of Obviousness over Yu and Leedy '695

Petitioner contends that claims 17, 18, 22, 84, 95, 129–132, 143–146, 151, and 152 of the challenged patent are unpatentable under 35 U.S.C. § 103 as obvious over Yu and Leedy '695. Pet. 46–57. Petitioner supports

its contentions with citations to the references and with declaration testimony of Dr. Franzon (Ex. 1002). *Id*. Patent Owner opposes. Prelim. Resp. 50–59.

Because Patent Owner has statutorily disclaimed claims 143, 144, and 151 (Ex. 2140), we will not institute an *inter partes* review of claims 143, 144, and 151 over Yu and Leedy '695. *See* 37 C.F.R. § 107(e). Claim 145, however, depends from claim 144, which, in turn, depends from claim 143. Claim 145, therefore, requires require all the limitations recited in disclaimed claims 143 and 144. Similarly, claim 152 depends from disclaimed claim 151 and so requires all the limitations recited by that claim. Accordingly, we will include the limitations recited in disclaimed claims 143, 144, and 152 as necessary to our discussion of this asserted ground.

1. Summary of Yu

Yu describes a three-dimensional integrated circuit structure for implementing a real-time microvision system. Ex. 1009, 831–832. "The system consists of a number of 2D LSIs vertically stacked using 3D LSI technology. . . ." *Id.* at 832. Yu's Figure 1 is reproduced below.

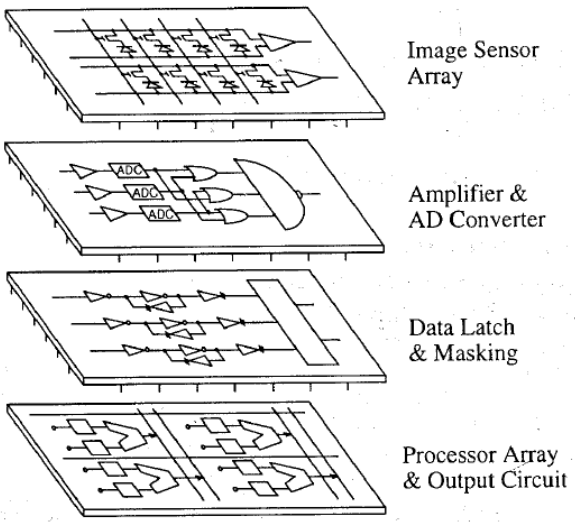

Figure 1: Basic concept of real-time microvision system with 3D integration structure

Figure 1 shows a basic concept of a real-time microvision system with a 3D integration structure.

In Yu's microvision system, substrates are ground and polished to thin the substrates to about 30 microns. *Id.* at 831–832 ("The Si substrate of the 2D-LSI which has the basic circuits is ground and polished to make thin wafer."); *id.* at Abstract ("In fabrication, grinding and chemical-mechanical polishing techniques are used to thin the wafer to 30 μm."). Wafers then are bonded together using a combination of conductive microbumps and a UV-hardening adhesive. *Id.* at 834–835 ("The thinned wafer is bonded to a thick wafer using In/Au micro-bumps with the minimum size of 5 μm x 5 μm and UV hardening adhesive layer with thickness of 1 μm by forcing the z direction pressure after careful wafer alignment."). The microbumps connect to buried interconnect structures that form vertical interconnects between vertically stacked circuitry. *Id.* at Fig. 8.

2. Analysis

Petitioner provides, with support of its declarant, analysis purporting to explain how the combination of Yu and Leedy '695 ("the Yu ground") would have conveyed to one of ordinary skill in the art the limitations recited in the challenged claims. *See* Pet. 46–57. Also with support of its declarant, Petitioner provides reasons why one of ordinary skill in the art would have combined the teachings of the references in the manner proposed by Petitioner. *See, e.g., id.* at 46–48.

In general, Petitioner relies on Yu's microvision system with a 3D integration structure as describing most of the limitations recited in the challenged claims. *Id.* at 46 ("Yu teaches or suggests all but a few of the features recited in the Challenged Claims."). For example, regarding independent claim 17, Petitioner relies on Yu's description of the "thick wafer" illustrated as the base wafer for disclosing the recited first substrate. *Id.* at 48. For the recited substantially flexible semiconductor substrate, Petitioner relies on Yu's "thinned wafer" that supports interconnect contacts, which (according to Petitioner) Yu refers to as "In/Au microbumps" on its topside surface. *Id.* at 49.

Petitioner acknowledges that Yu does not disclose expressly that "its dielectric is characterized by a tensile stress of about 5 x 10^8 dynes/cm^2 or less." *Id.* at 46. For that limitation and similarly to Petitioner's asserted ground of obviousness over Bertin '754, Poole, and Leedy '695 ("the Bertin '754 ground"), Petitioner relies on Leedy '695. *See, e.g., id.* at 46–48. Unlike the Bertin '754 ground that relies on Poole for describing polishing after removing semiconductor material, however, the Yu ground relies on Yu as teaching polishing (not Poole). *See, e.g., id.* at 17 (providing

an overview of the Bertin '754 ground), 46–47 (providing an overview of the Yu ground), 60 (describing differences between the Bertin '754 ground and the Yu ground); *see generally id.* at 17–43 (the Bertin '754 ground), 46–57 (the Yu ground).

Petitioner provides, with support of Dr. Franzon, several reasons to combine the Yu and Leedy '695 references, including (i) purported advantages indicated by Leedy '695 (*id.* at 47), (ii) reasonable expectation of success (*id.*), (iii) being in the same field and addressing the same problem of vertically integrating ICs (*id.* at 48), and (iv) involving the substitution of one known element for another to yield predictable results with known benefits (*id.*).

Patent Owner opposes, making many of the same types of arguments used to challenge the Bertin '754 ground. *See, e.g.*, Prelim. Resp. 1–5 (arguing the Petition as a whole fails to present a sufficient reason to combine the reference), 35–50 (arguing that the Bertin '754 does not render obvious the claims), 50–59 (arguing that the Yu ground does not render obvious the challenged claims). For example, Patent Owner argues "[a]s with Bertin, the crux of Petitioner's argument is that it would have been 'beneficial' to incorporate the low tensile stress dielectric disclosed by Leedy '695 into the Yu device." *Id.* at 50.

For substantially the same reasons as discussed above, we determine that Petitioner has provided adequate argument and evidence to show a reasonable likelihood of prevailing in its assertions that at least one of claims 17, 18, 22, 84, 95, 129–132, 145, 146, and 152 would have been obvious over Yu and Leedy '695.

E. Asserted Ground of Obviousness over Yu and Kowa

Petitioner contends that claims 17, 18, 22, 84, 95, 129–132, 143–146, 151, and 152 of the challenged patent are unpatentable under 35 U.S.C. § 103 as obvious over Yu and Kowa. Pet. 57–58. Petitioner explains that this asserted ground is presented in addition to its other asserted grounds and relies on a different construction of "low stress dielectric" that requires stress-balancing multiple dielectrics, which purportedly is taught in Kowa. *Id*. at 57.

Petitioner cursorily articulates this ground, which is asserted against fifteen claims (each depending from one of four independent claims), in four sentences. *See Id.* at 57–58. Petitioner provides a single sentence regarding its proposed combination, indicating that this ground "is identical to [the Yu ground] except that Leedy '695 is replaced with Kowa, resulting in a 3D multichip package that achieves a *net* stress of 5 x 10^8 dyne[s]/cm^2 tensile or less through stress balancing." *Id.* at 57–58 (citing Ex. 1007, 7–8, 10–11) (emphasis added). Regarding the requisite rationale to combine the references, Petitioner provides three sentences:

> *Kowa* teaches an alternative way to deal with stress to that of *Leedy '695*: by depositing films having alternating stress directions, a zero or very slightly tensile net stress can be achieved. Ex. 1007 at 10, Fig. 3; Ex. 1002 at ¶¶104-108. A person of skill would have been motivated to use the alternative taught in *Kowa* to manage stresses in *Yu*. Ex. 1002 at ¶¶109-110, 143-144. *Kowa* discloses controlling net stress to a zero or slightly tensile stress using stress balancing.

Id. at 58.

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")); *see also Intelligent Bio-Systems, Inc. v Illumina Cambridge Ltd*., No. 2015-1693, 2016 WL 2620512, at *6 (Fed. Cir. May 9, 2016) ("It was [Petitioner]'s burden to demonstrate both that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.") (internal quotation marks removed). The Board's rules further specify that a petition must include "[a] full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence" and "where each element of [each challenged] claim is found in the prior art patents or printed publications relied upon [and] the relevance of the evidence to the challenge raised." 37 C.F.R. §§ 42.22(a)(2), 42.104(b)(4), (5).

We determine that Petitioner has not met its burden to show with particularity why the challenged patent would have been obvious to one of ordinary skill in the art over Yu and Kowa. First, Petitioner has not explained sufficiently how the disclosure of Kowa regarding *net* stress teaches the recited limitation of "having a stress of 5 x 10^8 dynes/cm^2 tensile or less." *Id*. at 57. Second, Petitioner has not provided a sufficient articulated reasoning with rational underpinning to support its legal conclusion of obviousness. *KSR*, 550 U.S. at 418. Petitioner's statement

that "[a] person of skill would have been motivated to use the alternative taught in Kowa to manage stresses in Yu" (Pet. 58) is conclusory and, as such, is not sufficient. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (indicating "rejections on obviousness grounds cannot be sustained by mere conclusory statements").

Accordingly, we determine that the information in the Petition does not establish that there is a reasonable likelihood that Petitioner would prevail with respect to this asserted ground.

F. Prosecution of Related Patent Applications

Patent Owner also contends that we should deny the Petition under 35 U.S.C. § 325(d). Prelim. Resp. 12–16. Patent Owner urges this action because Petitioner's asserted grounds use some references considered by the Examiner during prosecution of related patents and, according to Patent Owner, Petitioner's asserted grounds raise similar issues to those considered during prosecution. *Id*. For example, Patent Owner contends that "[a]t most, the proposed Grounds swap out a previously considered primary reference for a new one allegedly disclosing the same thing." *Id.* at 12. Patent Owner also contends that Leedy '695 and Bertin '754 were considered by the Examiner during prosecution of a related patent application, but that the Examiner never raised the combination of Leedy '695 and Bertin '754. *Id.* at 14. Patent Owner seems to be arguing that, because the Examiner did not reject the pending claims in a related patent application during prosecution over the combination of Leedy '695 and Bertin '754, the Examiner did not consider the pending claims to be unpatentable over the combination of those references.

First, to the extent that Patent Owner is arguing we should give deference to earlier determinations of allowability because of the Examiner's "explicit consideration of the reference" Bertin '754 (*id.*), there is no presumption of validity as to the challenged claims in an *inter partes* review.[10] Furthermore, under 35 U.S.C. § 325(d), "[i]n determining whether to institute or order a proceeding under . . . chapter 31 [*Inter Partes* Review], the Director *may* take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office" (emphasis added). The permissive language of the statute indicates that we may consider a petition that presents the same prior art or arguments previously presented to the Office.

Moreover, Patent Owner argues that "[i]n the present Petition, Bertin and Yu are being cited for substantially the same facts as Sugiyama, then being combined with Leedy '695 in substantially the same way for substantially the same purpose of increasing structural integrity and durability in a stacked 3D IC device." *Id.* at 14. Even assuming that substantially the same art for substantially the same claims had been considered previously by the Office, we are not persuaded that all the issues presented by the Petitioner's combinations of (i) Bertin '754, Poole, and Leedy '695 and (ii) Yu and Leedy '695 have been considered previously by

[10] Whereas a patent is presumed "valid" unless overcome by clear and convincing evidence before a district court, a petitioner's burden in an *inter partes* review is to prove "unpatentability" by a preponderance of the evidence. *Compare* 35 U.S.C. § 282(a), *with* § 316(e).

the Office. We note, for example, that the Petition relies on testimony of Dr. Franzon (Ex. 1002), which was not before the Office previously.

Having considered the record before the Office during examination, as well as the parties' arguments and present record, we decline to exercise our discretion to deny the Petition based on the prosecution of a related patent application.

III. CONCLUSION

For the foregoing reasons, we determine that there is a reasonable likelihood that Petitioner would prevail in showing that at least one of claims 17, 18, 22, 84, 95, 129–132, 145, 146, and 152 of the challenged patent is unpatentable.

Any discussion of facts in this decision are made only for the purposes of institution and are not dispositive of any issue related to any ground on which we institute review. The Board has not made a final determination with respect to the patentability of any challenged claim. The Board's final determination will be based on the record as fully developed during trial.

IV. ORDER

After due consideration of the record before us, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the challenged patent is instituted on the following grounds of unpatentability asserted in the Petition:

Claims 17, 18, 22, 84, 95, 129–132, 145, 146, and 152 as unpatentable under 35 U.S.C. § 103 over Bertin '754, Poole, and Leedy '695; and

Claims 17, 18, 22, 84, 95, 129–132, 145, 146, and 152 as unpatentable under 35 U.S.C. § 103 over Yu and Leedy '695;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial commences on the entry date of this decision; and

FURTHER ORDERED that the trial is limited to the grounds identified above and no other ground set forth in the Petition as to any challenged claim is authorized.

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