Trials@uspto.gov
571-272-7822

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.,
Petitioner,

v.

ATI TECHNOLOGIES ULC,
Patent Owner

Case IPR2015-00326
Patent 6,897,871 B1

Before JONI Y. CHANG, BRIAN J. McNAMARA, and JAMES B. ARPIN, Administrative Patent Judges.

McNAMARA, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and
37 C.F.R. § 42.73

BACKGROUND

On July 10, 2015, we instituted an *inter partes* review of claims 1–3, 5, 6, 8–11, 13, 15, 17, 18, and 20 ("the challenged claims") of U.S. Patent No. 6,897,871 B1 (Ex. 1001, "the '871 Patent"). Paper 13 ("Dec. to Inst."). ATI Technologies ULC ("Patent Owner") filed a redacted and an un-redacted Patent Owner Response and a Motion to Seal. Papers 21, 20, and 19, respectively. LG Electronics, Inc. ("Petitioner") filed an Opposition to Patent Owner's Motion to Seal (Paper 25), Petitioner's own Motion to Seal (Paper 27), an un-redacted Reply, and a redacted Reply (Papers 28 and 29, respectively).[1] We authorized Patent Owner to file a Sur-Reply. Paper 32. Patent Owner filed duplicate Sur-Replies on February 9, 2016. Papers 36 and 37. Petitioner also filed a Motion to Exclude (Paper 41), which Patent Owner opposed (Paper 42), to which Petitioner replied (Paper 44). An oral hearing was conducted on April 6, 2016, and a transcript entered into the record. Paper 48 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6(c). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d). Having reviewed the arguments of the parties and the supporting evidence, we conclude that challenged claims 1–3, 5, 6, 8–11, 13, 15, 17, and 18 are unpatentable. Petitioner has not demonstrated that claim 20 is unpatentable.

[1] Unless otherwise noted, all references herein are to Petitioner's un-redacted Reply, Paper 28 ("Reply").

BACKGROUND AND RELATED PROCEEDINGS

In this proceeding, we instituted *inter partes* review on the following grounds:

Claims 1, 2, 5, 8, 10–11, 13, and 15 as anticipated under 35 U.S.C. § 102(e) by Lindholm;

Claims 3 and 6 as obvious under 35 U.S.C. § 103 over the combination of Lindholm and Open GL;

Claims 9, 17, and 18 as obvious under 35 U.S.C. § 103 over the combination of Lindholm and Kizhepat;

Claim 20 as obvious under 35 U.S.C. § 103 over the combination of Lindholm and Kurihara;

Claim 15 as obvious under 35 U.S.C. § 103 over Rich; and

Claim 20 as obvious under 35 U.S.C. § 103 over the combination of Rich and Kurihara.

During the oral hearing, Patent Owner conceded that, if it failed to antedate Lindholm, claims 1, 2, 5, 8, 10–11, 13, and 15 are unpatentable as anticipated by Lindholm, claims 3 and 6 are unpatentable as obvious under 35 U.S.C. § 103 over the combination of Lindholm and Open GL, and claims 9, 17, and 18 are unpatentable as obvious under 35 U.S.C. § 103 over the combination of Lindholm and Kizhepat. Ex. 2126, slide 2; Tr. 26 ("[T]he only basis for patentability with respect to grounds 1 through 3 is the antedating of Lindholm.").

All of the members of the panel in this proceeding participated in the oral hearing in related case IPR2015-00325, during which Patent Owner's arguments concerning antedating of Lindholm were heard. Tr. 5. Patent Owner relies the same evidence and substantially the same arguments in the present review and in IPR2015-00325 in support of its efforts to antedate Lindholm. *Compare, e.g.,*

IPR2015-00326, Paper 20, at v–x, 20–32 *with* IPR2015-00325, Paper 21, at v–x, 15–29. In the Final Written Decision in IPR2015-00325, the panel determined that Patent Owner had not antedated Lindholm. *LG Elecs., Inc. v. ATI Techs. ULC*, Case IPR2015-00325, slip op. at 12–53 (PTAB April 14, 2016) (Paper 62). In view of the determination that Patent Owner has not antedated Lindholm, and in view of Patent Owner's concession, we conclude that claims 1, 2, 5, 8, 10–11, 13, and 15 are unpatentable as anticipated by Lindholm, claims 3 and 6 are unpatentable as obvious under 35 U.S.C. § 103 over the combination of Lindholm and Open GL, and claims 9, 17, and 18 are unpatentable as obvious under 35 U.S.C. § 103 over the combination of Lindholm and Kizhepat.

The only matters remaining before this panel are whether claim 15 is obvious over Rich and whether claim 20 is obvious over the combination of Rich and Kurihara and the combination of Lindholm and Kurihara.

THE '871 PATENT

In computer graphics systems, a three-dimensional shape is represented by collection of simple polygons called "primitives." Ex. 1001, col. 1, ll. 11–12. Primitives are formed by the interconnection of individual pixels. *Id.* at col. 1, ll. 15–17. Color and texture are applied to the individual pixels that comprise the shape based on their location within the primitive and the primitive's orientation relative to the generated shape. *Id.* at col. 1, ll. 17–19.

A three-dimensional shape represented by a wireframe collection of primitives is transformed into colored images by two graphics-processing operations: (i) vertex operations and (ii) pixel operations. Prelim. Resp. 2 (citing Ex. 1001, col. 1, ll. 11–59). To orient the wireframe model as desired, matrix transformations applied to vertices Vx, Vy, Vz of the primitives generate new vertices Vx′ Vy′, Vz′, which then are translated into pixels to generate a rendered

object that can be displayed as a two-dimensional image. *Id.* at 3 (citing Ex. 1001, col. 1, ll. 36–49). Pixel operations performed on each pixel of the rendered object determine the pixel's color and appearance. *Id.* (citing Ex. 1001, col. 1, ll. 49–53).

Conventional graphics processors include "shaders" that specify how and with what corresponding attributes a final image is generated on a screen or other device. Ex. 1001, col. 1, ll. 24–27. Conventional graphics processors require both a vertex shader and a pixel shader to render an object. *Id.* at col. 1, ll. 61–62. A vertex shader accepts as inputs data representing the vertices Vx, Vy, Vz, applies the matrix transformation, and provides angularly-oriented vertices Vx′, Vy′, Vz′. A pixel shader operating at the pixel level provides the color value associated with each pixel of the rendered object. *Id.* at col. 1, ll. 50–54.

The '871 Patent employs a "unified shader" capable of performing both vertex operations and pixel operations. *Id.* at col. 2, ll. 37–39. A multiplexer receives vertex data at a first input, and pixel parameter data and attribute data from a rasterization engine at a second input. *Id.* at col. 3, ll. 60–65. In response to a control signal, an arbiter circuit selects one of a plurality of inputs for processing and a shader coupled to the arbiter performs vertex operations or pixel operations based on the selected one of the inputs. *Id.* at col. 2, ll. 40–49. A control signal generated by the arbiter determines which of the two multiplexer inputs is provided to the unified shader. *Id.* at col 3, l. 65–col. 4, l. 1. According to an arbitration scheme implemented in the arbiter, vertex data at the first input is transmitted to the unified shader if there are sufficient resources available in the unified shader to operate on the vertex data; otherwise interpolated pixel data on the second multiplexer input is passed to the unified shader. *Id.* at col. 4, ll. 2–8.

The unified shader includes a general purpose register for storing the plurality of selected inputs, a sequencer for storing logical and arithmetic

instructions used to perform vertex and pixel manipulation operations, and a processor capable of executing both floating point arithmetic and logical operations on the selected inputs according to the instructions stored in the sequencer. *Id.* at col. 2, ll. 50–57. According to the arbitration scheme, if the general purpose register in the unified shader does not have sufficient space to store incoming vertex data, the arbiter does not transmit the vertex data. *Id.* at col. 5, ll. 23–26. Instead, instructions for pixel calculation operations are carried out in the unified shader until enough registers become available to perform vertex operations. *Id.* at col. 5, ll. 27–33. When vertex data is transmitted to the unified shader, the resulting vertex data is transferred to a render back end block that converts the resulting vertex data to a format suitable for display. *Id*. at col. 5, ll. 54–59.

CHALLENGED CLAIMS

Claims 15 and 20, reproduced below, are the only claims remaining to be addressed in this Decision:

> 15. A unified shader, comprising:
>
> a general purpose register block for maintaining data;
>
> a processor unit; and
>
> a sequencer, coupled to the general purpose register block and the processor unit, the sequencer maintaining instructions operative to cause the processor unit to execute vertex calculation and pixel calculation operations on selected data maintained in the general purpose register block.
>
> 20. The shader of claim 15, wherein the processor unit executes vertex calculations while the pixel calculations are still in progress.

ANALYSIS OF PRIOR-ART CHALLENGES

Introduction

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." We resolve the question of obviousness on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art;[2] and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). In an obviousness analysis, some reason must be shown as to why a person of ordinary skill would have combined or modified the prior art to achieve the patented invention. *See Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008). A reason to combine or modify the prior art may be found explicitly or implicitly in market forces; design incentives; the "interrelated teachings of multiple patents"; "any need or problem known in the field of endeavor at the time of invention and addressed by the patent"; and the background knowledge, creativity, and common sense of the person of ordinary skill. *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324,

[2] Petitioner and Patent Owner rely on substantially similar assessments of the level of ordinary skill in the relevant art. Ex. 1003 ¶ 41; Ex. 2003 ¶ 30. Although the parties are critical of the experience level of each other's expert witness (PO Resp. 49, Reply 25), each of Petitioner's and Patent Owner's declarants appear to exceed the qualifications required for a person of ordinary skill in the relevant art (*see* Ex. 1003 ¶¶ 3–8; Ex. 2003 ¶¶ 6–17), and we credit their testimony as to the definition of a person of ordinary skill in the art.

132–9 (Fed. Cir. 2009) (quoting *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418–21 (2007)).

Claim 15 as Obvious over Rich

Claim 15, which is drawn to a unified shader, does not recite an arbiter or a selection function as described above. Petitioner argues that Rich discloses a processor memory and registers, an arithmetic logic unit (ALU) as the processor unit, and a processing element array control unit as the sequencer. Pet. 47, 49–50. Petitioner notes Rich discloses that during pixel processing, the pixel data is retrieved from the memory 34 and processed. *Id.* at 47 (citing Ex. 1005, col. 33, ll. 60–64). Petitioner acknowledges that Rich is silent regarding executing vertex calculation operations on the selected data maintained in the general purpose register block. *Id*. at 47; Ex. 1003, Declaration of Dr. Nader Bagherzadeh ("Bagherzadeh Decl.") ¶ 216. Petitioner also notes that, in Rich, databases containing vertex data may be loaded into video memory via interfaces or may reside in locally accessible memory, and pixel data may be stored and retrieved from local processor memory 34. Pet. 48 (citing Ex. 1005, col. 9, ll. 1–12). Thus, Petitioner contends it would have been obvious to a person of ordinary skill that vertex data could also be stored in local processor memory 34 and retrieved for subsequent processing, for example by modifying Rich to maintain or temporarily store both primitive and vertex data from a database in processor memory 34 for local access by the ALU to process and transform primitives and their vertices. *Id*. at 48. As a reason for this modification, Petitioner cites faster and more efficient access resulting from temporary storage of data just before processing operations would reduce stall time associated with directly accessing data from external memory. *Id.*

As to claim 15, Patent Owner contends that Petitioner's Rich-based grounds fail because Rich would not work for its intended purpose if vertex data were stored in an on-chip memory. PO Resp. 33. Patent Owner emphasizes that Rich's pipelined architecture stores vertex data (i.e., the transformed vertex data after the completion of vertex processing) in external memory to make the output of vertex-processing phase accessible to processing elements 32 during the pixel processing phase. *Id*. at 35. Patent Owner notes that, in Rich, processing element 32 that operates on a piece of data during the vertex processing phase is not necessarily the same processing element that operates on the data during the pixel-processing phase. *Id.*

Patent Owner states that both Rich and the system recited in claim 15 must address input-routing because these systems have a single type of computational resource that operates on two different types of inputs—vertex and pixel inputs that compete for access to the computation resource. *Id.* at 37. According to Patent Owner, the systems recited in claim 15 and Rich address this issue in different ways. *Id.* at 38. Patent Owner argues that the claimed sequencer maintains instructions for both vertex and pixel operations that allow the processor to work with the general purpose register block to execute the appropriate instructions on the appropriate data at the appropriate time. *Id*. Patent Owner contrasts this approach to that of Rich, in which vertex and pixel operations are performed in discrete phases, such that vertex data stored in external, shared memory is accessible for routing to appropriate processing element 32 for pixel processing. *Id.* Patent Owner asserts that this difference eliminates the need in Rich for a general purpose register block or sequencer, as claimed, and that if Rich were modified to store vertex data locally (e.g., in on-chip memory 34), its processing elements would not be able to access the transformed data efficiently,

meaning that Rich would not work for its intended purpose. *Id.* at 39–40. Patent Owner also argues that Rich "teaches away" because a person of ordinary skill would have understood that the Rich's external memory is a shared memory for all processing elements, whereas its on-chip memory 34 is dedicated to one processing element. *Id.* at 41–42. Patent Owner also disputes the testimony of Petitioner's expert that a person of ordinary skill would be motivated to store vertex data on chip for faster and more efficient access because Rich discloses that processing elements 32 have only a small amount of memory 34 in their own dedicated circuitry. *Id.* at 40–41.

Claim 15 recites a "unified shader," i.e., "a shader that is configured to perform both vertex and pixel operations" (Ex. 1001, col. 2, ll. 57–58), comprising a general purpose register block, a processor unit and sequencer coupled to both that maintains instructions to perform vertex calculation operations and pixel circulation operations on selected data maintained in the general purpose register block. The language of claim 15 does not limit the shader to one that follows any particular operational sequence; nor is claim 15 limited to a shader having an "on-chip" general purpose memory block.

Petitioner acknowledges that Rich does not disclose explicitly vertex processing on data retrieved from processor memory 34. Bagherzadeh Decl. ¶ 216. However, Petitioner cites a disclosure in Rich that suggests making vertex data locally accessible, thereby recognizing that Rich could be operated using local on-chip memory to store vertex data. Reply 17 (citing Ex. 1005, col. 9, ll. 1–12). Rich discloses that the image generation system accesses the database of primitives defining the image to be generated and assigns the primitives to processing elements 32 of processing element array 30 and that "the database may reside in memory accessible through the host processor 22 or locally accessible." Ex. 1005,

col. 9, ll. 3–7, 10–12. Processing elements 32 transform the primitives defined in model space to x, y coordinates or screen coordinates. *Id*. at col. 9, ll. 17–21. Thus, we agree with Petitioner that Rich suggests making vertex data locally accessible. In addition, although Rich also discloses external memory circuitry may be necessitated when processing elements 32 have only a small amount of memory 34, we credit the testimony of Petitioner's declarant, Dr. Bagherzadeh, that, at the time of the '871 Patent, it would have been within the ability of one of ordinary skill to add more memory to the processing elements and that the use of on-chip memory was well known and commonly used in the art of data processing for fast access. Reply 20 (citing Bagherzadeh Decl. ¶ 223).

Petitioner further argues that simply moving the vertex data to an on-chip memory would not render Rich's system inoperable. Reply 17. As Petitioner notes, one of ordinary skill seeking to gain faster access to vertex data would have had reason to trade off pixel processing efficiency, without rendering the system inoperable for its intended purpose. Thus, we conclude that Petitioner has demonstrated that a person of ordinary skill would have had reason to modify Rich to arrive at the subject matter broadly recited in claim 15.

Claim 20 as Obvious over Rich and Kurihara

Claim 20 further limits claim 15, reciting that "the processor unit executes vertex calculations while the pixel calculations are still in progress." Discussing the meaning of this limitation, Patent Owner explains that "[o]ne of the hallmarks of the unified shader is the ability to flexibly switch between vertex calculations and pixel calculations." Tr. 24–25. By way of example, Patent Owner explains that in a ten instruction thread, one may execute five pixel instructions (1–5), stop and execute the vertex calculations from another thread, and sometime later execute the remaining instructions (6–10) of the original thread. *Id*. at 23. Thus,

we understand Patent Owner to contend that claim 20 does not require the processor perform vertex and pixel calculations simultaneously, but that a processor have the ability to switch between vertex and pixel calculations as data is available. *Id.*; PO Resp. 45–46. Petitioner contends that this limitation would cover at least vertex and pixel calculations that are carried out simultaneously. Tr. 18; Pet. 58–59. In the absence of further definition in claim 20, we agree that this limitation would include switching between calculations or calculations that take place simultaneously.

Petitioner does not address whether it would have been obvious to one of ordinary skill to execute some instructions in one thread, pause execution of that thread, for example when data is not yet available, and execute instructions from another thread before returning to the first thread. Instead Petitioner contends that it would have been obvious in view of Rich and Kurihara to execute vertex and pixel calculations simultaneously. Pet. 58–59.

Petitioner acknowledges that Rich does not disclose explicitly that both vertex and pixel processing occur simultaneously, but notes that, because Rich allows parallel processing and sharing of data among processing elements, Rich provides for simultaneous processing of both vertex and pixel data. Pet. 58. Petitioner argues that Kurihara discloses a graphics data parallel processing system that determines the type of graphics data to be transferred to first-in, first-out ("FIFO") memories that send graphic data to respective processors for processing. *Id.* at 59. Noting that the system does not have to wait until all FIFO memories are emptied to transfer data, Petitioner argues that Kurihara allows for simultaneous processing of different types of graphics data. *Id.*

As a basis for its combination with Kurihara, Petitioner states that the advantages of simultaneously processing pixel and vertex data were known in the

art and that Rich discloses a number of parallel processing elements 32 allowing for simultaneous execution of various processing functions. Reply 21. Petitioner argues that it would have been known to one of ordinary skill to process pixel data in one of Rich's processing units 32 at the same time as processing vertex data in another of Rich's processing units 32, as taught by Kurihara. *Id.*

Patent Owner contends that Kurihara and Rich are incompatible because Rich's disclosure of vertex and pixel processing in discrete, *sequential* phases is the opposite of *simultaneously* performing different types of graphics operations, as disclosed in Kurihara. PO Resp. 43. Patent Owner also contends that even if the references could be combined, Kurihara does not suggest a single "processor unit" executes vertex calculations while pixel calculations are in progress. *Id*. a t 44–45. Patent Owner argues that, in claim 20, the single processor unit executes a first type of graphics processing operation, e.g., vertex processing, while a second type of graphics processing, e.g., pixel processing, is in progress by stalling one type of processing in order to perform the other type of processing. *Id.* at 45. According to Patent Owner, none of Kurihara's graphics processors can perform vertex calculations while pixel calculations are in progress. *Id.* at 46. Thus, Patent Owner's arguments incorporate two assumptions: (1) that claim 20 extends only to diverting processing resources to processing a different type of data, while processing a first type of data; and (2) that the processing unit in claim 20 is a single processor.

Petitioner responds that nothing in claim 20 limits the processing unit to a single processing element and that Kurihara's group of graphics processors corresponds to the processing unit recited in claim 20. Reply 22. Claim 20 recites a processor unit, but does limit the processor unit to a single computational or processing element. Although Patent Owner's declarant, Dr. Andrew Wolfe,

asserts that Kurihara concerns how information is loaded into FIFO memories and does not disclose features of the processor (Ex. 2003, Declaration of Dr. Andrew Wolfe ("Wolfe Decl.") ¶¶ 316–319), we note that claim 20 does not recite any specific features of the processor unit, other than that the processor unit executes vertex calculations while pixel calculations are still in progress.

As discussed above, Petitioner contends that claim 20 includes simultaneously processing vertex and pixel calculations. Patent Owner contends, however, that Kurihara does not disclose that feature. PO Resp. 46. Kurihara claims a graphic data parallel processing apparatus having "a plurality of processors for simultaneously processing graphic data and defining a corresponding graphic image" and for displaying the graphic image. Ex. 1007, col. 9, ll. 10–14 (claim 1). Claim 1 of Kurihara also recites "the graphic data for each graphic image being of first and second different types and of relatively and respectively larger and smaller quantities and requiring relatively and respectively smaller and greater processing times." *Id.* at col. 9, ll. 14–18. Although claim 1 of Kurihara recites a plurality of processors for simultaneously processing graphic data and first and second types of graphic data requiring different processing times, the claim does not recite explicitly processing the first and second data types at the same time.

Patent Owner contends that, in Kurihara, FIFO memories simultaneously transfer vertex or pixel data to graphics processors and each processor performs one type of graphics processing on the data type it receives. PO Resp. 44 (citing Ex. 1007, col. 4, ll. 56–65, col. 5, l. 37). Kurihara teaches that it was known in the art for graphics processors to process coordinate data independently by selecting an available FIFO memory according to half-full flags, but that, because attribute data must be transferred simultaneously through FIFO memories after all the FIFO half-

full flags were set to 0, it was necessary to wait until the slowest graphics processor is released from the half-full state. Ex. 1007, col. 2, ll. 49–66, Fig. 5. As a result, other processors would have no data to process resulting in wasted time. *Id.* at col. 2, l. 67–col. 3, l. 2.

Kurihara discloses that the graphics processors process data in parallel. Ex. 1007, col. 5, l. 37. However, Kurihara treats coordinate (vertex) and attribute (pixel) data differently. In Kurihara, controller 1 determines whether or not graphic data must be transferred to selected ones of the FIFO memories according to flags. *Id*. at col. 6, ll. 53–55. Controller 1 detects the type of data to be transferred and, based on flags set by data quantity detectors for each type of data, determines whether FIFO memories have free space to receive the coordinate or attribute data to be sent to the respective graphic processor. *Id.* at. col. 5, ll. 15–36; col. 8, ll. 19–26. Coordinate data is loaded into the FIFO memory if any one of the first flags is set to zero. *Id.* at col. 6, l. 56–61, col. 8, ll. 2–6, 31–34, Fig. 3. In contrast, attribute data is loaded into the FIFO only if all of the second flags are set to zero. *Id.* at col. 6, l. 61–col. 7, l. 3, col. 8, ll. 14–15, Fig. 3. In this way, Kurihara improves processing speed by reducing the suspension period in which no data are transferrable due to fluctuations in coordinate data (shape data). *Id.* at col. 8, l. 66–col. 9, l. 2. Separately processing coordinate data with the graphics processors, Kurihara minimizes processing periods in the graphics processing due to fluctuations in the quantities of coordinate data and quickly and simultaneously transfers attribute data to all of the graphic processors. *Id*. at col. 9, ll. 3–8.

Petitioner's declarant, Dr. Bagherzadeh, states that Kurihara discloses that the parallel processing system does not have to "wait until all of the FIFO memories 5 are emptied to transfer graphics data" and, based on this disclosure, he asserts "Kurihara's system therefore allows for the simultaneous processing of

different types of graphics data." Bagherzadeh Decl. ¶¶ 287–288 (citing Ex. 1007, col. 4, ll. 56–62). However, the text cited by Dr. Bagherzadeh concerns "simultaneously transferring the attribute data with only a short wait time to the FIFO memories 5 because the system does not wait until all of the FIFO memories 5 are emptied." Ex. 1007, col. 4, ll. 56–60 (emphasis added). As discussed above, Kurihara discloses transferring the coordinate data to a FIFO memory where the flag indicates space is available, but "[i]f any one of the FIFO memories 5 has insufficient space to receive the attribute data, the controller suspends the write operation until every one of the FIFO memories 5 has sufficient free space to receive the attribute data." *Id.* at col. 6, l. 67–col. 7, l. 3. Thus, although Kurihara discloses providing coordinate data to the FIFO memories as they become available, Kurihara does not disclose providing pixel data to the FIFO memories until they are all available. Kurihara further discloses that the attribute data is transferred from the FIFO memories to the graphics processors simultaneously. *Id.* at col 4, ll. 61–62, col. 9, ll. 5–8. The simultaneous transfer of attribute data to graphics the processors suggests that attribute processing occurs simultaneously, but does not provide any insight into whether coordinate processing and attribute processing occur simultaneously. Although the simultaneous transfer of attribute data to the processors does not necessarily preclude that vertex processing can proceed in one processor at the same time pixel processing takes place in another processor, Petitioner has not cited an adequate description of this feature in Kurihara.

In consideration of the above, we are unable to conclude that the subject matter cited by Petitioner demonstrates that Kurihara discloses executing vertex calculations and pixel calculations simultaneously.

Claim 20 as Obvious over Lindholm and Kurihara

As discussed above, in IPR2015-00325, we determined that claim 15 is unpatentable over Lindholm. Petitioner acknowledges that Lindholm does not disclose explicitly that both vertex and pixel processing occur simultaneously, and cites Kurihara as disclosing this feature. Pet. 36–37. For the reasons discussed above, Petitioner has not demonstrated that Kurihara discloses this limitation.

Secondary Considerations

Having determined that Petitioner has not established obviousness of claim 20 based on the prior art cited in its challenges, we limit our analysis of Patent Owner's secondary consideration arguments to claim 15. Patent Owner contends that the release of its Xenos chip, as the first commercially available unified shader, was a watershed event that overcame industry skepticism and resulted in a substantial change in the industry's approach to the architecture of graphics products. PO Resp. 47. Petitioner's Reply states that Patent Owner's expert, Dr. Wolfe, testified that claim 15 recites a specific type of unified shader and that Patent Owner failed to explain what claimed features it alleges the industry has embraced. Reply 22–23.

In its secondary consideration arguments, Patent Owner states only that the "hallmark of a unified shader is the ability to perform either vertex operations or pixel operations on inputs maintained in a shared repository." PO Resp. 46. Dr. Wolfe's testimony on behalf of Patent Owner discusses concerns that an architecture suitable for a pixel shader would result in hardware being idle most of the time during vertex shading, and that load balancing would be challenging in a unified shader. Wolfe Decl. ¶¶ 326–329. None of these features is recited in claim 15, nor does Dr. Wolfe connect the limitations of claim 15 to Patent Owner's purported success. Thus, we find that Patent Owner fails to establish the required

nexus between the merits of the claimed invention and the alleged evidence of secondary considerations. Accordingly, Patent Owner's objective evidence is accorded little weight. We conclude that, on balance, the evidence of obviousness outweighs the weak evidence of nonobviousness. *See Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007).

MOTION TO EXCLUDE

Petitioner's Motion to Exclude is similar to that filed in IPR2015-00325, in which Petitioner sought to exclude evidence concerning Patent Owner's efforts to antedate Lindholm and other references that are not part of this proceeding. In IPR2015-00325, having decided the issue concerning Lindholm in Petitioner's favor, we dismissed Petitioner's Motion to Exclude as moot. For the same reasons, we dismiss Petitioner's Motion to Exclude in this proceeding, as moot.

MOTIONS TO SEAL

Patent Owner moved to seal portions of its Patent Owner Response, the entirety of Exhibits 2007, 2009–2018, and 2020–2072, 2093–2118, portions of Dr. Wolfe's Declaration (Exhibit 2003), and the entirety of the Declarations of Calvin Watson and Laurent Lefebvre (Exhibits 2005 and 2006) on the basis that these exhibits and related argument in the Patent Owner Response contain confidential information concerning the development of Patent Owner's shader. Paper 19 ("Patent Owner's Motion to Seal"). Pending a ruling on Patent Owner's Motion to Seal, Petitioner moved to seal its Reply Brief and Exhibits 1013, 1015–1020, 1022, 1033–1041, and 1044. Paper 27 ("Petitioner's Motion to Seal").

We addressed similar issues in IPR2015-00325. In deciding Patent Owner's First and Second Motions to Seal in IPR2015-00325, we observed that our Final Written Decision addressed nearly all of the documents Patent Owner sought to seal. *LG Elec., Inc. v. ATI Tech. ULC*, Case IPR2015-00325, slip op. at 7 (PTAB

Apr. 14, 2016) (Paper 63) (denial of Patent Owner's Motion to Seal). Balancing the public interest in maintaining a complete and understandable record, we denied Patent Owner's Motion to Seal. *Id*. Although we authorized each party to file a motion to expunge certain documents within one week of our ruling, no such motions were filed.

The documents the parties seek to seal in this proceeding cover the same subject matter as that addressed in IPR2015-00325, and we reach the same conclusion. For that reason, we deny both Patent Owner's Motion to Seal and Petitioner's Motion to Seal.

CONCLUSION

Having determined in IPR2015-00325 that Patent Owner did not antedate Lindholm, we conclude that claims 1, 2, 5, 8, 10–11, 13, and 15 are unpatentable as anticipated by Lindholm, claims 3 and 6 are unpatentable as obvious under 35 U.S.C. § 103 over the combination of Lindholm and Open GL, and claims 9, 17, and 18 are unpatentable as obvious under 35 U.S.C. § 103 over the combination of Lindholm and Kizhepat.

For the reasons discussed above, we also conclude that Petitioner has demonstrated by a preponderance of the evidence that claim 15 is unpatentable as obvious under 35 U.S.C. § 103 over Rich.

However, Petitioner has not demonstrated that claim 20 is unpatentable over the combination of Rich and Kurihara or the combination of Lindholm and Kurihara.

We also dismiss as moot Petitioner's Motion to Exclude and deny all Motions to Seal.

ORDER

In consideration of the above, it is

ORDERED that claims 1–3, 5, 6, 8–11, 13, 15, 17, and 18 of the '871 Patent are unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is *dismissed* as moot;

FURTHER ORDERED that Patent Owner's Motion to Seal is *denied*;

FURTHER ORDERED that Petitioner's Motion to Seal is *denied*;

FURTHER ORDERED, that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

Robert G. Pluta
Bryan Nese
MAYER BROWN, LLP
rpluta@mayerbrown.com
bnese@mayerbrown.com

PATENT OWNER:

Jon E. Wright
Michael D. Specht
Michael B. Ray
Jonathan Tuminaro
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
jwright-PTAB@skgf.com
mspecht-PTAB@skgf.com
mray-PTAB@skgf.com
jtuminar-PTAB@skgf.com