UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION
Requester and Appellant

v.

NETLIST, INC.
Patent Owner and Respondent

Appeal 2013-009066
Inter partes Reexamination Control No. 95/001,381
United States Patent 7,532,537 B2
Technology Center 3900

Before JOHN A. JEFFERY, KEVIN F. TURNER, and STANLEY M. WEINBERG, *Administrative Patent Judges*.

DECISION ON REQUEST FOR REHEARING

Requester requests rehearing of our decision dated January 16, 2014 ("Dec."), where we affirmed the Examiner's final decision declining to reject claims 1-49, 51-55, 57-61, and 63 in the above-identified *inter partes* reexamination. Request for Rehearing filed Feb. 18, 2014 ("Req. Reh'g"). Patent Owner challenges the asserted basis for the request in comments filed March 19, 2014 ("Comments"). For the reasons noted in Patent Owner's comments as well as those below, we deny the request to modify our decision.

The Proposed New Matter Rejection

First, Requester asks that we reconsider our affirmance of the Examiner's decision declining to reject claims 1-23, 45-49, 51-55, 57-61, and 63 as failing to satisfy the written description requirement of § 112, first paragraph. Req. Reh'g 1-4. In our decision, we held that the negative limitation "DDR chip selects that are not CAS, RAS, or bank address signals" that was added to independent claims 1, 13, and 18 during reexamination prosecution was reasonably supported by the reexamined '537 patent's original disclosure and, therefore, was not new matter. Dec. 8-10. Specifically, we found that the original '537 patent disclosure reasonably conveys a reason to exclude the relevant limitations, namely in view of (1) consistency with JEDEC standards[1]; (2) the '537 patent's excluding RAS and CAS signals in Table 2; and (3) various other passages from the '537 patent cited by Patent Owner and the Examiner indicating that

[1] A JEDEC standard was cited along with other prior art references in our earlier decision on page 5. For brevity, we omit full citations to these references here.

chip selects are distinct from CAS, RAS, and bank address signals, and where the chip selects are DDR chip selects. Dec. 9-10 (citing *Santarus, Inc. v. Par Pharm., Inc.*, 694 F.3d 1344, 1351 (Fed. Cir. 2012)).

Requester contends that we erred in relying on the *first two* above-identified items as reasonably conveying a reason to exclude the relevant limitations, and that we did not identify any reason in the '537 patent for excluding bank address signals. Request 3-4. We find these arguments unpersuasive. Although we indicated that the '537 patent did not articulate *expressly* a reason to exclude RAS and CAS signals, we noted that they were nonetheless excluded from an embodiment in Table 2. Dec. 9. At a minimum, ordinarily skilled artisans would reasonably infer at least an *implicit* reason to exclude these signals based on their *explicit* exclusion in the context of the reference. *Accord* Comments 4 ("The specification of the '537 Patent expressly distinguishes the signals at issue as opposed to only a mere hint of – i.e., a 'reason for' – exclusion in *Santarus*. Even so, the record does indicate a 'reason for' the DDR chip select exclusion.").

Moreover, as Patent Owner indicates, Requester fails to address the *third* item noted on pages 9 and 10 of our decision, namely the various other passages from the '537 patent cited by Patent Owner and the Examiner indicating that chip selects are distinct from CAS, RAS, *and bank address signals*. Comments 2-4 (citing '537 patent, col. 16, ll. 62-66; col. 17, l. 47 – col. 18, l. 50). Accordingly, Requester has inaccurately suggested that we relied *only* on unarticulated reasons as support for the negative limitation. Req. Reh'g. 3. Patent Owner's reference to JEDEC standards and Dr. Sechen's unrebutted testimony that ordinarily skilled artisans would understand a DDR chip select to be exclusive of RAS, CAS, and bank

address signals only bolsters the identified support for the negative limitation in the '537 patent and reason for exclusion. *See* Comments 3-4 (citing Sechen Decl. ¶¶ 37-38).

Accordingly, we are unpersuaded that we misapprehended or overlooked those points in rendering our decision.

The Proposed Rejections Based on QBMA

Requester also seeks reconsideration of our affirmance of the Examiner's decision declining to reject (1) claims 1, 8, 13, 14, 16, 18-20, 24, 25, 30, 35, 36, 39, 41, 42, 45-49, 53-55, 58-61, and 63 over QBMA and Dell ("Issues 7 and 9"), and (2) claims 51, 52, and 57 over QBMA, Dell, and JEDEC ("Issue 10"). Req. Reh'g 4-6. In our decision, we held that QBMA and Dell collectively failed to teach or suggest that the system and physical memory domains are compatible with their respective numbers of chip selects with 2:1 ratio as recited in the independent claims. Dec. 18-20. We also held that Requester failed to rebut persuasively Patent Owner's position that other relied-upon signals in QBMA do not constitute "chip selects" as those address-based signals are understood in the art and evidenced by Dr. Sechen's explanation in this regard. Dec. 20 (citing Resp. Br. 16; Sechen Decl. ¶¶ 46-54).

Requester argues that Dr. Sechen's "unjustified assumption" in paragraph 49 of his declaration that QBMA's Bank Enable (BE) signal is a timing signal and not an "address" or "chip select" signal purportedly caused us to misapprehend the references' applicability to a key claim limitation. Request 4-6. We find this contention unavailing. First, as Patent Owner indicates, this argument was not raised previously on appeal. Comments 5

("Appellant's multi-page argument as to the 'ENABLE' and 'BE CLK' signals was *never* raised by Appellant in its appeal briefs to the Board. . . . These signals were not even mentioned in Appellant's appeal briefs."). Comments 5 (citing App. Br. 23-26; Reb. Br. 7-8) (emphasis in original). Rather, Requester's arguments in the briefs regarding Issues 7, 9, and 10 were directed principally to the alleged shortcomings of Dell—not QBMA. *See* App. Br. 23-26; Reb. Br. 7-8. Accordingly, we decline to consider Requester's untimely arguments based on QBMA's alleged shortcomings here in the first instance on rehearing. *See* 37 C.F.R. § 41.79(b)(1).

Nevertheless, even if we were to consider these belated arguments, we find them unpersuasive for the reasons indicated by Patent Owner. Comments 4-8. That ordinarily skilled artisans would understand that QBMA's two chip select signals (S0 and S1) are the only such signals in the reference and are distinguished from other types of signals as Patent Owner indicates only further undermines Requester's position on page 6 of the Request that QBMA's Bank Enable signal is somehow a "chip select" signal. Comments 4 (citing Sechen Decl. ¶¶ 46, 48). *Accord* Sechen Decl. ¶ 49 (declaring that ordinarily skilled artisans would understand that QBMA's Bank Enable signal is a clock signal—not an address signal or chip select signal); Comments 6-7 (citing this paragraph).

Accordingly, we are not persuaded that we misapprehended or overlooked those points in rendering our decision.

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Patent US 7,532,537 B2

CONCLUSION

For the foregoing reasons, we have granted Requester's request to the extent that we have reconsidered our decision, but we deny the request with respect to making any changes therein.

Pursuant to 37 C.F.R. § 41.79(d), this decision is final for the purpose of judicial review. A party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

DENIED

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