UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION
Requester and Appellant

v.

NETLIST, INC.
Patent Owner and Respondent

Appeal 2013-009066
Inter partes Reexamination Control 95/001,381
United States Patent 7,532,537 B2
Technology Center 3900

Before JOHN A. JEFFERY, KEVIN F. TURNER, and STANLEY M. WEINBERG, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Third Party Requester Inphi Corporation ("Requester") appeals under 35 U.S.C. §§ 134 and 315 the Examiner's decision declining to adopt Requester's proposed rejections of claims 1-49, 51-55, 57-61, and 63. App. Br. 2.[1] Claims 50, 56, and 62 have been cancelled. *Id.* The Respondent, Patent Owner Netlist ("Patent Owner"), is a party to this appeal under 35 U.S.C. § 315(a).

We have jurisdiction under 35 U.S.C. §§ 134 and 315, and we heard the appeal on November 20, 2013.[2] We affirm.

STATEMENT OF THE CASE

This proceeding arose from a request for *inter partes* reexamination filed on behalf of Requester on June 9, 2010, of United States Patent 7,532,537 B2 ("the '537 patent"), issued to Solomon et al. on May 12, 2009.

In this proceeding, the Examiner deemed claims 1-49, 51-55, 57-61, and 63[3] to be patentable and declined to adopt various proposed rejections of those claims—a decision that Requester appeals. App. Br. 2.

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[1] Throughout this opinion, we refer to (1) the Request filed June 9, 2010 ("Request"); (2) the Right of Appeal Notice mailed February 7, 2012 ("RAN"); (3) Requester's Appeal Brief filed May 31, 2012 ("App. Br."); (4) Patent Owner Respondent's Brief filed July 2, 2012 ("Resp. Br."); (5) the Examiner's Answer mailed April 16, 2013 ("Ans.") (incorporating the RAN by reference); and (6) Requester's Rebuttal Brief filed May 16, 2013 ("Reb. Br.").

[2] Throughout this opinion, we refer to the transcript of this oral hearing filed December 27, 2013 ("Tr.").

RELATED PROCEEDINGS

This appeal is said to be related to various pending proceedings. First, the '537 patent, a parent of U.S. Patent 7,636,274, is in reexamination (Control No. 95/001,377) and on appeal to this Board (Appeal No. 2013-009044).[4] App. Br. 2; Resp. Br. 1.

Second, the '537 patent and two other U.S. patents, 7,619,912 and 7,636,274, are said to be at issue in a pending stayed litigation. App. Br. 1 (citing Case No. 2:09-cv-06900 (C.D. Cal.)).

Third, we are informed that the '537 patent, which is said to be a continuation-in-part of U.S. Patent 7,289,386, is the subject of pending litigation that was stayed in connection with an associated reexamination (Control No. 95/000,546) that was merged with another reexamination proceeding of the '386 patent (Control No. 95/000,577). App. Br. 1 (citing Case No. 4:08-cv-04144 (N.D. Cal.)).

Fourth, the '912 patent, which is said to be a continuation of the '386 patent, is also said to be (1) the subject of pending stayed litigation and (2) associated with three merged reexaminations (Control Nos. 95/000,579, 95/000,578, 95/001,339). App. Br. 1-2 (citing Case No. 4:09-cv-05718 (N.D. Cal.)).

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[3] These claims include the '537 patent's claims 1-44 (some of which were amended during prosecution of this reexamination) and claims 45-49, 51-55, 57-61, and 63 that were added during prosecution. RAN 2-3.

[4] The decision in connection with related Appeal No. 2013-009044 is mailed concurrently with this decision.

Lastly, we are informed that U.S. Patent 7,864,627, which is said to be related to the '537 patent, is currently being reexamined. Resp. Br. 1 (citing Control No. 90/001,758).[5]

THE INVENTION

The invention of the '537 patent relates to computer system memory modules and, specifically, improving the modules' performance and/or memory capacity. To this end, a memory module comprises plural memory devices electrically coupled to a circuit that (1) selectively isolates one or more loads of the memory devices from the computer system and (2) translates between a system memory domain of the computer system and a physical memory domain of the memory module. *See generally* '537 patent, col. 1, ll. 28-32; col. 2, l. 62 – col. 3, l. 35; Figs. 1-9B. Claim 1 is illustrative of the invention and is reproduced below:

> 1. A memory module comprising:
>
> a plurality of memory devices, each memory device having
> a corresponding load; and
>
> a circuit electrically coupled to the plurality of memory devices and configured to be electrically coupled to a memory controller of a computer system, the circuit selectively isolating one or more of the loads of the memory devices from the computer system, the circuit comprising logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module, wherein the

[5] Patent Owner's Respondent Brief (at 1) appears to have identified an incorrect control number for this reexamination. The correct control number appears to be 95/001,758.

system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with a second number of chip selects equal to twice the first number of chip selects, wherein the plurality of memory devices comprises double-data rate (DDR) dynamic random-access memory (DRAM) devices and the chip selects of the first and second number of chip selects are DDR chip selects that are not CAS, RAS, or bank address signals.

THE PRIOR ART

The following prior art references are cited in the proposed rejections that are at issue in this appeal:

First Named Inventor	Patent Number	Issue Date
Kolor	US 5,590,071	Dec. 31, 1996
Connolly	US 5,802,395	Sept. 1, 1998
Johnson	US 6,233,650 B1	May 15, 2001
Wong	US 6,414,868 B1	July 2, 2002
Dell	US 6,446,184 B2	Sept. 3, 2002

QBM Alliance, *Quad Band Memory (QBM™): DDR 200/266/333 devices producing DDR 400/533/667*, Platform Conference (2002) ("QBMA")

DESIGN SPECIFICATION FOR JEDEC DIMM STANDARD NO. 21-C, Rev. 1.3, Release 11 b (2002) ("JEDEC")

THE PROPOSED REJECTIONS ON APPEAL[6]

Requester appeals the following proposed rejections that the Examiner did not adopt:

Claims	Statutory Basis (35 U.S.C.)	Cited References
1, 4-6, 13, 15, 24, 35, 39, 41	§ 102(b)	Johnson ("Issue 3")[7]
1, 4-6, 13, 15, 24, 35, 39, 41	§ 103	Johnson and JEDEC ("Issue 4")
1-7, 9, 12, 13, 15-31, 34-44	§ 103	Wong and Johnson ("Issue 5")
1, 8, 13, 14, 16, 18-20, 24, 25, 30, 35, 36, 39, 41, 42, 45-49, 53-55, 58-61, 63[8]	§ 103	QBMA and Dell ("Issues 7 and 9")
51, 52, 57	§ 103	QBMA, Dell, and JEDEC ("Issue 10")
45-49, 53-55, 58-61, 63	§ 103	Connolly and Kolor ("Issue 11")

[6] Although Patent Owner asks that we not admit portions of the "Background of the Technology" section of Requester's brief that are said to constitute unsubstantiated statements (Resp. Br. 18-19)—an allegation that is disputed (Reb. Br. 3-5)—we nonetheless consider Requester's brief as filed, giving any content, substantiated or otherwise, its due weight in arriving at our decision.

[7] For clarity, we refer to the issue numbers corresponding to those used by the parties and the Examiner.

[8] Although the Examiner includes cancelled claims 50, 56, and 62 in the proposed rejections for Issues 7, 9, and 11 (RAN 7-8), we nonetheless present the correct claim listings here for clarity.

App. Br. 5. Requester also appeals the Examiner's declining to reject independent claims 1, 13, and 18 (and their dependent claims) under 35 U.S.C. § 112, first paragraph as impermissibly adding new matter. App. Br. 4; Reb. Br. 5-6.[9]

THE PROPOSED NEW MATTER REJECTION

Requester argues that the phrase "DDR chip selects that are not CAS, RAS, or bank address signals" that was added to independent claims 1, 13, and 18 during reexamination impermissibly adds new matter to the '537 patent's original disclosure. App. Br. 7; Reb. Br. 5-6. According to Requester, the originally-filed Specification does not expressly teach "DDR chip selects," let alone suggest any advantage of using these chip selects over other memory device types that are said to be compatible with the disclosed embodiments. *Id.*

The Examiner, however, finds that the disputed added limitation is supported in column 16, line 49 to column 17, line 7 of the '537 patent. RAN 20.

[9] Although Requester challenged the entry of certain amendments and evidence (the Sechen Declaration) after prosecution closed (App. Br. 5-7), Requester nonetheless withdrew this issue from appeal as directed to petitionable matters. Reb. Br. 5. Accordingly, this issue is not before us. We do, however, address the new matter issue under § 112 because it is an appealable matter. *See* MPEP 2658(II) ("Where new or amended claims are presented or where any part of the disclosure is amended, the claims of the reexamination proceeding are to be examined for compliance with 35 U.S.C. 112.").

Patent Owner likewise contends that the disputed limitation is supported by the '537 patent but cites different passages than the Examiner in this regard. Resp. Br. 7.

ISSUE

Under § 112, first paragraph, has the Examiner erred in declining to reject independent claims 1, 13, and 18 by finding that the added limitation reciting "DDR chip selects that are not CAS, RAS, or bank address signals" is not new matter?

ANALYSIS

We sustain the Examiner's decision to not reject independent claims 1, 13, and 18 under § 112, first paragraph as failing to comply with the written description requirement by impermissibly adding new matter to the original disclosure. To satisfy the written description requirement, the disclosure must reasonably convey to skilled artisans that the patentee possessed the claimed invention as of the filing date. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). Although the description requirement under § 112 does not demand (1) any particular form of disclosure or (2) that the Specification recite the claimed invention verbatim, a description that merely renders the invention obvious does not satisfy the requirement. *Id.* at 1352 (citations omitted).

Here, it is undisputed that the negative limitation, "DDR chip selects that are not CAS, RAS, or bank address signals," was added by amendment

during reexamination. It is likewise undisputed that this particular phrase is not expressly stated in the '537 patent's original disclosure.

Nevertheless, it is well settled that negative limitations are permissible forms of expression to define the scope of a claimed invention. *See generally Animal Legal Defense Fund v. Quigg*, 932 F.2d 920, 923 (Fed. Cir. 1991). But the mere absence of a positive recitation in the original disclosure is not basis to exclude the limitation. MPEP § 2173.05. Rather, "[n]egative claim limitations are adequately supported when the specification describes a *reason* to exclude the relevant limitation." *Santarus, Inc. v. Par Pharm., Inc.*, 694 F.3d 1344, 1351 (Fed. Cir. 2012) (emphasis added).

On this record, we find the original disclosure reasonably conveys such a reason for exclusion. First, as Patent Owner's representative indicated at the oral hearing, the recited exclusion is consistent with JEDEC standards that distinguish the respective recited signals. Tr. 10. Second, the logic table in the '537 patent's Table 2 in a passage cited by Patent Owner pertains to selecting among ranks of memory devices 30 using gated CAS signals. Notably, the first row of this table indicates a logic "1" in the "CS" (chip select) column but indicates "X" for both the "RAS" and "CAS" columns—an exclusionary indicator. While not expressly articulating a reason to exclude the RAS and CAS signals, they are nonetheless excluded from this embodiment. *Accord* Tr. 5-7, 9-10 (acknowledging that Table 2 of the '537 patent refers to embodiments that exclude certain signals). And various other passages from the '537 patent cited by both Patent Owner and the Examiner indicate that chip selects are distinct from CAS, RAS, and

bank address signals, and where the chip selects are DDR chip selects. Resp. Br. 7; RAN 20.

When considering the '537 patent's disclosure as a whole, we find it reasonably supports the negative limitation that was added to independent claims 1, 13, and 18. Accordingly, the Examiner did not err in declining to reject these claims and their dependent claims under § 112, first paragraph.

THE PROPOSED ANTICIPATION REJECTION ("ISSUE 3")

The Examiner finds that Johnson does not anticipate independent claims 1, 13, 24, 35, and 39 for the reasons provided by Patent Owner on pages 14 through 31 and 33 through 36 of the remarks accompanying the amendment of August 22, 2011 ("PO Aug. 2011 Remarks"). RAN 6, 13, 18-19 (incorporating these remarks by reference). In these incorporated remarks, Patent Owner argued, among other things, that Johnson does not disclose (1) a memory module comprising a circuit for selectively isolating one or more memory device loads from the computer system as claimed and (2) the recited translation and different number of chip selects between the system and physical memory domains. PO Aug. 2011 Remarks, at 16-22. Patent Owner also argued in these incorporated remarks that Johnson fails to provide an enabling disclosure with respect to the recited translation limitation. *Id.* at 22-24.

Requester argues that Johnson teaches all recited limitations, namely those pertaining to address translation and chip select signals. App. Br. 31-33. According to Requester, Johnson performs "excess-bit translation" by decoding address bits from the memory controller to generate an "S" bit to

select between upper and lower memory banks. App. Br. 32. Requester adds that Johnson's splitting a system address space into two physical address spaces using one system address line necessarily involves a translation between the system and physical memory domains, where the domains are said to be compatible with a different number of chip selects as claimed. *Id.* According to Requester, skilled artisans would have also inferred Johnson's teaching DDR chip selects recited in independent claims 1, 13, and 18 in light of Johnson's disclosed embodiments that are said to be compatible with various memory device types. App. Br. 32-33.

Patent Owner argues, among other things, that Requester failed to challenge various patentability grounds on appeal, namely those based on Johnson's (1) lacking the recited load isolation and (2) alleged non-enabling disclosure regarding the recited translation limitation. Resp. Br. 7-11. Patent Owner adds that Johnson fails to disclose the translation and chip select limitations because Johnson uses the same number of chip select signals corresponding to both the system and physical memory domains, and Requester's reliance on Johnson's "S" signal for memory device selection is also misplaced. Resp. Br. 11-13.

ISSUE

Under § 102, has the Examiner erred in declining to reject independent claims 1, 13, 24, 35, and 39 by finding that Johnson does not disclose a memory module comprising a circuit that (1) selectively isolates one or more loads of memory devices from a computer system and (2) comprises logic which translates between system and physical memory

domains, where the system memory domain is compatible with a first number of chip selects and where the physical memory domain is compatible with twice that number of chip selects?

ANALYSIS

Waiver

We begin by noting—as does Patent Owner (Resp. Br. 9-11)—that Requester's Appeal Brief does not squarely address two key grounds for patentability from Patent Owner's August 2011 remarks that the Examiner incorporated by reference in the RAN, namely those based on Johnson's (1) lacking the load isolation limitation, and (2) alleged non-enabling disclosure regarding the recited translation limitation. PO Aug. 2011 Remarks, at 16-18, 22-24; RAN 19 (incorporating pages 14 through 31 and 33 through 36 of these remarks by reference). The Examiner's (1) explicitly incorporating these particular remarks by reference and (2) withdrawing the anticipation rejection (among other rejections) based on these remarks indicates that the Examiner found the remarks persuasive in declining to adopt the proposed anticipation rejection over Johnson. Despite Requester's contentions to the contrary (Reb. Br. 8-11), these remarks include the two articulated deficiencies of Johnson noted above and at least suggest that these two deficiencies at least partly influenced the Examiner's decision declining to adopt the proposed anticipation rejection of independent claims 1, 13, 24, 35, and 39 over Johnson.

Requester's contention (Reb. Br. 9) that these additional bases were never stated by the Examiner and that the "crux" of the Examiner's

declining to reject the claims was based on a narrow construction of "translate" and not other limitations is unavailing. First, Requester's reliance on pages 10, 11, and 15 of the RAN (Reb. Br. 9) is inapposite, for these cited pages pertain to Issues 1, 2, and 6 that are not at issue in this appeal. Second, although Requester generally asserts that "all limitations were met by the appropriate prior art" in the opening brief as Requester indicates (Reb. Br. 9 (citing App. Br. 31-33)), such general assertions do not persuasively rebut the Examiner's reliance on the specific reasons articulated in Patent Owner's August 2011 remarks that include the two above-noted deficiencies of Johnson that were incorporated by reference in the RAN.

Because Requester (1) does not address these two incorporated grounds for patentability in the Appeal Brief and (2) fails to show good cause for doing so, any alleged error in the Examiner's declining to adopt the proposed anticipation rejection based on these grounds is waived. *See* 37 C.F.R. § 41.67(c)(1)(vii) ("Any arguments or authorities not included in the brief . . . will be refused consideration by the Board, unless good cause is shown."). Accordingly, to the extent that Requester's position is based on earlier responses made before this appeal and not articulated in the opening brief (*see* Reb. Br. 9-11), we decline to consider those arguments here.[10]

[10] *See* 37 C.F.R. § 41.67(c)(1)(vii); *see also* MPEP 2675 ("It is essential that the Board . . . should be provided with a brief fully stating the position of the appellant with respect to each issue involved in the appeal so that *no search of the record is required in order to determine that position*.") MPEP 2675 (emphasis added).

For these reasons alone, Requester has not persuaded us that the Examiner erred in declining to reject independent claims 1, 13, 24, 35, and 39 as anticipated by Johnson.

Translation and Chip Select Limitations

We further find no error in the Examiner's declining to reject independent claims 1, 13, 24, 35, and 39 as anticipated by Johnson, for the additional reason that we agree with Patent Owner that Johnson does not disclose a memory module with logic that translates between system and physical memory domains, where the system memory domain is compatible with a first number of chip selects, and the physical memory domain is compatible with twice that number of chip selects.

We first construe the term "translate." Notably, unlike the related appeal in connection with *inter partes* Reexamination Control No. 95/001,377 (Appeal No. 2013-009044) ("the related appeal") where the Examiner explicitly construed the recited translation to be limited to the disclosed embodiments that require using implied translation logic equations, the Examiner does not expressly construe the term "translate" in the present appeal. *Compare* RAN 2-24 of the present reexamination *with* RAN 10 of the '377reexaminaton. Despite this ambiguity, we nonetheless construe the term "translate" here to be consistent with the earlier appeal—a point that was undisputed at the oral hearing. *Accord* Tr. 3-4, 8-9 (agreeing that the term "translate" should be construed consistently in both appeals). Accordingly, as in the earlier appeal, we construe "translate" to require a

circuit configurable to convert address and/or control signals between a system memory domain and a physical memory domain.

With this construction, we find that Johnson does not anticipate independent claims 1, 13, 24, 35, and 39. Despite Requester's arguments to the contrary, and even assuming, without deciding, that Johnson's deriving a FET switch "S" control signal from an address decoding circuit constitutes a translation between system and physical memory domains as Requester contends (App. Br. 32-33 (citing Johnson, col. 3, ll. 51-58; col. 4, ll. 3-11)), Requester has still not shown that this translation is between domains that are *necessarily* compatible with their respective numbers of chip selects with the recited 2:1 ratio. Rather, the evidence on this record tends to suggest that, at best, Johnson's system and memory domains are compatible with the same number of chip select signals as Patent Owner indicates. Resp. Br. 12 (citing Sechen Decl. ¶¶ 18-27). *Accord* RAN 19 (incorporating pages 18-22 of PO Aug. 2011 Remarks).

Therefore, regardless of whether skilled artisans would have "inferred" that Johnson's chip selects are DDR chip selects as Requester contends (App. Br. 32-33)—a problematic inference under anticipation standards that require that this feature is necessarily present in Johnson[11]—Johnson still fails to anticipate the recited memory module with the chip select limitations in independent claims 1, 13, 24, 35, and 39 that require the system and physical memory domains to be necessarily compatible with

[11] "Inherency . . . may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (citations omitted).

their respective numbers of chip selects with the recited 2:1 ratio. For this additional reason, Requester has not persuaded us that the Examiner erred in declining to reject claims 1, 4-6, 13, 15, 24, 35, 39, and 41 as anticipated by Johnson.

THE PROPOSED OBVIOUSNESS REJECTION OVER JOHNSON AND JEDEC ("ISSUE 4")

For similar reasons, we are likewise unpersuaded that that Examiner erred in declining to reject claims 1, 4-6, 13, 15, 24, 35, 39, 41 as obvious over Johnson and JEDEC. RAN 6, 13, 18-19 (incorporating pages 24-25 of PO Aug. 2011 Remarks). Despite Requester's contentions (App. Br. 33-34; Reb. Br. 8), we find that not only does JEDEC fail to cure Johnson's above-noted deficiencies, but the weight of the evidence on this record favors the Examiner's decision declining to reject the claims over these references. *Accord* Resp. Br. 13.

Accordingly, Requester has not persuaded us that the Examiner erred in declining to reject claims 1, 4-6, 13, 15, 24, 35, 39, and 41 as obvious over Johnson and JEDEC.

THE PROPOSED OBVIOUSNESS REJECTION OVER WONG AND JOHNSON ("ISSUE 5")

We are also unpersuaded of error in the Examiner's declining to reject claims 1-7, 9, 12, 13, 15-31, and 34-44 as obvious over Wong and Johnson. RAN 6-7, 14, 18-19 (incorporating pages 26-28 of PO Aug. 2011 Remarks).

First, because Requester's proposed rejection relies on Wong—not Johnson—for the recited chip select compatibility limitations, Requester's arguments pertaining to Johnson in this regard (Reb. Br. 6-7) are inapposite to this particular proposed ground of rejection. *See* Request, at 125-26 (citing only Wong, col. 4, ll. 30-32, 43-53, 55-60; Figs. 4A-4B in connection with the chip select compatibility limitations of claim 1). *Accord* App. Br. 28 (arguing Wong's disclosure in connection with the chip select limitations); Resp. Br. 14-15; PO Aug. 2011 Remarks, at 26-27 (arguing Wong's deficiencies in connection with the chip select limitations). Nevertheless, to the extent that Johnson applies to this aspect of this proposed rejection, we are unpersuaded by Requester's arguments for the reasons noted above.

Turning to Wong, we are unpersuaded by Requester's contentions (App. Br. 26-29; Reb. Br. 7) that Wong teaches or suggests the recited chip select limitations. In short, Requester does not persuasively rebut the Examiner's and Patent Owner's position that Wong's EDO Row Address Strobe (RAS) signals (i.e., RASUX and RASLX signals) are not chip select signals as Requester asserts because Wong's RAS signals are timing signals—not address signals. RAN 19 (incorporating pages 26-27 of PO Aug. 2011 Remarks); Resp. Br. 14-15 (citing Sechen Decl. ¶¶ 39-42). Although Wong's address signal "A13" is used as a bank selection input to a bank control circuit 2000 that drives RAS signals to the memory chips of the selected bank as Requester indicates (App. Br. 28 (citing Wong, Abstract)), these RAS signals are nonetheless not chip selects, let alone DDR chip selects, as those address-based signals are understood in the art—a fact

evidenced by Dr. Sechen's explanation in this regard. Sechen Decl. ¶¶ 33-43.

Although Wong's decoding addresses in connection with address signal "A13" (i.e., the most significant address bit) constitute a translation between system and physical memory domains as we noted in the related appeal (*see* Wong, col. 4, ll. 33-53; Figs. 3, 4A), we cannot say—nor has Requester shown—that the cited prior art teaches or suggests that these domains are compatible with their respective numbers of chip selects with the recited 2:1 ratio. Accordingly, Requester has not persuaded us that the Examiner erred in declining to reject claims 1-7, 9, 12, 13, 15-31, and 34-44 as obvious over Wong and Johnson.

THE PROPOSED REJECTION OVER QBMA AND DELL ("ISSUES 7 AND 9")

We are also unpersuaded of error in the Examiner's declining to reject claims 1, 8, 13, 14, 16, 18-20, 24, 25, 30, 35, 36, 39, 41, 42, 45-49, 53-55, 58-61, and 63 as obvious over QBMA and Dell. RAN 7-8, 16-19 (incorporating pages 28-31 of PO Aug. 2011 Remarks).

First, because Requester's proposed rejection relies on QBMA—not Dell—for the recited chip select compatibility limitations, Requester's arguments pertaining to Dell in this regard (Reb. Br. 7-8) are inapposite to this particular proposed ground of rejection. *See* Request, at 222 (citing only page 24 of QBMA in connection with the chip select compatibility limitations of claim 1). *Accord* Resp. Br. 16; PO Aug. 2011 Remarks, at 28, 31 (noting that only QBMA was cited for teaching the recited chip selects).

Nevertheless, to the extent that Dell applies to this aspect of this proposed rejection, we are unpersuaded that Dell teaches or suggests the recited chip selects for the reasons indicated by Patent Owner. Resp. Br. 17; Sechen Decl. ¶¶ 55-59.

That said, we found in the related appeal—as did the Examiner[12]—that Dell's remapping circuit translates addresses to convert at least address signals between a system memory domain and a physical memory domain. Therefore, we agree with Requester (App. Br. 23-24) to the extent that Dell's address translation fully meets the recited translation under the term's broadest reasonable interpretation, namely a circuit configurable to convert address and/or control signals between a system memory domain and a physical memory domain as noted above.

But despite (1) the Examiner's finding in the related appeal that Dell and QBMA are combinable,[13] and (2) Requester's contentions to the contrary (App. Br. 23-26; Reb. Br. 7-8), we nonetheless agree with the Examiner and Patent Owner that these references fail to teach or suggest that the system and physical memory domains are compatible with their respective numbers of chip selects with the 2:1 ratio as recited in the independent claims. To be sure, both Patent Owner and Dr. Sechen admit that QBMA discloses DDR chip selects, namely the signals "S0" and "S1" on pages 31 and 32 that are used to simultaneously select two ranks. PO Aug. 2011 Remarks, at 29-30; Sechen Decl. ¶¶ 46, 48. But Requester does not persuasively rebut Patent Owner's position that the cited prior art fails to

[12] *See* Appl'n Control No. 95/001,337, RAN 11
[13] *See id.* ("Dell teaches address translation (remapping) circuitry *that would have been compatible with the system of QBMA*." (emphasis added)).

teach or suggest the system and physical memory domains are compatible with their respective numbers of chip selects, let alone DDR chip selects, with the recited 2:1 ratio as Patent Owner indicates. Resp. Br. 16 (citing Sechen Decl. ¶¶ 46, 48); PO Aug. 2011 Remarks, at 30. Nor does Requester persuasively rebut Patent Owner's position that other relied-upon signals in QBMA do not constitute "chip selects" as those address-based signals are understood in the art—a fact evidenced by Dr. Sechen's explanation in this regard. Resp. Br. 16; Sechen Decl. ¶¶ 46-54.

Therefore, we are unpersuaded of error in the Examiner's declining to reject claims 1, 8, 13, 14, 16, 18-20, 24, 25, 30, 35, 36, 39, 41, 42, 45-49, 53-55, 58-61, and 63 as obvious over QBMA and Dell.

THE PROPOSED REJECTION OVER QBMA, DELL, AND JEDEC ("ISSUE 10")

Because Requester has not shown that JEDEC cures the above-noted deficiencies regarding QBMA and Dell as Patent Owner indicates (Resp. Br. 17) , we likewise are unpersuaded that the Examiner erred by declining to reject claims 51, 52, and 57 as obvious over QBMA, Dell, and JEDEC. RAN 8, 17-19.

THE PROPOSED REJECTION OVER CONNOLLY AND KOLOR ("ISSUE 11")

We are likewise unpersuaded of error in the Examiner's declining to reject claims 45-49, 53-55, 58-61, and 63 as obvious over Connolly and Kolor. RAN 8, 18-19. As Patent Owner indicates (Resp. Br. 17), these

claims depend from independent claims 1, 13, or 18 that each recite the translation and chip select limitations noted above. Despite Requester's contentions to the contrary (App. Br. 29-31; Reply Br. 8), Requester does not persuasively rebut Patent Owner's position that Connolly's or Kolor's RAS and CAS signals are not DDR chip selects as those address-based signals are understood in the art—a fact evidenced by Dr. Sechen's explanation in this regard. Resp. Br. 17-18; Sechen Decl. ¶¶ 61-68.

Nevertheless, even assuming, without deciding, that (1) the Connolly/Kolor system translates address signals between memory domains and (2) some other unspecified signals in Kolor can be used for chip selection as Requester asserts (App. Br. 29-30), Requester still fails to persuasively rebut Patent Owner's position regarding the recited chip select compatibility limitations in independent claims 1, 13, and 18. Resp. Br. 18; Sechen Decl. ¶¶ 61-68. On this record, we find the weight of the evidence favors Patent Owner's position that Connolly and Kolor collectively fail to teach or suggest that the system and physical memory domains are compatible with their respective numbers of chip selects with the recited 2:1 ratio as recited in independent claims 1, 13, and 18 from which claims 45-49, 53-55, 58-61, and 63 depend.

Therefore, we are unpersuaded of error in the Examiner's declining to reject claims 45-49, 53-55, 58-61, and 63 as obvious over Connolly and Kolor.

CONCLUSION

The Examiner did not err in declining to reject (1) claims 1-23, 45-49, 51-55, 57-61, and 63 under § 112, first paragraph; (2) claims 1, 4-6, 13, 15, 24, 35, 39, 41 under § 102; and (3) claims 1-9, 12-31, 34-49, 51-55, 57-61, and 63 under § 103.

ORDER

The Examiner's decision declining to reject claims 1-49, 51-55, 57-61, and 63 is affirmed.

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

AFFIRMED

peb

Appeal 2013-009066
Reexamination Control 95/001,381
Patent US 7,532,537 B2

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