Filed on behalf of Hewlett-Packard Co.
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HEWLETT-PACKARD COMPANY,
Petitioner

v.

MCM PORTFOLIO, LLC,
Patent Owner

Patent No. 7,162,549
Issued Jan. 9, 2007
for
MULTIMODE CONTROLLER FOR
INTELLIGENT AND "DUMB" FLASH CARDS

Inter Partes Review No. Unassigned

PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-19 AND 37 C.F.R. § 42.100 *et. seq.*

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EXHIBIT LIST

1999)

HP 1026 CV of Dr. Sanjay Banerjee

HP 1027 Holczer Affadavit

HP 1028 IDSs from '549 Patent Reissue Appln. (as of 03-26-13)

HP 1029 TPL's Proposed Claim Constructions (337-TA-841)

HP 1030 Markman Order (337-TA-841)

I. Mandatory Notices

Real Parties-in-Interest: Hewlett-Packard Co. ("HP" or "Petitioner"), MCM Portfolio, LLC ("Patent Owner), and Technology Properties Limited, LLC ("TPL" or "Exclusive Licensee")

Related Matters: The following matters would affect or be affected by the decision in this proceeding:

- *Technology Properties Limited, LLC v. Hewlett-Packard Co.*, 6:12-cv-208 (E.D. Tex.);
- *Technology Properties Limited, LLC v. Acer Inc.*, 6:12-cv-200 (E.D. Tex.);
- *Technology Properties Limited, LLC v. Brother Indus. Ltd.*, 6:12-cv-201 (E.D. Tex.);
- *Technology Properties Limited, LLC v. Dell, Inc.*, 6:12-cv-204 (E.D. Tex.);
- *Technology Properties Limited, LLC v. Falcon NW Computer Sys., Inc.*, 6:12-cv-205 (E.D. Tex.);
- *Technology Properties Limited, LLC v. HiTi Digital, Inc.*, 6:12-cv-207 (E.D. Tex.);
- *Technology Properties Limited, LLC v. Newegg Inc.*, 6:12-cv-213 (E.D. Tex.);
- *Technology Properties Limited, LLC v. Seiko Epson Corp.*, 6:12-cv-216 (E.D. Tex.);
- *Certain Computer and Computer Peripheral Devices and Components Thereof and Products Containing Same*, Inv. No. 337-TA-841 (ITC) ("the related ITC Investigation"); and
- Pending U.S. Patent Appln. No. 12/351,691 (pending reissue application).

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II. Grounds for Standing

Petitioner certifies that U.S. Patent No. 7,162,549 ("the '549 Patent") is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this petition.

III. The Pending Reissue Application

As of the filing date of this petition, the '549 Patent is the subject of a pending reissue proceeding (U.S. Appl'n. No. 12/351,691). A stay of the reissue proceeding is warranted because, *inter alia*, (i) the prior art being used to challenge the '549 Patent's claims in this petition is directly relevant to the validity of the claims in the *ex parte* reissue proceeding; (ii) the record from the reissue proceeding indicates that the Patent Owner failed to submit to the Office two of the primary prior art references being relied upon by Petitioner in this proceeding (AwYong and Battaglia)—even though these references were relied upon in the related ITC Investigation as invalidating the '549 Patent and even though the Patent Owner submitted to the Office other prior art references from the related ITC Investigation; and (iii)

conducting the reissue proceeding concurrently with an *inter partes* review proceeding would duplicate efforts within the Office and could potentially result in inconsistencies between the proceedings.

IV. Identification of Challenge (37 C.F.R. § 104(b)(1)-(3)) and Relief Requested (37 C.F.R. § 42.22(a)(1))

Petitioner challenges claims 7, 11, 19, and 21 of the '549 Patent under 35 U.S.C. §§ 102 and 103. Petitioner requests cancellation of those claims.

A. Priority Date of the '549 Patent

On its face, the '549 Patent claims priority to a provisional patent application (60/386,396) filed June 4, 2002. HP 1001. In the related ITC Investigation, the Patent Owner's exclusive licensee – Technology Properties Limited, LLC ("TPL") – agreed that June 4, 2002 is the effective filing date of the '549 Patent. Accordingly, claims 7, 11, 19, and 21 of the '549 Patent are entitled to an effective filing date of no earlier than June 4, 2002. *See also* HP 1008 (Dr. Banerjee Decl.), ¶ 33.

B. Printed Publications Relied On

1. Primary References

i. AwYong (HP 1002/HP 1003)

"AwYong" is a printed publication titled "An Integrated Control System

Design of Portable Computer Storage Peripherals." HP 1002 (English translation)[1]; HP 1003 (original Chinese publication). The document is described as a "Thesis Submitted to Department of Electrical and Control Engineering College of Electrical Engineering and Computer Science National Chiao-Tung University in Partial Fulfillment of the Requirements for the Degree of Master in Electrical and Control Engineering by Chee-Kong AwYong." HP 1002.

AwYong was published and publicly available as of December 22, 2000. Dr. Robert Ellett,[2] an experienced librarian, testified about the public availability of AwYong in the related ITC Investigation. HP 1009, Q/A 24-36; *see also* HP 1010. Dr. Ellett described the MARC (Machine Readable Cataloging) system and his inspection of the MARC record for AwYong, which he obtained from the National Chiao-Tung University (NCTU) Library in Hsinchu, Taiwan. HP 1011; HP 1009, Q/A 13-24. He

[1] An affidavit provided by Abraham Holczer attests to the accuracy of AwYong's translation. HP 1027; *see also* HP 1002, p. 85 (original certification of accuracy).

[2] When attempting to contact Dr. Ellett to provide a declaration for this proceeding, Petitioner learned that Dr. Ellett passed away on January 9, 2013. Thus, Petitioner relies on Dr. Ellett's declaration and testimony from the related ITC Investigation, which was brought by Patent Owner's exclusive licensee (TPL) and during which TPL cross-examined Dr. Ellett.

testified about the process by which AwYong was indexed, cataloged, shelved, and publicly searchable. HP 1009, Q/A 24-36. As explained by Dr. Ellett, the thesis was submitted in June 2000 (as indicated on the cover of the thesis); approved by the thesis advisor on June 9, 2000 (as indicated on page 2 of the thesis); and indexed, cataloged, shelved, and publicly accessible as of December 22, 2000 (as indicated on the back cover of the thesis). HP 1009, Q/A 24-36. Dr. Ellett also explained that the December 22, 2000 publication date is confirmed by the MARC record; the dates on the thesis itself; the back cover of the thesis, which includes the date "89 12 22," which corresponds to western calendar December 22, 2000; and the Publication Certification, which is an official document of NCTU. *Id.*; HP 1002; HP 1012; HP 1013; HP 1014. Dr. Ellett further explained that NCTU is a public university whose resources are available to the general public, and thus a member of the public would have been able to search for and gain access to the thesis as of December 22, 2000. HP 1009, Q/A 35-36. Accordingly, AwYong is prior art to the '549 Patent under at least 35 U.S.C §§ 102(a) and (b).

The Office did not consider AwYong during the original prosecution of the '549 Patent. HP 1001, pp. 1, 2. Moreover, it appears the Patent Owner has not submitted AwYong in the pending reissue application, HP 1028, even though AwYong was raised in invalidity challenges during the related ITC Investigation.

ii. U.S. Patent No. 6,987,927 ("Battaglia") (HP 1004)

U.S. Patent No. 6,987,927 ("Battaglia") was filed July 13, 2000, and issued Jan.

17, 2006. Therefore, it qualifies as prior art to the '549 Patent under at least § 102(e). The Office did not consider Battaglia during the original prosecution of the '549 Patent. HP 1001, pp. 1, 2. Moreover, it appears the Patent Owner has not submitted Battaglia in the pending reissue application, HP 1028, even though Battaglia was raised in invalidity challenges during the related ITC Investigation.

iii. U.S. Patent No. 6,199,122 ("Kobayashi") (HP 1005)

U.S. Patent No. 6,199,122 ("Kobayashi") was filed on July 22, 1998, and issued on March 6, 2001. Therefore, it qualifies as prior art to the '549 Patent under at least 35 U.S.C. §§ 102(a) and (b).

Kobayashi is listed on the face of the '549 Patent as a reference cited during prosecution (HP 1001, p. 2), and the '549 Patent file history indicates that Kobayashi formed the basis for rejections during original prosecution (HP 1015, pp. 319-22, 413-18, 504-9). However, the Office did not combine Kobayashi with the reference indicated below under 35 U.S.C. § 103. *Id.*

2. Secondary References

i. Samsung SmartMedia Card Model No. K9D1208V0M-SSB0 Datasheet ("the Samsung Datasheet") (HP 1006)

The Samsung Datasheet indicates it was available by November 20, 2000, and provides a web address where users could access the document. HP 1006, p. 1. Moreover, an archived version of this Samsung website (accessed via the Wayback Machine Internet Archive) confirms that the Samsung Datasheet was available to the

public at least as early as December 11, 2000. HP 1016. Therefore, the Samsung Datasheet qualifies as prior art under at least 35 U.S.C. §§ 102(a) and (b).

The Office did not consider the Samsung Datasheet during the original prosecution of the '549 Patent. HP 1001, pp. 1, 2.

ii. International Application Publication No. WO 98/03915 ("Kikuchi") (HP 1007)

International Patent Application Publication No. WO 98/03915 ("Kikuchi") was published January 29, 1998. Therefore, it qualifies as prior art to the '549 Patent under at least §§ 102(a) and (b). The Office did not consider Kikuchi during the original prosecution of the '549 Patent. HP 1001, pp. 1, 2. Moreover, it appears the Patent Owner has not submitted Kikuchi in the pending reissue application. HP 1028.

C. <u>Statutory Grounds for Challenge</u>

Petitioner requests cancellation of claims 7, 11, 19, and 21 on the following grounds:

A. Claims 7, 11, 19, and 21 are anticipated under 35 U.S.C. §§ 102(a) and (b) by AwYong;

B. Claims 7, 11, 19, and 21 are rendered obvious under 35 U.S.C. § 103 by Battaglia alone and in view of the Samsung Datasheet; and

C. Claims 7, 11, 19, and 21 are rendered obvious under 35 U.S.C. § 103 by Kobayashi in view of Kikuchi.

V. Claim Construction

In the context of an *inter partes* review proceeding, claim terms are given their broadest reasonable construction in view of the specification. 37 C.F.R. § 42.100(b).[3]

A. Terms Construed in the Related ITC Investigation

In the related ITC Investigation, an Administrative Law Judge interpreted both the phrases "flash adapter" and "flash adapter section" from the challenged claims to mean "a section of the controller chip that enables communication with the flash storage system." HP 1030, pp. 73-77; *see also* HP 1029, p. 3.

B. Terms Not Construed in the Related ITC Investigation

1. Flash Storage System and Flash Section

"Flash storage system" and "flash section," when given their broadest reasonable interpretation, can be construed to refer to a flash memory card and flash memory circuits, respectively. The patent specification describes a flash medium 4020b, which corresponds to a card, as containing a flash section 4022 and a medium ID 4030. HP 1001, 28:29-31, 28:42-43, Figs. 31, 32. This description aligns with the specification description of a "flash storage system [that] comprises a flash section

[3] Because the Office's claim construction standard differs from that applied in a district court or similar judicial proceeding, nothing in this petition should preclude Petitioner from advancing an alternative construction in such proceedings, and Petitioner reserves all rights in this regard.

and at least a medium ID." *Id.* at 30:27-29, 30:50-51.

2. The "Determining" and "Detector" Limitations

The "determining" limitation of claim 7 and "detector" limitation of claim 11 may be assigned their plain meaning. Both claims refer to a "controller chip to interface with a flash storage system with or without a controller" that "determin[es] whether the flash storage system includes a controller for error correction." *Id.* at 30:24-30, 30:52-59. In the case of claim 11, the controller chip is recited as having a detector.

VI. Background of the Technology at Issue

A. Technical Background of the '549 Patent

The '549 Patent identifies itself as relating to a multi-format memory card reader. Claims 7, 11, 19, and 21 refer to techniques for interfacing with different types of flash memory cards: those with and without on-card controllers. While certain types of flash memory cards have an on-card controller for error correction and bad block mapping, other types do not. As these concepts pertain to the '549 Patent, error correction maintains the integrity of stored data, which can be corrupted by environmental factors and circuit failure. The concepts of both error correction and bad block mapping – and their application to flash memory – were well known and established prior to the effective filing date of the '549 Patent in June 2002. HP 1008 (Dr. Banerjee Decl.), ¶ 27.

Claims 7, 11, 19, and 21 each require a determination as to whether or not an

inserted memory card includes a controller for error correction. These claims also require that – when interfacing with controllerless cards – the task of error correction and bad block mapping is managed by "firmware" located in a flash adapter. The specification describes this as "firmware 4012*b* of the host computer, which now, on top of its normal access section software, also manages error correction and bad block mapping" of the flash memory card. HP 1001, 28:54-58.

B. Prior Art Flash Memory Cards

The '549 Patent identifies several formats of memory cards as prior art. HP 1001, 2:27-54. Many of these card formats have features relevant to the challenged claims' recitations. For example, SD, MMC, MemoryStick, and CompactFlash cards each were defined, in respective standards documents, to include controllers for error correction, flash sections, and medium IDs. By contrast, standards documents for SmartMedia cards defined them to be controllerless but to include flash sections and medium IDs. All of these cards were defined by their respective standards documents before the effective filing date of the '549 Patent (June 2002) and are referenced by the prior art documents on which this petition is based. Moreover, the '549 Patent admits that prior art card readers from Lexar Media read SmartMedia cards and CompactFlash cards that, as discussed below, are controllerless and controller-based cards, respectively. HP 1001, 3:12-16. Therefore, Petitioner offers the following brief summary of each card to provide context for the discussion of invalidity challenges herein.

1. CompactFlash Cards Have Controllers, Flash Sections, and Medium IDs.

As explained in the CompactFlash Specification, CompactFlash (CF) cards include an on-card controller for error correction and a flash section. HP 1017, §1.3, p. 12. Figure 1 of this specification shows both:

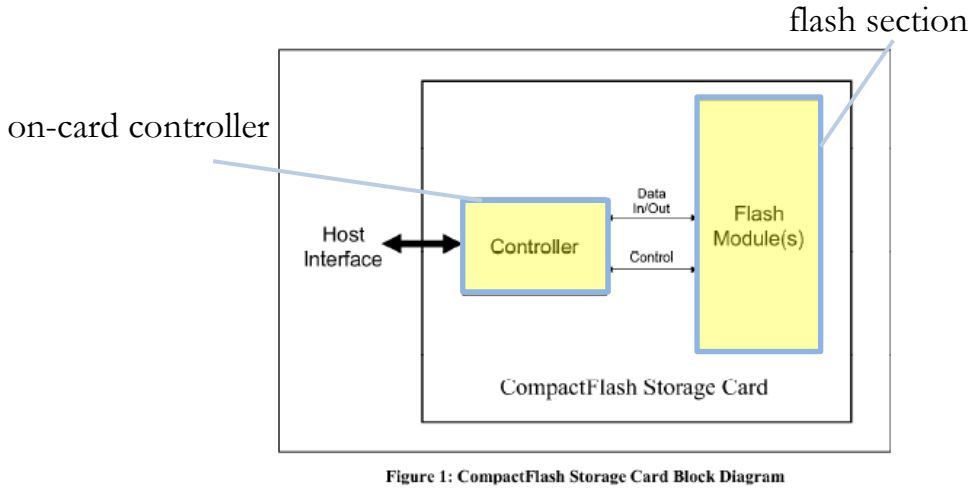


Figure 1: CompactFlash Storage Card Block Diagram

Figure 1: FIG. 1 of CompactFlash Specification (annotated) (HP 1017, p. 15)

Indeed, the CompactFlash Specification explains that "CompactFlash Storage Cards[']on-card intelligent controller manages interface protocols, data storage and retrieval as well as Error Correcting Code (ECC), defect handling and diagnostics, power management, and clock control." *Id.* at §1.3, p. 12.

CompactFlash cards have both a flash section and a medium ID. HP 1008 (Dr. Banerjee Decl.), ¶¶ 51-52. The "flash section" in these cards is demonstrated in Figure 1, *supra*. HP 1017, p. 15. Further, the '549 Patent describes CompactFlash as one of the prior art "flash card formats," acknowledging that these cards have a "flash section." HP 1001, 2:27-54. As described in the CompactFlash Specification,

CompactFlash cards have a medium ID, called a "Card Information Structure (CIS)," as well. HP 1017, §4.4, p. 50.

2. MMC and SD Cards Have Controllers, Flash Sections, and Medium IDs.

MultiMediaCards (MMC) and Secure Digital (SD) cards are identified by their standards documents as related to each other. Both MMC and SD cards include an on-card controller for error correction, as well as a flash section. HP 1018, p. 7 (MMC); HP 1019, §4.10.1, pp. 48-51 (SD). The on-card controllers ("Card Interface Controller") and flash sections ("memory core") are shown in the following figures:

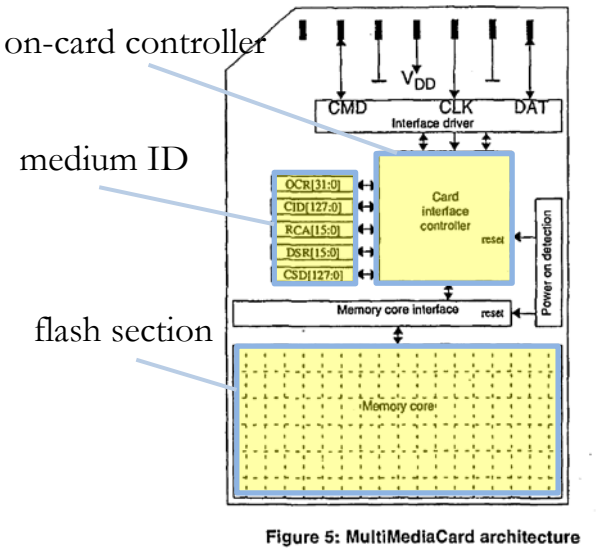


Figure 2: FIG. 5 of MMC System Summary (annotated) (HP 1020, p. 14)

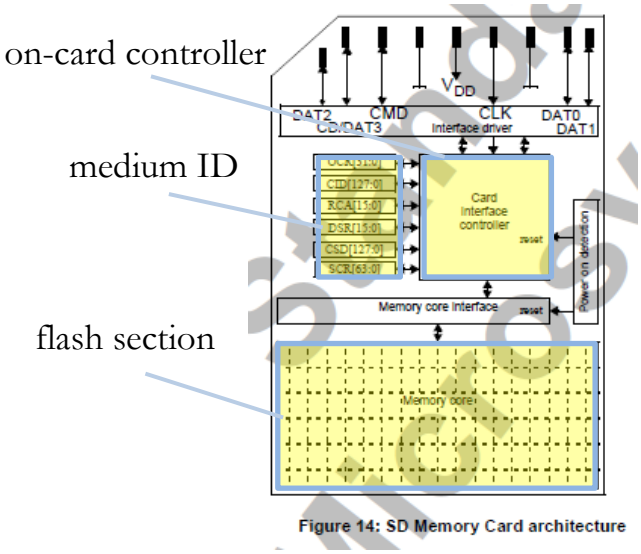


Figure 3: FIG. 14 of the SD Memory Card Specifications (annotated) (HP 1019, p. 18)

The "on-card intelligent controller manages interface protocol interface protocols and data storage and retrieval, as well as Error Correction Code (ECC) algorithms, defect handling and diagnostics, power management, and clock control."

HP 1018, p. 7; *see also* HP 1019*,* §4.10.1, pp. 48-51 (explaining SD on-card controller).

MMC and SD cards also have both a flash section and a medium ID, as shown in Figure 2 and Figure 3, *supra*. HP 1008 (Dr. Banerjee Decl.), ¶¶ 58-59 (MMC), 64-65 (SD). The inclusion of a "flash section" in each of these cards is evident from the specifications of the cards themselves. HP 1020, p. 14, Fig. 5 (MMC); HP 1020, pp. 18, 51-52 (SD). Further, the '549 Patent itself describes MMC and SD as "flash card formats," acknowledging that these cards have a "flash section." HP 1001, 2:27-54. As described in each of their specifications, MMC and SD cards have a medium ID, such as a CID [card identification] register, as well. HP 1018, p. 28 (MMC); HP 1019, §5.2, p. 61 (SD).

3. MemoryStick Cards Have Controllers, Flash Sections, and Medium IDs.

Likewise, MemoryStick (MS) cards include an on-card controller for error correction, as shown in the MemoryStick Standard, Format Specifications, ver. 1.2. HP 1021, Fig. 4.1.1. The MS cards' on-card controller is shown here:

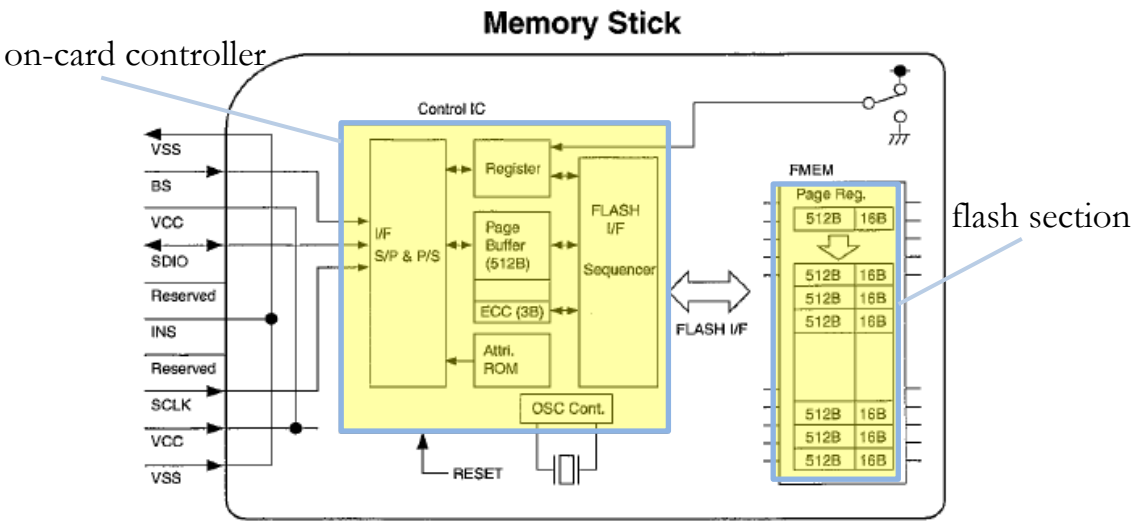


Fig. 4.1.1 Block Diagram(example)

Figure 4: FIG. 4.1.1 of the MemoryStick Standard (annotated) (HP 1021, p. 21)

MS cards have both a flash section and a medium ID. HP 1008 (Dr. Banerjee Decl.), ¶¶ 69-70. The inclusion of a "flash section" in MS cards is evident from the card specifications themselves. HP 1021, p. 21. Further, the '549 Patent describes MemoryStick as one of the prior art "flash card formats," acknowledging that these cards have a "flash section." HP 1001, 2:27-54. As described in their specifications, MemoryStick cards have a medium ID – the "Boot & Attribute Information" outlined in the MS Specifications – as well. HP 1021, §7.4.4, p. 132.

4. SmartMedia Cards Have Flash Sections and Medium IDs But Do Not Have On-Card Controllers.

SmartMedia cards do not have an on-card controller for error correction, as defined by the SmartMedia Specifications. HP 1008 (Dr. Banerjee Decl.), ¶ 40.

The SmartMedia Software Algorithm Guidelines Version 1.00 was issued on

May 19, 2000 (HP 1022, p. 1); the SmartMedia ECC Reference Manual Ver. 2.1 (Software and Hardware) was issued on September 15, 1999 (HP 1023, p. 1); and the SmartMedia Interface Library was issued on July 1, 2000 (HP 1024, p. 1).[4] Collectively, these documents will be referred to as "the SmartMedia Specifications." In order to design a host or reader for SmartMedia cards, one of ordinary skill in the art would necessarily have accessed the SmartMedia Specifications and been familiar with the teachings therein.

The SmartMedia Specifications explain that error correction operations, including bad block mapping, are performed by a host controller external to the SmartMedia card itself. HP 1022; HP 1023; HP 1024. For example, the SmartMedia Interface Library depicts a circuit layout diagram with an "ECC logic" block:

[4] Accordingly, each of these documents is prior art to the '549 Patent under at least 35 U.S.C. §§ 102(a) and (b). Indeed, the '549 Patent acknowledges the SmartMedia format (as well as other memory card formats) as admitted prior art in the background section of the specification. HP 1001, 2:27-4:26.

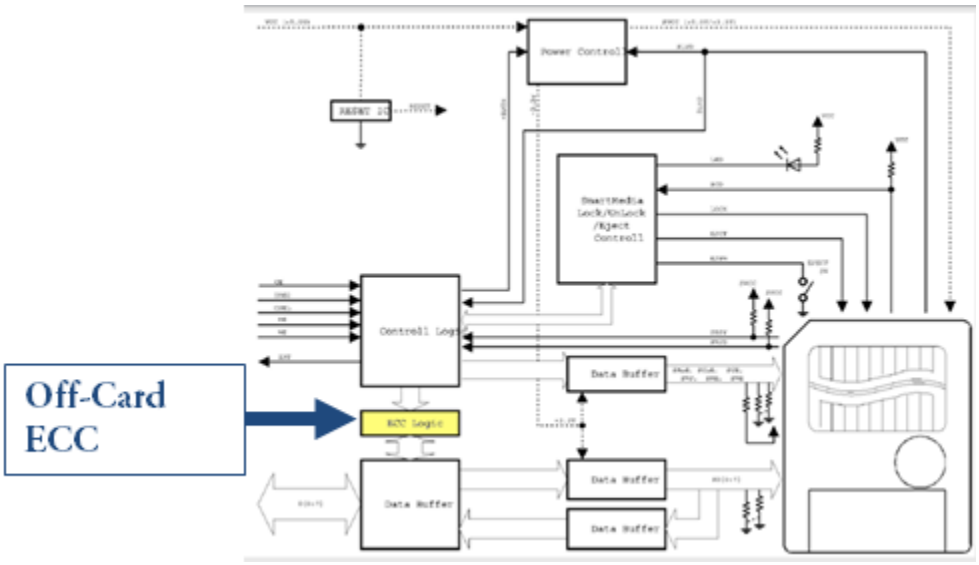


Figure 5: Fig. 2-1 of SmartMedia Interface Library (annotated) (HP 1024, p. 5)

The ECC logic represents the error correction process performed by the external (host) controller, as required by the controllerless SmartMedia card. HP 1024, Fig. 2-1, p. 5. In addition, the SmartMedia Software Algorithm Guidelines describe in detail bad block mapping operations as part of error correction and depict an exemplary logical-physical conversion table generation flow. HP 1022, pp. 15-18. Further, the SmartMedia Specifications teach using firmware (software in non-volatile memory) to perform error correction. HP 1023, p. 3.

Thus, SmartMedia cards do not have an on-card controller, and the SmartMedia Specifications mandate that an external controller perform the required error correction and bad block mapping operations. HP 1008 (Dr. Banerjee Decl.), ¶ 43.

Furthermore, SmartMedia cards have both a flash section and a medium ID.

HP 1008 (Dr. Banerjee Decl.), ¶¶ 44-45. The inclusion of a "flash section" in these cards is evident from the card specifications themselves. HP 1025, p. 11 (describing "flash memory" in SmartMedia cards). Further, the '549 Patent describes SmartMedia as one of the prior art "flash card formats," acknowledging that these cards have a "flash section." HP 1001, 2:27-54.

As described in the SmartMedia specifications, SmartMedia cards have a medium ID as well. HP 1025, p. 15, Fig. 6.2. For example, the SmartMedia Electronic Specifications Web-Online Version 1.00, issued on May 19, 1999, (HP 1025) explains that SmartMedia cards have a medium ID, which is accessed by a command called the 90h command, as shown in the following figure:

Fig. 6-2 Operating Command Table

Function	1st cycle	2nd cycle	Acceptable Command during Busy State
Serial Data Input (Note 1)	80h		
Read (1)	00h		
Read (2) (Note 2)	01h		
Read (3) (Note 3)	50h		
Reset	FFh		O
Page Program (Note 1)	10h		
Block Erase (Note 1)	60h	D0h	
Status Read	70h		O
ID Read	90h		

Figure 6: FIG. 6.2 of the SmartMedia Specifications (annotated) (HP 1025, p. 15)

VII. Invalidity Challenges

A. AwYong Anticipates the Challenged Claims.

As described herein, AwYong anticipates claims 7, 11, 19, and 21 of the '549 Patent under 35 U.S.C. §§ 102(a) and (b).

1. Independent Claim 7

i. "using a controller chip to interface a flash storage system with or without a controller to a computing device"

AwYong describes a system that uses a controller chip to allow host computing devices (*e.g.*, desktop or notebook PCs) to use various types of flash memory cards. HP 1002, pp. 14, 17, 23, Fig. 2-2. As illustrated in FIG. 2-2 (reproduced as Figure 7, *infra*) AwYong describes a controller implemented in a single chip that interfaces with multiple types of flash storage systems, including SmartMedia cards (which do not have a controller) and CompactFlash and MMC cards (which do have a controller). *Id.* at 23, Fig. 2-2.

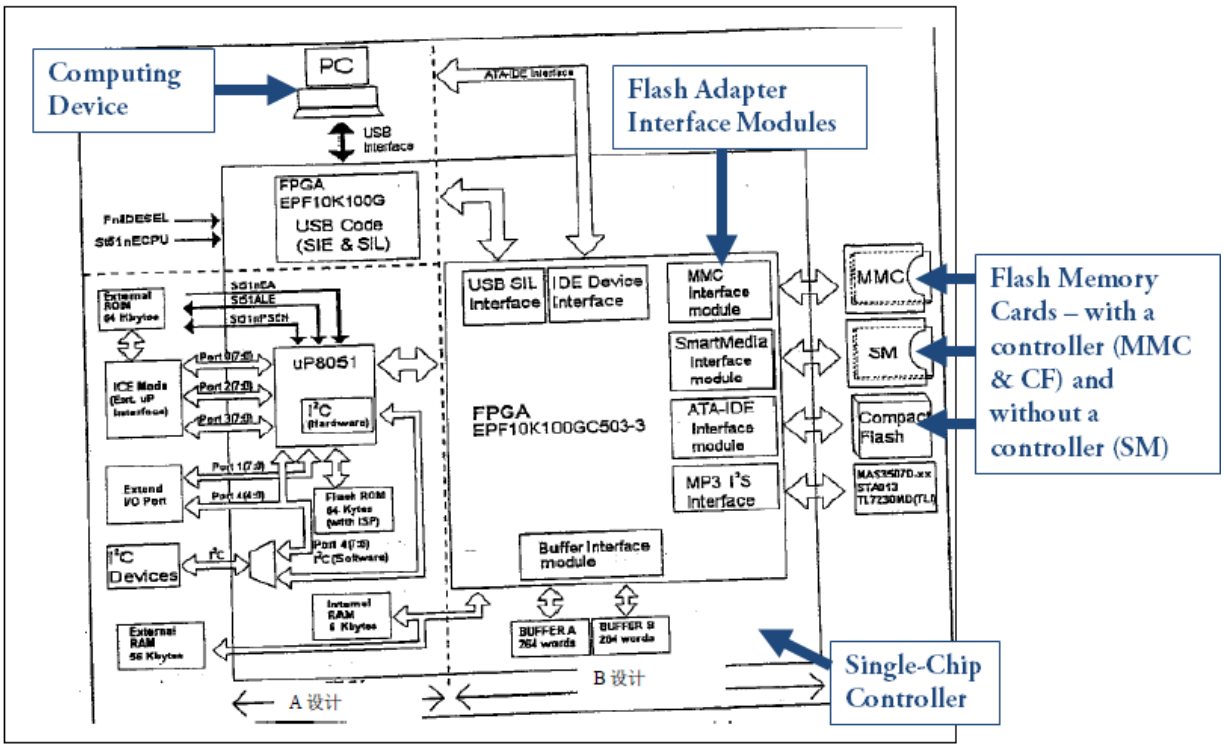


Figure 7: FIG. 2-2 of AwYong (annotated)

AwYong states that the "fundamental motivation of this research is to design a

single-chip controller and use this controller as the computing center of the device system. One end of this system can be connected to a storage card such as a Smart Media Card, Compact Flash Card, or Multi Media Card that is popular in the current market, and the other end can be connected to a desktop PC." *Id.* at 14; *see also id.* at 16-17. AwYong expressly recognizes that unlike the other card types, SmartMedia cards do not have on-card controllers:

> It [the single-chip controller] must have the memory management capability. It is troublesome to deal with the Smart Media storage card, because there is no processor for managing the memory inside the Smart Media storage card, and it is managed by an external system. To solve the problems of compatibility and universality, the Solid State Floppy Disk Card (SSFDC) Association rigidly defines a set of memory management specifications (SSFDC Physical Format Specification Version 1.11), and all the external systems that need to access data from Smart Media storage cards must observe these management specifications to correctly access Smart Media storage cards. Therefore, this single-chip controller must be capable of enforcing these management specifications to manage the memories inside Smart Media storage cards. *Id.* at 17.

Thus, AwYong teaches using a controller chip to interface with flash storage systems both with and without controllers.

ii. "the controller chip comprising a flash adapter"

AwYong's controller chip comprises a flash adapter section in the form of interface modules for each type of card read by the chip. HP 1002, pp. 14, 23, 50-75,

Fig. 2-2. As shown in Figure 7, *supra*, the controller chip includes an "MMC Interface module" for MMC cards, a "SmartMedia Interface module" for SmartMedia cards, and an "ATA-IDE Interface module" for CompactFlash cards. *Id.* at 23, 50-75, Fig. 2-2.

iii. "wherein the flash storage system comprises a flash section and at least a medium ID"

AwYong's system is compatible with multiple types of flash storage systems, including CompactFlash, SmartMedia, and MMC cards. HP 1002, pp. 14, 17, 23, Fig. 2-2. As explained previously, each of these cards comprises a flash section and a medium ID as defined by the cards' specifications. HP 1018, p. 28 (MMC); HP 1017, pp. 50-59 (CF); HP 1025, p. 15 (SmartMedia); HP 1008 (Dr. Banerjee Decl.), ¶¶ 44-45, 51-52, 58-59.

iv. "determining whether the flash storage system includes a controller for error correction"

AwYong's system distinguishes controller-based cards from cards with controllers. As discussed previously, AwYong describes compatibility with multiple types of flash storage systems, including SmartMedia (which does not have a controller) and CompactFlash and MMC (which do have controllers). HP 1002, pp. 14, 17, 23, 48-49, 54, 57, Figs. 2-2, 5-3, 5-4, 5-5. AwYong's controller detects a type of card inserted into its card reader and engages different processes based on whether the card has a controller or not. When a SmartMedia card is detected, AwYong's controller determines that the SmartMedia card does not have a controller and,

accordingly, engages memory management operations on its behalf. HP 1008 (Dr. Banerjee Decl.), ¶¶ 43, 78. When a CompactFlash card is detected, however, AwYong's controller determines that the CompactFlash card has a controller for error correction and, accordingly, does not engage such memory management operations. *Id.* at ¶¶ 50, 78.

AwYong determines card type via a "storage card-interface control register" (part of the Control Register Module) that detects the type of card inserted. HP 1002, pp. 48-49. This register is "[r]esponsible for transmission interface switching control. When different memory cards are applied, their transmission interfaces and control logic circuits may be different, and the controller uses this register to perform switching operations." *Id.*

v. "in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section"

AwYong's controller uses firmware to perform error correction and bad block mapping upon the insertion of a SmartMedia card (a controllerless card) but not upon the insertion of an MMC or CompactFlash card (cards with controllers). HP 1002, p. 23, Fig. 2-2. As shown in Figure 7, *supra*, the controller chip includes interfaces for the various memory card types. *Id.* at 23, 50-75, Fig. 2-2.

The SmartMedia Interface includes an SM_ECC module, as shown in FIG. 5-4

of AwYong (reproduced as Figure 8, *infra*), which handles error correction for the SmartMedia card. *Id.* at 56, 63, 65, 66, Fig. 5-4.

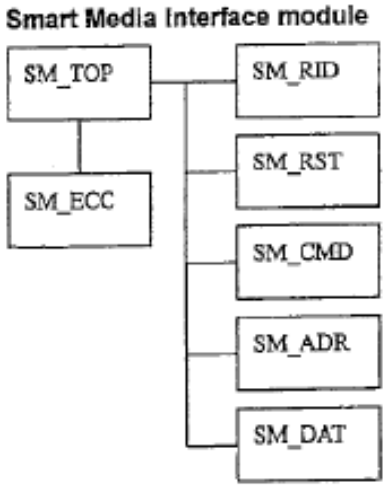


Figure 8: FIG. 5-4 of AwYong

AwYong describes this ECC (error correcting code) module as follows:

> Error Correcting Code: when data is stored, to avoid the damage to data during transmission or data damage due to the damage of the memory itself and to prevent errors in writing data into the Smart Media, data is encoded before being written into the Smart media. In this case, a group of codes is generated after encoding. This group of codes is stored in a special place in the Smart Media. When the data is read out, decoding is made to check whether any data error occurs. If yes, the error is corrected. *Id.* at 63.

The interface modules for CompactFlash and MMC cards, on the other hand, do not contain an ECC module, because those cards (unlike SmartMedia cards) have an on-card controller that performs error correction. *Id.* at 66, Fig. 5-8. Thus, there is no need for an ECC module in the CompactFlash and MMC card interface modules.

AwYong also discloses bad block mapping operations performed by the controller chip for SmartMedia cards, but not for MMC or CompactFlash cards. AwYong describes replacing damaged blocks with spare blocks. *Id.* at 32. Specifically, AwYong describes the process by which the "Block Status records whether [a] block is good or damaged" and "block address mapping" for use with SmartMedia cards. *Id.* at 33-35. As part of memory management operations, this bad block mapping for SmartMedia cards is performed by the controller chip because the "single-chip controller must be capable of enforcing these management specifications to manage the memories inside Smart Media storage cards." *Id.* at 17.

Furthermore, AwYong discloses that the controller chip uses firmware to perform the error correction and bad block mapping operations for SmartMedia cards. AwYong describes that various functions, including memory management, are part of the "firmware design part," including "automatic data error detection and correction (ECC=error correcting code) ... of the Smart Media Card Interface." *Id.* at 41.

2. Dependent Claim 19 – "wherein the flash adapter further comprises a plurality of interfaces for receiving a plurality of flash storage systems"

AwYong's controller chip has interface modules for various types of flash storage systems (cards), including SmartMedia cards (which do not have a controller) and CompactFlash and MMC cards (which do have a controller). HP 1002, pp. 14, 17,

20, 23, 50-75, Fig. 2-1, 2-2.

3. Independent Claim 11

i. "a computing device"

AwYong describes a system in which a controller chip allows host computing devices (*e.g.*, desktop or notebook PCs) to use various types of flash memory cards. HP 1002, pp. 14-17, 23, Fig. 2-2. The computing device is shown as a PC in FIG. 2-2 of AwYong (reproduced as Figure 7, *supra*). *Id.* at 14-17, 23, Fig. 2-2.

ii. "a flash storage system comprising a flash section and at least a portion of a medium ID"

As discussed in Section VII.A.1.iii, *supra*, AwYong discloses CompactFlash, SmartMedia, and MMC flash storage systems. *See id.* at 14, 17, 23, Fig. 2-2. Each card type includes flash memory and a medium ID as defined by the cards' specifications. HP 1018, p. 28 (MMC); HP 1017, pp. 50-59 (CF); HP 1025, p. 15 (SmartMedia); HP 1008 (Dr. Banerjee Decl.), ¶¶ 44-45, 51-52, 58-59.

iii. "a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device"

AwYong's controller chip interfaces host computing devices (*e.g.*, desktop or notebook PCs) to various flash memory cards. HP 1002, pp. 14-17, 23, Fig. 2-2. As shown in FIG. 2-2 of AwYong (reproduced as Figure 7, *supra*), the controller chip interfaces with multiple types of flash storage systems—including SmartMedia, CompactFlash, and MMC. *Id.*

iv. "the controller chip comprising an interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems"

As described in Section VII.A.1.i, *supra*, and as shown in FIG. 2-2 of AwYong (reproduced as Figure 7, *supra*), AwYong's controller chip has multiple interface modules to accept multiple types of flash storage systems—including SmartMedia cards (which do not have a controller), and CompactFlash and MMC cards (which do have a controller). *Id.* at 14-17, 23, 50-75, Fig. 2-2.

v. "a detector to determine whether the flash storage system includes a controller for error correction"

As discussed in Section VII.A.1.iv, *supra*, AwYong describes a detector (card detect pins) to determine whether the flash storage systems include a controller or not. *See id.* at 14, 17, 23, 48-49, 54, 56, 58, Figs. 2-2, 5-3, 5-4, 5-5.

vi. "a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section"

As discussed in Section VII.A.1.v, *supra*, AwYong discloses firmware to perform error correction and bad block mapping for controllerless flash storage systems. *See id.* at 23, 33-35, 41, 50-75, Fig. 2-2, Fig. 5-4, Fig. 5-8.

4. Dependent Claim 21 – "wherein the flash adapter further comprises a plurality of interfaces for receiving a plurality of flash storage systems"

AwYong's controller chip has interface modules for various types of flash

storage systems (cards), including SmartMedia cards (which do not have a controller) and CompactFlash and MMC cards (which do have a controller). *See* HP 1002, pp. 14, 17, 20, 23, 50-75, Figs. 2-1, 2-2.

5. AwYong Claim Chart

Claim Language	Disclosure in AwYong (HP 1002)
7. A method comprising:	AwYong's controller chip performs the method recited by claim 7.
using a controller chip to interface a flash storage system with or without a controller to a computing device,	AwYong describes a single controller chip that allows host computing devices to use various types of flash memory cards, including SmartMedia cards (which do not have a controller) and CF and MMC cards (which do have a controller). *See* pp. 14, 17, 23, Fig. 2-2.
the controller chip comprising a flash adapter,	AwYong's controller chip comprises a flash adapter section in the form of interface modules for each type of card read by the chip. *See* pp. 14, 23, 50-75, Fig. 2-2.
wherein the flash storage system comprises a flash section and at least a medium ID;	AwYong's system is compatible with multiple types of flash storage systems, including CompactFlash, SmartMedia, and MMC cards, each of which have a flash section (memory) and a medium ID. *See* pp. 14, 17, 23, Fig. 2-2; *see also* HP 1018, p. 28 (MMC); HP 1017, pp. 50-59 (CF); HP 1025, p. 15 (SmartMedia); HP 1008 (Dr. Banerjee Decl.), ¶¶ 44-45, 51-52, 58-60.
determining whether the flash storage system includes a controller for error correction; and	AwYong describes a "storage card-interface control register" that distinguishes controller-based cards from controller-less cards. *See* pp. 48-49. AwYong's system is compatible with cards both with (CF, MMC) and without (SmartMedia) an on-card controller and engages different processes for them, particularly for error correction and bad block mapping discussed *infra*.
in an event where the flash storage system does not have a controller for	AwYong's SmartMedia Interface includes an SM_ECC module, which handles error correction for SmartMedia

Claim Language	Disclosure in AwYong (HP 1002)
error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.	cards. *See* pp. 56, 63, 65, 66, Fig. 5-4. AwYong's interface modules for CF and MMC cards, on the other hand, do not contain an ECC module, because those cards have on-card controllers that perform error correction. *See* p. 66, Fig. 5-8. AwYong further discloses bad block mapping operations performed by the controller chip for SmartMedia cards (but not for MMC or CompactFlash cards) in a process whereby "[b]lock Status records whether [a] block is good or damaged" and "block address mapping" for use with SmartMedia cards. *See* pp. 33-35. AwYong describes that SmartMedia memory management functions are performed by a "firmware design part." *See* p. 41.
11. A system comprising:	AwYong's controller chip is part of a system.
a computing device;	AwYong describes a system in which a controller chip allows host computing devices to use various types of flash memory cards. *See* pp. 14-17, 23, Fig. 2-2.
a flash storage system comprising a flash section and at least a portion of a medium ID; and	AwYong's system is compatible with multiple types of flash storage systems, including CF, SmartMedia, and MMC cards, each of which have a flash section (memory) and a medium ID. *See* pp. 14, 17, 23, Fig. 2-2; *see also* HP 1018, p. 28 (MMC); HP 1017, pp. 50-59 (CF); HP 1025, p. 15 (SmartMedia); HP 1008 (Dr. Banerjee Decl.), ¶¶ 44-45, 51-52, 58-59.
a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device,	AwYong describes a system in which a controller chip allows host computing devices to use various types of flash memory cards. *See* pp. 14-17, 23, Fig. 2-2.
the controller chip comprising an interface	AwYong describes a single controller chip that allows host computing devices to use various types of flash

Claim Language	Disclosure in AwYong (HP 1002)
mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems,	memory cards, including SmartMedia cards (which do not have a controller) and CF and MMC cards (which do have a controller). *See* pp. 14, 17, 23, Fig. 2-2.
a detector to determine whether the flash storage system includes a controller for error correction and	AwYong describes a "storage card-interface control register" that distinguishes controller-based cards from controller-less cards. *See* pp. 48-49. AwYong's system is compatible with cards both with (CF, MMC) and without (SmartMedia) an on-card controller and engages different processes for them, particularly for error correction and bad block mapping discussed *infra*.
a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.	AwYong's SmartMedia Interface includes an SM_ECC module, which handles error correction for SmartMedia cards. *See* pp. 56, 63, 65, 66, Fig. 5-4. AwYong's interface modules for CF and MMC cards, on the other hand, do not contain an ECC module, because those cards have on-card controllers that perform error correction. *See* p. 66, Fig. 5-8. AwYong further discloses bad block mapping operations performed by the controller chip for SmartMedia cards (but not for MMC or CompactFlash cards) in a process whereby "[b]lock Status records whether [a] block is good or damaged" and "block address mapping" for use with SmartMedia cards. *See* pp. 33-35. AwYong describes that SmartMedia memory management functions are performed by a "firmware design part." *See* p. 41.
19/21. The method / system of claim 7 / 11, wherein the flash adapter further comprises a plurality of interfaces for receiving a plurality of flash storage systems.	AwYong discloses a controller chip with interface modules for multiple types of flash storage systems (cards), including SmartMedia, CompactFlash, and MMC cards. *See* pp. 14, 17, 20, 23, 50-75, Figs. 2-1, 2-2.

B. Battaglia, Alone and in Combination with the Samsung Datasheet, Renders the Challenged Claims Obvious.

As described herein, claims 7, 11, 19, and 21 of the '549 Patent are obvious under 35 U.S.C. § 103 over Battaglia (HP 1004) alone and in combination with the Samsung Datasheet (HP 1006).

1. Independent Claim 7

i. "using a controller chip to interface a flash storage system with or without a controller to a computing device"

Battaglia describes an enhanced digital data collector 317 including a processor 320 that is a controller chip to interface flash storage systems to a computing device 338, shown as a "computer, camera, camcorder, PDA, Hi Capacity FDD, HDD, etc." in FIG. 8 of Battaglia (reproduced as Figure 9, *infra*). HP 1004, 14:24-31, 14:43-57, 15:66-16:11, Fig. 8.

Battaglia describes compatibility with multiple types of flash storage systems—including SmartMedia cards (which do not have a controller) and CompactFlash, MMC, Memory Stick, and SD cards (which have a controller). *Id.* at 14:24-31, 14:43-47, 15:66-16:11, Figs. 8-9.

ii. "the controller chip comprising a flash adapter"

Battaglia's processor 320 interfaces "each perspective [sic] media" via media interface 322, which would be a "flash adapter" section of controller. HP 1004, 14:43-57, Figs. 8-9. Media interface 322 includes an interface for each type of flash memory

card and "includes the electronics necessary to interface each particular media to local system bus 321." *Id.* at 14:43-57, Figs. 8-9. FIG. 9 of Battaglia (reproduced as Figure 10, *infra*) depicts a block diagram of media interface 322. *Id.* at 14:21-31, 15:66-16:11, Figs. 8-9.

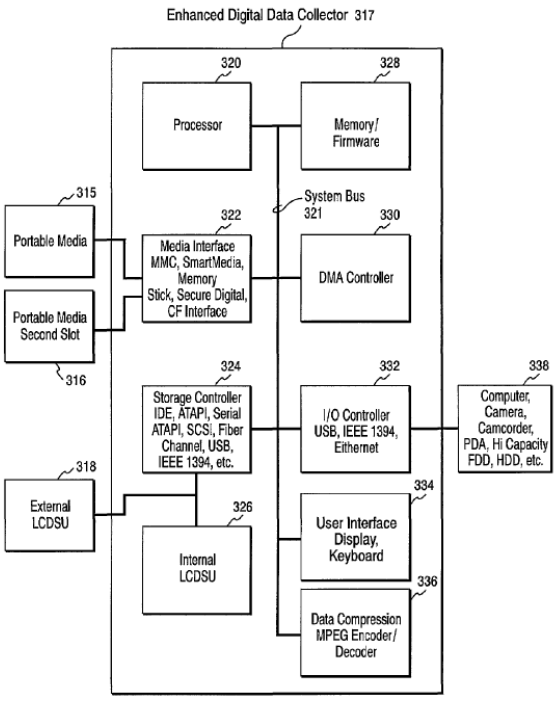


Fig. 8

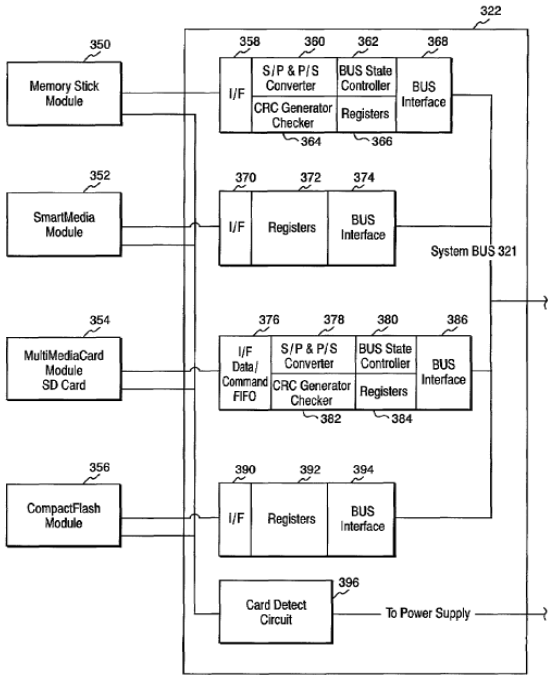


Fig. 9

Figure 9: FIG. 8 of Battaglia

Figure 10: FIG. 9 of Battaglia

iii. "wherein the flash storage system comprises a flash section and at least a medium ID"

Battaglia's system is compatible with multiple types of flash storage systems—including CompactFlash, SmartMedia, MMC, Memory Stick, and SD. *Id.* at 14:24-31, 15:66-16:11, Figs. 8-9. As explained in Section VI.B, *supra*, each of these types of cards comprises a flash section and a medium ID as defined by the cards' specifications. HP

1018, p. 28 (MMC); HP 1019, p. 61, Table 28 (SD); HP 1017, pp. 50-63 (CF); HP 1025, p. 15 (SmartMedia); HP 1021, pp. 21, 70-71 (MS).

iv. "determining whether the flash storage system includes a controller for error correction"

Battaglia's system distinguishes controller-based cards from cards with controllers. As discussed previously, Battaglia describes compatibility with multiple types of flash memory cards, including SmartMedia cards (which do not have a controller) and CompactFlash, MMC, Memory Stick, and SD cards (which have a controller). *Id.* at 14:24-31, 15:66-16:11, Figs. 8-9. Battaglia's processor detects a type of card inserted into a card reader via a card detect circuit and engages different processes based on whether the card has a controller or not. Specifically, Battaglia discloses that the media interface 322 includes a "card detect circuit" 396 "which is operable to sense when any" of the multiple types of flash memory cards "are plugged into the enhanced digital data collector" and which then generates a signal to the power supply to turn on power to the inserted card. HP 1004, 16:12-17, Figs. 8-9. The processor 320 determines, based upon the detection by the card detect circuit, the type of flash memory card inserted. *Id.* at 16:4-23, Figs. 8-9.

Therefore, Battaglia's processor determines whether the flash memory card includes a controller (CompactFlash, MMC, Memory Stick, or SD Cards) for error correction or not (SmartMedia Cards), based on upon the detected type of card and the cards' properties as set forth in the cards' specifications.

v. "… using firmware … to perform operations to manage error correction of the flash section, including bad block mapping …"

Battaglia includes a processor 320 and memory/firmware 328, as shown in FIG. 8 of Battaglia (reproduced as Figure 9, *supra*). *Id.* at 14:51-57, Figs. 8-9. The processor manages data transfers and controls the interfacing of each type of memory card to bus 321. *Id.* at 14:51-57. Processor 320 is coupled to memory 328, which stores program code and firmware executed by the processor in performing the processor's digital data collector management and control tasks. *Id.* at 15:66-16:3, 16:44-49, 16:54-58, 18:1-3, 19:13-19, Figs. 8, 9, 11. Because SmartMedia cards do not have a controller and because Battaglia's system acts as a host controller for SmartMedia cards, SmartMedia error correction and bad block mapping routines are among the "program code/firmware" stored in memory 328 and executed by processor 320 in performing its "management and control" tasks. *Id.* at 15:66-16:3, 16:44-49, 16:54-58, 18:1-3, 19:13-19, Figs. 8, 9, 11.

Accordingly, it would have been obvious to a person of ordinary skill in the art to include error correction operations, such as bad block mapping, as part of Battaglia's "program code/firmware." HP 1008 (Dr. Banerjee Decl.), ¶¶ 95-96. A person of ordinary skill in the art at the time of the effective filing date of the '549 Patent would have known to implement the step of using firmware in the flash adapter to perform operations to manage error correction and bad block mapping for controllerless SmartMedia cards as taught by the SmartMedia Specifications (discussed

previously in Section VI.B.4, *supra*) because it would be at least a simple use/substitution of known elements to obtain predictable results, be obvious to try, and/or be a matter of design choices to comply with SmartMedia protocols. *Id.*

For example, the skilled artisan would have had ample reason to combine the teachings of Battaglia with the Samsung Datasheet, particularly because Battaglia expressly discloses provision of a host for SmartMedia cards. The Samsung Datasheet provides product details about Samsung's SmartMedia card model KRD1208V0M-SSB0 and also includes "SmartMedia Technical Notes" that explain ECC and bad block mapping operations required of the host (system). HP 1006, pp. 9-11. For example, the Samsung Datasheet illustrates a "Program Flow Chart" for "Error Correcting Code," which can be implemented by the host using firmware, as shown in Figure 11, *infra*. *id.*; *see* HP 1008 (Dr. Banerjee Decl.), ¶ 99 ("firmware is merely a type of software, specifically 'software for hardware'").

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart

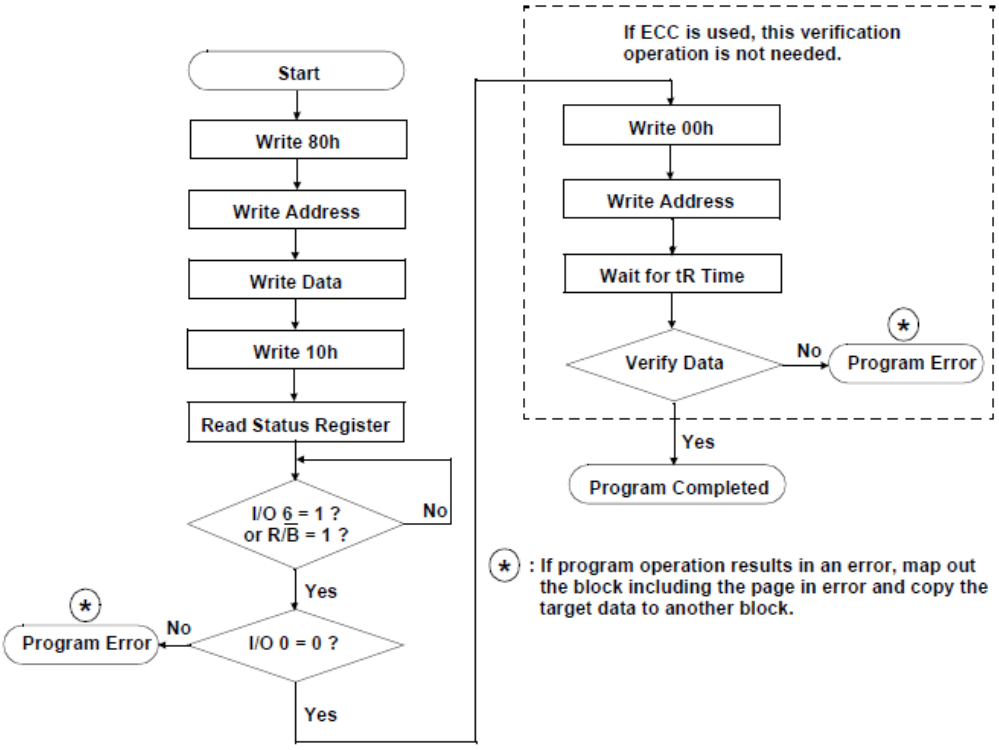


Figure 11: ECC Program Flow Chart in Samsung Datasheet (HP 1006, p. 10)

The Samsung Datasheet also expressly discloses that "[t]he system design must be able to mask out the invalid block(s) via address mapping" and "create the invalid block table via the following suggested flow chart (Figure 1)." HP 1006, p. 9.

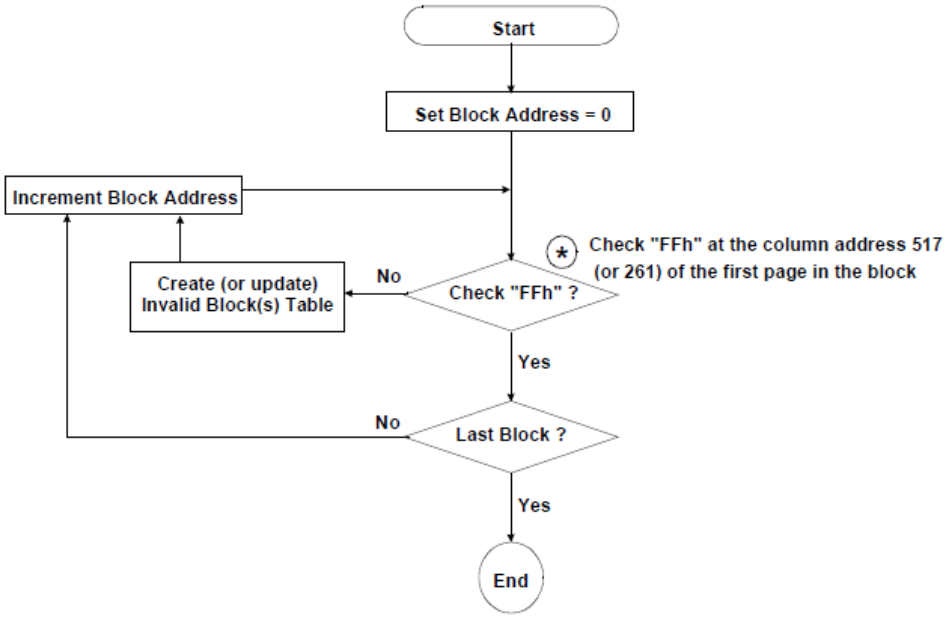


Figure 12: FIG. 1 of the Samsung Datasheet (HP 1006, p. 9)

Moreover, the Samsung Datasheet describes that "additional invalid blocks may develop" and describes a "Block Replacement" scheme. *Id.* at 10.

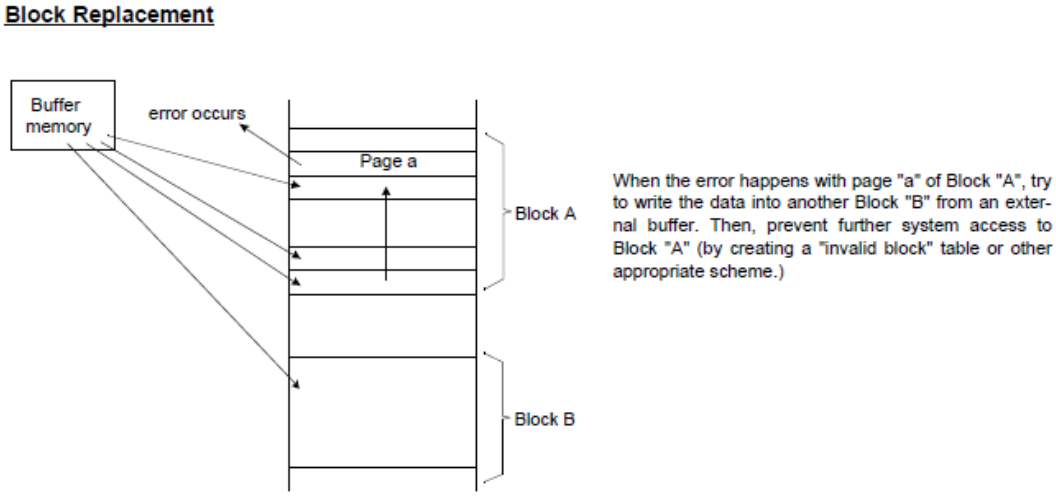


Figure 13: Bad Block Replacement in Samsung Datasheet (HP 1006, p. 11)

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the effective filing date of the '549 Patent to incorporate the Samsung Datasheet's error correction and bad block mapping schemes using firmware for

SmartMedia cards into Battaglia's flash adapter section for interfacing with the same SmartMedia card types "[t]o improve the efficiency of memory space" in the SmartMedia cards. *Id.* at 10. A person of ordinary skill in the art would have been motivated to seek already-existing error correction and bad block mapping schemes for SmartMedia cards, including those described in the Samsung Datasheet. HP 1008 (Dr. Banerjee Decl.), ¶¶ 97, 99, 100. Further, this combination would have been obvious to a person of ordinary skill in the art because as it would have been merely the product of ordinary skill and common sense. *Id.* at ¶ 100.

2. Dependent Claim 19 – "… a plurality of interfaces …"

Battaglia's processor 320 interfaces with a plurality of different flash memory cards via media interface 322, which includes an interface for multiple types of flash memory cards and "includes the electronics necessary to interface each particular media to local system bus 321." HP 1004, 14:24-31, 14:43-57, 15:66-16:11, Figs. 8-9. Digital data collector 317 "include[s] ports for receiving a wide variety of media, such as, MultiMediaCard (MMC), SmartMedia, Memory Stick, Secure Digital, [and] CompactFlash." *Id.* at 14:24-31, 14:43-57, 15:66-16:11, Figs. 8-9.

3. Independent Claim 11

i. "a computing device"

Battaglia's enhanced digital data collector 317 interfaces flash storage systems to a computing device (described as a "computer, camera, camcorder, PDA, Hi Capacity FDD, HDD, etc."). *Id.* at 14:21-24, Figs. 8-9.

ii. "a flash storage system comprising a flash section and at least a portion of a medium ID"

As discussed in Section VII.B.1.iii, *supra*, Battaglia discloses CompactFlash, SmartMedia, MemoryStick, SD, and MMC flash storage systems. *Id.* at 14:24-31, 15:66-16:11, Figs. 8-9. Each card type has both a flash section and a medium ID. HP 1018, p. 28 (MMC); HP 1019, p. 61, Table 28 (SD); HP 1017, pp. 50-63 (CF); HP 1025, p. 15 (SmartMedia); HP 1021, pp. 21, 70-71 (MS).

iii. "a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device"

Battaglia's digital data collector 317 includes a processor 320 (*i.e.*, a controller chip) to interface flash storage systems to a computing device 338, shown as a "computer, camera, camcorder, PDA, Hi Capacity FDD, HDD, etc." in FIG. 8 of Battaglia (reproduced as Figure 9, *infra*). HP 1004, 14:24-31, 14:43-57, 15:66-16:11, Fig. 8.

iv. "the controller chip comprising an interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems"

As described previously, and as shown in FIGS. 8 and 9 of Battaglia (reproduced as Figure 9 and Figure 10, *supra*), Battaglia's processor 320 interfaces "each perspective [sic] media" via media interface 322, which corresponds to the "flash adapter" section of the controller. HP 1004, 14:43-57. The media interface 322 includes an interface for each type of flash memory card and "includes the electronics

necessary to interface each particular media to local system bus 321." *Id.* at 14:43-47 The media interface 322 is capable of receiving multiple types of flash storage systems, including SmartMedia cards (which do not have a controller) and CompactFlash, MMC, Memory Stick, and SD cards (which have controllers). *Id.* at 14:24-31, 14:43-57, 15:66-16:11, Figs. 8-9.

v. "a detector to determine whether the flash storage system includes a controller for error correction"

As discussed in Section VII.B.1.iv, *supra*, Battaglia discloses a detector (card detect pins) to determine whether the flash storage systems include a controller or not. *See id.* at 14:24-31, 14:43-57, 15:66-16:11, 16:12-17, 16:4-23, Figs. 8-9.

vi. "a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping …"

As discussed in Section VII.B.1.v, *supra*, one of ordinary skill in the art would have understood that Battaglia's system could use firmware to perform error correction and bad block mapping for controllerless flash storage systems. *See id.* at 14:43-47, 14:51-57, 15:66-16:3, 16:44-49, 16:54-58, 18:1-3, 19:13-19, Figs. 8-9, 11.

Moreover, and one of skill in the art would have been motivated to combine Battaglia with the Samsung Datasheet as discussed in Section VII.B.1.v, *supra*.

4. Dependent Claim 21 – "… a plurality of interfaces …"

Battaglia's controller chip has interfaces for multiple types of flash storage

systems (cards), including SmartMedia cards (which do not have a controller) and CompactFlash and MMC cards (which do have a controller). *See id.* at 14:24-31, 14:43-57, 15:66-16:11, Figs. 8-9.

5. Battaglia/Samsung Datasheet Claim Chart

Claim Language	Disclosure in Battaglia (HP 1004) and the Samsung Datasheet (HP 1006)
7. A method comprising:	Battaglia's system performs a method in accordance with the claim's limitations.
using a controller chip to interface a flash storage system with or without a controller to a computing device,	Battaglia describes an enhanced digital data collector 317 including a processor 320 that is a controller chip to interface flash storage systems to a computing device 338. HP 1004, 14:24-31, 14:43-57, 15:66-16:11, Fig. 8. Battaglia describes compatibility with multiple types of flash storage systems, including SmartMedia cards (which do not have a controller) and CF, MMC, Memory Stick, and SD cards (which have a controller). *Id.* at 14:24-31, 14:43-57, 15:66-16:11, Figs. 8-9.
the controller chip comprising a flash adapter,	Battaglia describes the processor 320 interfacing "each perspective [sic] media" via media interface 322, which would be "flash adapter" section of controller. HP 1004, 14:43-57, Figs. 8-9. Media interface 322 includes an interface for each of CF, MMC, SD, MemoryStick, and SmartMedia flash memory cards. *Id.*
wherein the flash storage system comprises a flash section and at least a medium ID;	Battaglia's system is compatible with multiple types of flash storage systems, including CF, MMC, SD, MemoryStick, and SmartMedia, each of which have a flash section (memory) and a medium ID. HP 1004, 14:24-31, 15:66-16:11, Figs. 8-9; *see also* HP 1018, p. 28 (MMC); HP 1017, pp. 50-59 (CF); HP 1025, p. 15 (SmartMedia); HP 1008 (Dr. Banerjee Decl.), ¶¶ 44-45, 51-52, 58-59.
determining whether the flash storage system	Battaglia's system distinguishes controller-based cards from controller-less cards. Battaglia discloses that the

Claim Language	Disclosure in Battaglia (HP 1004) and the Samsung Datasheet (HP 1006)
includes a controller for error correction; and	media interface 322 includes a "card detect circuit" 396 "which is operable to sense when any" of multiple types of flash memory cards "are plugged into the enhanced digital data collector" and which then generates a signal to the power supply to turn on power to the inserted card. HP 1004, 16:12-17. A processor 320 determines, based upon the detection by the card detect circuit, the type of flash memory card inserted. *Id.* at 16:4-23. Battaglia's system is compatible with cards both with (CF, MMC, SD, MS) and without (SmartMedia) an on-card controller and engages different processes for them, as discussed *infra*.
in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.	Because Battaglia's system is compatible with SmartMedia cards (which do not have a controller), it would have been obvious to one of ordinary skill in the art to implement error correction and bad block mapping routines as part of the "program code/firmware" stored in memory 328 and executed by processor 320 in performing its "management and control" tasks. HP 1004, 15:66-16:3, 16:44-49, 16:54-58, 18:1-3, 19:13-19, Figs. 8, 9, 11. The skilled artisan would have been motivated to do so by the SmartMedia Specifications, which mandate that a host controller is needed to perform these actions. Moreover, the Samsung Datasheet explains ECC and bad block mapping operations required of the host (system) using SmartMedia cards. HP 1006, pp. 9-11. For example, the Samsung Datasheet illustrates a "Program Flow Chart" for "Error Correcting Code," which can be implemented by the host using firmware. *Id.* It would have been obvious to one of ordinary skill in the art to combine the teachings of the Samsung Datasheet with Battaglia's system "[t]o improve the efficiency of memory space" in the SmartMedia cards. *Id.* at 10.
11. A system comprising:	Battaglia discloses a system for interfacing with flash memory cards. HP 1004, Figs. 8-9.
a computing device;	Battaglia's enhanced digital data collector 317 to interface

Claim Language	Disclosure in Battaglia (HP 1004) and the Samsung Datasheet (HP 1006)
	flash storage systems to a computing device 338. HP 1004, 14:21-24, Figs. 8-9.
a flash storage system comprising a flash section and at least a portion of a medium ID; and	Battaglia's system is compatible with multiple types of flash storage systems, including CF, MMC, SD, MemoryStick, and SmartMedia, each of which have a flash section (memory) and a medium ID. HP 1004, 14:24-31, 15:66-16:11, Figs. 8-9; *see also* HP 1018, p. 28 (MMC); HP 1017, pp. 50-59 (CF); HP 1025, p. 15 (SmartMedia); HP 1008 (Dr. Banerjee Decl.), ¶¶ 44-45, 51-52, 58-59.
a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device,	Battaglia describes the enhanced digital data collector 317 including a processor 320 that is a controller chip to interface flash storage systems to a computing device 338. HP 1004, 14:24-31, 14:43-57, 15:66-16:11, Fig. 8.
the controller chip comprising an interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems,	Battaglia describes compatibility with multiple types of flash storage systems, including SmartMedia cards (which do not have a controller) and CF, MMC, Memory Stick, and SD cards (which have a controller). *Id.* at 14:24-31, 14:43-57, 15:66-16:11, Figs. 8-9.
a detector to determine whether the flash storage system includes a controller for error correction and	Battaglia's system distinguishes controller-based cards from controller-less cards. Battaglia's system has a "card detect circuit" 396 "which is operable to sense when any" of multiple types of flash memory cards "are plugged into the enhanced digital data collector" and which then generates a signal to the power supply to turn on power to the inserted card. HP 1004, 16:12-17. A processor 320 determines, based upon the detection by the card detect circuit, the type of flash memory card inserted. *Id.* at 16:4-23. Battaglia's system is compatible with cards both with (CF, MMC, SD, MS) and without (SmartMedia) an on-card controller and engages different processes for them,

Claim Language	Disclosure in Battaglia (HP 1004) and the Samsung Datasheet (HP 1006)
	as discussed *infra*.
a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.	Because Battaglia's system is compatible with SmartMedia cards (which do not have a controller), it would have been obvious to one of ordinary skill in the art to implement error correction and bad block mapping routines as part of the "program code/firmware" stored in memory 328 and executed by processor 320 in performing its "management and control" tasks. HP 1004, 15:66-16:3, 16:44-49, 16:54-58, 18:1-3, 19:13-19, Figs. 8, 9, 11. The skilled artisan would have been motivated to do so by the SmartMedia Specifications, which mandate that a host controller is needed to perform these actions. Moreover, the Samsung Datasheet explains ECC and bad block mapping operations required of the host (system) using SmartMedia cards. HP 1006, pp. 9-11. For example, the Samsung Datasheet illustrates a "Program Flow Chart" for "Error Correcting Code," which can be implemented by the host using firmware. *Id.* It would have been obvious to one of ordinary skill in the art to combine the teachings of the Samsung Datasheet with Battaglia's system "[t]o improve the efficiency of memory space" in the SmartMedia cards. *Id.* at 10.
19/21. The method / system of claim 7 / 11, wherein the flash adapter further comprises a plurality of interfaces for receiving a plurality of flash storage systems.	Battaglia discloses that the processor 320 interfaces with a plurality of different flash memory cards via media interface 322, which includes an interface for multiple types of flash memory cards and "includes the electronics necessary to interface each particular media to local system bus 321." HP 1004, 14:24-31, 14:43-57, 15:66-16:11, Figs. 8-9.

C. Kobayashi, in View of Kikuchi, Renders the Challenged Claims Obvious.

As described herein, claims 7, 11, 19, and 21 of the '549 Patent are obvious under 35 U.S.C. § 103 over Kobayashi (HP 1005) in view of Kikuchi (HP 1007).

1. Independent Claim 7

i. "using a controller chip to interface a flash storage system with or without a controller to a computing device"

Kobayashi describes a system with a reader/writer 12, which includes a conversion controller 122, an ATA controller 124, and ROM 123 to interface flash memory cards 13 to a computer 11. HP 1005, 5:50-6:49, Figs. 1, 2, 10, 11, 12. Kobayashi discloses four embodiments. The "First Embodiment" describes interfacing with flash memory cards 13 without an on-card controller as shown in FIGS. 1 and 2, and the "Second Embodiment" describes interfacing with flash memory cards 13 with a controller 124 built therein as shown in FIG. 10. *Id.* at 5:50-6:49, 12:41-56, Figs. 1, 2, 10.

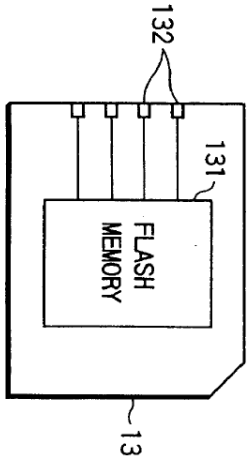


Figure 14: Flash Memory Card Without Controller (FIG. 2 of HP 1005)

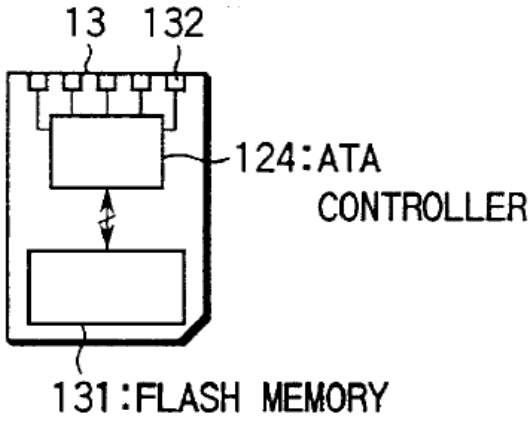


Figure 15: Flash Memory Card With Controller (124) (FIG. 10 of HP 1005)

The "Third Embodiment" describes interfacing with flash memory cards 13 both with and without controllers in a single slot, as shown in FIG. 11, and the "Fourth Embodiment" describes interfacing with flash memory cards 13 both with and

without controllers using multiple slots, as shown in FIG. 12. *Id.* at 12:57-13:51.

ii. "the controller chip comprising a flash adapter"

Kobayashi's controller 122 is a "one-chip microprocessor" with a flash adapter section to interface with flash memory cards 13. *Id.* at 5:66-6:4, 6:12-22, Figs. 1, 2.

iii. "wherein the flash storage system comprises a flash section and at least a medium ID"

Kobayashi's flash memory device 13 includes a flash section as "internal flash memory 131." *Id.* at 5:66-6:4, Figs. 1, 10. This flash memory device 13 also includes a medium ID such as a "CIS (Card Information Structure)." *Id.* at 7:25-32.

iv. "determining whether the flash storage system includes a controller for error correction"

Kobayashi describes a sensor (133/133A/133B) to determine whether the flash memory card 13 includes a controller 124 for error correction. *Id.* at 12:66-13:8, 13:37-50, Figs. 11, 12. "The sensor 133 includes an optical sensor or a microswitch" to detect whether a controller 124 is built into flash memory card 13. *Id.* at 13:9-14. FIG. 11 illustrates Kobayashi's "Third Embodiment," and FIG. 12 illustrates Kobayashi's "Fourth Embodiment":

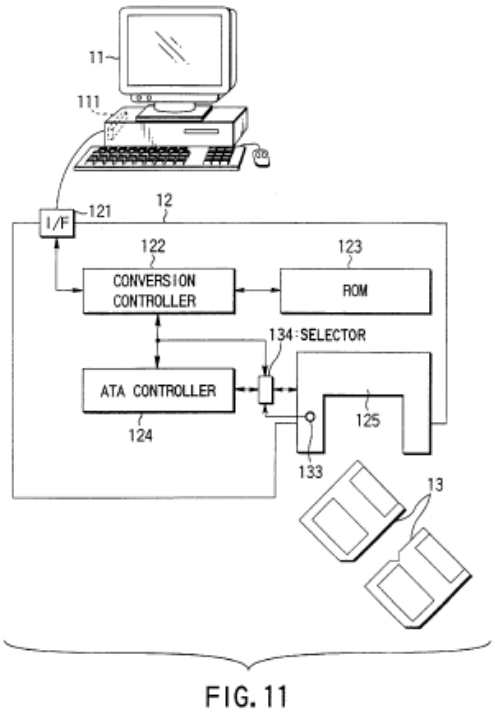


Figure 16: FIG. 11 of HP 1005

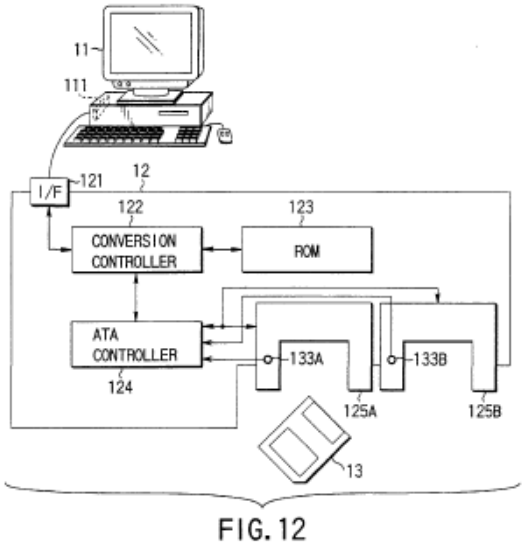


Figure 17: FIG. 12 of HP 1005

With respect to the "Third Embodiment," Kobayashi states:

> An example configuration of this type of reader/writer 12 is shown in FIG. 11. In this configuration, ***a sensor 133 determines the type of the memory card 13*** which is mounted on the connector 125. ***In the case where the result of determination indicates that the memory card 13 includes no ATA controller***, a selector 134 connects the ATA controller 124 and the connector 125. ***In the case where the memory card includes the ATA controller***, on the other hand, the selector 134 connects the conversion controller 122 and the connector 125. HP 1005, 12:66-13:8 (emphasis added).

With respect to the "Fourth Embodiment," Kobayashi states:

> Further, ***the memory card 13 having the ATA controller 124 built therein and the memory card having no ATA controller 124 built***

> *therein can be configured as a common memory card*. In such a case *the sensors 133A, 133B determine which type of memory card is mounted in which slot and notifies the result to the computer 11*. The computer 11 specifies the memory card 13 to be accessed, and issues a read/write command or the like. In the case, *where the designated memory card 13 has the controller 124 built therein*, the conversion controller 122 supplies the ATA command directly to the particular memory card. The *memory card 1 [sic] having no controller 124 built therein*, if accessed, is done so through the ATA controller 124 arranged in the reader/writer 12. *Id.* at 13:37-50 (emphasis added).

Thus, both embodiments determine whether a flash memory card includes a controller for error correction via a detector (sensor 133).

During the '549 Patent's original prosecution, the Patent Owner argued that Kobayashi does not disclose determining whether the flash memory card includes a controller in addition to the entire "firmware" limitation. HP 1015, p. 524. However, as explained above, Kobayashi explicitly teaches a sensor 133 to detect whether a coupled flash memory device 13 includes a controller 124 or not. HP 1005, 12:57-13:51; HP 1008 (Dr. Banerjee Decl.), ¶¶ 109-12.

v. "… using firmware … to perform operations to manage error correction of the flash section, including bad block mapping …"

As discussed previously, Kobayashi describes interfacing with flash memory cards 13 with and without a controller 124 built therein, as shown in FIGS. 11 and 12

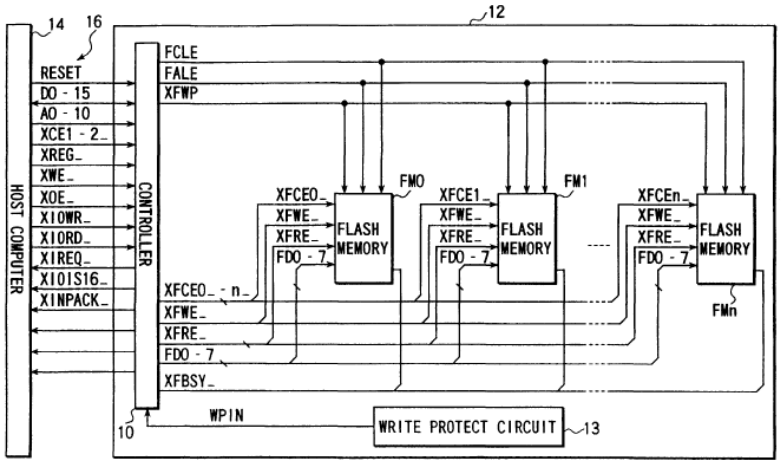
of Kobayashi. HP1005, 12:58-65. When a flash memory card 13 has a controller (124) built therein, selector 134 routes the card directly to conversion controller 122. *Id.* at 12:66-13:8, 13:37-50. However, where the flash memory card 13 does not have an ATA controller 124 built therein, selector 134 routes the card to an external ATA controller 124 provided in reader/writer 12. *Id.*

Kobayashi explains that ATA controller 124 is functionally the same regardless of its location in flash memory card 13 or in external reader/writer 12. *Id.* at 12:43-56 ("The operation of this example is identical to the operation of the first embodiment except that the communication between the conversion controller 122 and the ATA controller 124 (the communication based on the ATA standard) is established though the connector 125."). In fact, Kobayashi uses the same reference number (124) to describe the ATA controller at both locations – whether in flash memory card 13 or outside card 13 in reader/writer 12. *See id.* at Figs. 1, 10.

Controller 124 and conversion controller 122 use firmware to perform memory management operations such as error correction for flash memory card 13. *Id.* at 11:37-46. Kobayashi explains that conversion controller 122 and ATA controller 124 perform various memory management operations including checking "whether or not an error exists in the memory, whether or not the memory is accessible, whether or not there exists an irreparable error, whether or not there exists a hardware error, and whether or not the data are protected." *Id.* Kobayashi, however, is silent on the error

correction operation's details.

However, in the same field of endeavor – flash memory card interfaces – Kikuchi describes a single-chip controller 10, compliant with the ATA protocol (*i.e.*, an ATA controller), that can be provided on a flash memory card or, alternatively, can be provided on an off-card adapter. HP 1007, 7:10-22, 31:2-21, Figs. 1, 2, 15A, 15B. Kikuchi describes a controller 10 to execute read/write operations with respect to flash memory FM0-FMn and a host computer:



F I G. 1

Figure 18: FIG. 1 of Kikuchi

Kikuchi states that its invention "can be applied to a flash memory card in an arbitrary form, e.g., a flash memory card on which an SSFDC [SSFDC is an earlier name for SmartMedia] is detachably mounted." *Id.* at 31:3-7. Consequently, a "controller corresponding to the controller 10 in the above embodiment is incorporated in an adapter card which can be inserted (connected) into a card slot … and the SSFDC is detachably mounted on this adapter card." *Id.* at 31:9-21. Kikuchi's

FIG. 15A shows such an adapter 120 with controller 110 to interface with flash memory cards without an on-card controller built therein. *Id.* at 31:16-21.

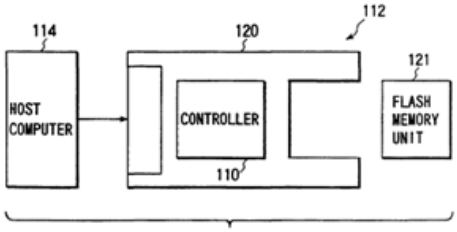


FIG. 15A

Figure 19: FIG. 15A of Kikuchi

Thus, similar to Kobayashi's ATA controller 124, Kikuchi discloses an ATA controller 10 that can be disposed in a flash memory card or in an adapter (controller 110) when the flash memory card has no controller. HP 1008 (Dr. Banerjee Decl.), ¶¶ 114-16.

Kikuchi describes controller 10 as a single chip controller "constituted by a CPU, a ROM, a RAM, an input/output interface circuit, and the like" and complies with "predetermined specifications, e.g., a PCMCIA-ATA." HP 1007, 7:10-22, 9:11-19. FIG. 2 of Kikuchi shows a "functional arrangement of controller 10." *Id.* at 9:14-20. Also, the "controller 10 detects an ECC error" and performs ECC operations in read/write operations accordingly. *Id.* at 28:21-29:2, 11:17-21. Kikuchi describes ECC as an operational program and also describes a "ROM which holds programs required for the operations of the controller." *Id.* at 2:4-10, 5:7-16. Therefore, the controller 10 uses firmware for ECC operations. HP 1008 (Dr. Banerjee Decl.), ¶¶ 118-20.

Moreover, Kikuchi describes bad block mapping by controller 10, including "a block substituting process or the like in the event of a failure or error." HP 1007, 11:17-21. Controller 10 "refers to the block quality flag in the block status information … to check whether the head block BL0 is non-defective or not," and "controller 10 detects a non-defective block BLj having the highest address rank." *Id.* at 21:20-22:5. Thus, Kikuchi discloses a controller using firmware to perform error correction, including bad block mapping, in an adapter (reader/writer) external to the card.

It would have been obvious to one of ordinary skill in the art at the time of the effective filing date of the '549 Patent to incorporate Kikuchi's error correction and ATA controller bad block mapping techniques into ATA controller 124 of Kobayashi "to reliably retain stored data." *Id.* at 4:1-3, 5:7-16; HP 1008 (Dr. Banerjee Decl.), ¶ 121. Because both Kobayashi and Kikuchi describe ATA controller functionality as the same regardless of the controller's location in a flash memory card or in an external adapter, the modified ATA controller 124 in reader/writer 12 of FIGS. 11 and 12 of Kobayashi would perform error correction and bad block mapping as expressly taught by Kikuchi in the event the inserted flash memory card does not have a controller built therein. HP 1005, 12:43-56, Figs. 1, 2, 10; HP 1008 (Dr. Banerjee Decl.), ¶ 121.

For at least the foregoing reasons, combining the ECC and bad block mapping teachings of Kikuchi with the teachings of Kobayashi is merely: (a) a combination of

prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) obvious to try; and/or (d) a matter of design choices and market incentives (*e.g.*, accuracy of flash memory card operations). MPEP § 2143; HP 1008 (Dr. Banerjee Decl.), ¶ 121-22.

2. Dependent Claim 19 – "… a plurality of interfaces …"

Kobayashi's system interfaces with multiple types of flash storage systems as shown in FIG. 12. HP 1005, 13:14-51.

3. Independent Claim 11

i. "a computing device"

Kobayashi describes that a "computer 11 includes a personal computer or the like." *Id.* at 5:59-65, Figs. 1, 10, 11, 12.

ii. "a flash storage system comprising a flash section and at least a portion of a medium ID"

Kobayashi describes that the flash memory device (13) includes a flash section as "internal flash memory 131." *Id.* at 5:66-6:4, Figs. 1, 10. The flash memory device (13) also includes a medium ID, such as a "CIS (Card Information Structure)" *Id.* at 7:25-32.

iii. "a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device"

Kobayashi describes a reader/writer 12, which includes a conversion controller

122, an ATA controller 124, and ROM 123 that interface flash memory cards 13 to computer 11. *Id.* at 5:50-6:49, Figs. 1, 2, 10, 11, 12.

iv. "the controller chip comprising an interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems"

As described previously, Kobayashi's Figs. 11 and 12 both disclose interfacing with flash memory cards (13) both with and without controllers. *Id.* at 12:57-13:51, Figs. 11, 12.

v. "a detector to determine whether the flash storage system includes a controller for error correction"

As discussed in Section VII.C.1.iv, *supra*, Kobayashi discloses a sensor (133/133A/133B) to determine whether the flash memory card (13) includes a controller (124) for error correction, shown in FIGS. 11 and 12. *Id.* at 12:66-13:8, 13:9-14, 13:37-50, Figs. 11, 12; HP 1008 (Dr. Banerjee Decl.), ¶¶ 108-12.

vi. "a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping …"

As discussed in Section VII.C.1.v, *supra*, Kobayashi discloses firmware to perform error correction for controllerless flash storage systems. HP 1005, 11:37-46, 12:43-56, 12:66-13:8, 13:37-50, Figs. 1, 2, 10, 11, 12.

To the extent that Kobayashi does not disclose this limitation, it would have been obvious to a person of ordinary skill in the art, and one of skill in the art would

have been motivated to combine Kobayashi with Kikuchi as discussed in Section VII.C.1.v, *supra*. HP 1008 (Dr. Banerjee Decl.), ¶¶ 121-22.

4. Dependent Claim 21 – "… a plurality of interfaces …"

Kobayashi describes a system that is capable of receiving multiple types of flash storage systems – with or without controllers – with a plurality of interfaces in FIG. 12. HP 1005, 13:14-51.

5. Kobayashi/Kikuchi Claim Chart

Claim Language	Disclosure in Kobayashi (HP 1005) and Kikuchi (HP 1007)
7. A method comprising:	Kobayashi's system performs a method in accordance with the claim's limitations.
using a controller chip to interface a flash storage system with or without a controller to a computing device,	Kobayashi describes a system with a reader/writer 12, which includes an ATA controller 124 to interface multiple types of flash memory cards 13 to a computer 11. HP 1005, 5:50-6:49, Figs. 1, 2, 10, 11, 12. Kobayashi teaches including a controller 124 directly on a card or as part of reader/writer 12. *Id.* at 5:50-6:49, 12:41-56, Figs. 1, 2, 10. Kikuchi also describes interfacing with flash memory cards with (Fig. 1) or without controllers (Fig. 15A). HP 1007, 31:2-21, Figs. 1, 15A.
the controller chip comprising a flash adapter,	Kobayashi describes a conversion controller 122/ATA controller 124 (a "one-chip microprocessor") with a flash adapter section to interface with flash memory cards 13. HP 1005, 5:66-6:4, 6:12-22, Figs. 1, 2. Kikuchi also describes a one-chip controller with a flash adapter section. HP 1007, 7:10-23, 31:2-21, Figs. 1, 2, 15A.
wherein the flash storage system comprises a flash section and at least a	Kobayashi describes that flash memory device (card) 13 includes a flash section: "internal flash memory 131." HP 1005, 5:66-6:4, Figs. 1, 10. This flash memory device also

Claim Language	Disclosure in Kobayashi (HP 1005) and Kikuchi (HP 1007)
medium ID;	includes a medium ID: "CIS (Card Information Structure)." *Id.* at 7:25-32. Kikuchi also describes that the flash memory card includes a flash section FM0-FMn, and also includes the same medium ID as Kobayashi: CIS (Card Information Structure). HP 1007, 7:10-23, 19:24-20:4, Figs. 1, 2, 7.
determining whether the flash storage system includes a controller for error correction; and	Kobayashi describes a sensor 133/133A/133 to determine whether the flash memory card (13) includes a controller (124) for error correction. HP 1005, 12:66-13:8, 13:37-50, Figs. 11, 12. "The sensor includes an optical sensor or a microswitch" to detect whether a controller 124 is built into flash memory card 13. *Id.* at 13:9-14.
in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.	In the case where the flash memory card (13) has an ATA controller (124) built therein, Kobayashi teaches a selector 134 that routes the card directly to conversion controller 122. HP 1005, 12:66-13:8, 13:37-50. However, when the card does not have a controller built therein, selector 134 routes the card to an external ATA controller 124 provided in reader/writer 12. *Id.* Kobayashi's controller 124 is functionally the same regardless of its location in flash memory card 13 or in external reader/writer 12. *Id.* at 12:43-56. In the same field of endeavor – flash memory card interfaces – Kikuchi describes an ATA controller 10 that can be provided on a flash memory or can be provided on an off-card adapter. HP 1007, 31:2-21, Figs. 1, 15A. Kikuchi also describes using firmware in external off-card ATA controller section for error correction operations, including bad block mapping, of coupled flash memory cards. HP 1007, 2:4-10, 5:7-16, 11:17-21, 28:21-29:2,, Figs. 1, 2, 15A. It would have been obvious to incorporate Kikuchi's error correction and bad block mapping techniques of off-card ATA controller 10 into the similar situated ATA controller 124 in the reader/writer 12 of Kobayashi "to reliably

Claim Language	Disclosure in Kobayashi (HP 1005) and Kikuchi (HP 1007)
	retain stored data." HP 1007, 4:1-3, 5:7-16.
11. A system comprising:	Kobayashi describes a system for interfacing with flash memory cards. HP 1005, Figs. 11, 12.
a computing device;	Kobayashi describes a "computer 11." HP 1005, 5:59-65, Figs. 1, 10, 11, 12. Kikuchi also describes a "host computer." HP 1007, Fig. 15A.
a flash storage system comprising a flash section and at least a portion of a medium ID; and	Kobayashi describes that flash memory device (card) 13 includes a flash section: "internal flash memory 131." HP 1005, 5:66-6:4, Figs. 1, 10. This flash memory device also includes a medium ID: "CIS (Card Information Structure)." *Id.* at 7:25-32. Kikuchi also describes that the flash memory card includes a flash section FM0-FMn, and also includes the same medium ID as Kobayashi: CIS (Card Information Structure). HP 1007, 7:10-23, 19:24-20:4, Figs. 1, 2, 7.
a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device,	Kobayashi describes a system with a reader/writer 12, which includes an ATA controller 124 to interface multiple types of flash memory cards 13 to a computer 11. HP 1005, 5:50-6:49, Figs. 1, 2, 10, 11, 12. Kobayashi teaches including a controller 124 directly on a card or as part of reader/writer 12. *Id.* at 5:50-6:49, 12:41-56, Figs. 1, 2, 10. Kikuchi also describes a one-chip controller with a flash adapter section. HP 1007, 7:10-23, 31:2-21, Figs. 1, 2, 15A.
the controller chip comprising an interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems,	Kobayashi describes a conversion controller 122 (a "one-chip microprocessor") with a flash adapter section to interface with flash memory cards 13 both with and without on-card controllers. HP 1005, 5:66-6:4, 6:12-22, Figs. 1, 2. Kikuchi also describes interfacing with flash memory cards with (Fig. 1) or without controllers (Fig. 15A). HP

Claim Language	Disclosure in Kobayashi (HP 1005) and Kikuchi (HP 1007)
	1007, 31:2-21, Figs. 1, 15A.
a detector to determine whether the flash storage system includes a controller for error correction and	Kobayashi describes a sensor (133/133A/133B) to determine whether the flash memory card 13 includes a controller (124) for error correction. HP 1005, 12:66-13:8, 13:37-50, Figs. 11, 12. "The sensor includes an optical sensor or a microswitch" to detect whether a controller (124) is built into flash memory card 13. *Id.* at 13:9-14.
a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.	In the case where the flash memory card 13 has an ATA controller (124) built therein, Kobayashi teaches a selector 134 that routes the card directly to conversion controller 122. HP 1005, 12:66-13:8, 13:37-50. However, when the card does not have a controller built therein, selector 134 routes the card to an external ATA controller 124 provided in reader/writer 12. *Id.* Kobayashi's controller 124 is functionally the same regardless of its location in flash memory card 13 or in external reader/writer 12. *Id.* at 12:43-56. In the same field of endeavor – flash memory card interfaces – Kikuchi describes an ATA controller 10 that can be provided on a flash memory or can be provided on an off-card adapter. HP 1007, 31:2-21, Figs. 1, 15A. Kikuchi also describes using firmware in external off-card ATA controller section for error correction operations, including bad block mapping, of coupled flash memory cards. HP 1007, 2:4-10, 5:7-16, 11:17-21, 28:21-29:2,, Figs. 1, 2, 15A. It would have been obvious to incorporate Kikuchi's error correction and bad block mapping techniques of off-card ATA controller 10 into the similar situated ATA controller 124 in the reader/writer 12 of Kobayashi "to reliably retain stored data." HP 1007, 4:1-3, 5:7-16.
19/21. The method / system of claim 7 / 11, wherein the flash adapter further comprises a	Kobayashi describes a system that is capable of receiving multiple types of flash storage systems – with or without controllers – with a plurality of interfaces in FIG. 12. HP

Claim Language	Disclosure in Kobayashi (HP 1005) and Kikuchi (HP 1007)
plurality of interfaces for receiving a plurality of flash storage systems.	1005, 13:14-51.

VIII. Conclusion

For the foregoing reasons, Petitioner respectfully requests that *inter partes* review be instituted for the '549 Patent and that claims 7, 11, 19, and 21 be cancelled.

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,162,549 and associated Exhibits 1001-1030 were served on March 27, 2013, via Express Mail upon the following:

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