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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SYNOPSYS, INC.
Petitioner

v.

MENTOR GRAPHICS CORPORATION
Patent Owner

Case IPR2012-00041
Patent 6,947,882 B1

Before SALLY C. MEDLEY, HOWARD B. BLANKENSHIP, and JENNIFER S. BISK, *Administrative Patent Judges.*

BISK, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Synopsys, Inc. filed a petition to institute an *inter partes* review of U.S. Patent 6,947,882 B1 (the "'882 patent"). 35 U.S.C. § 311. For the reasons that follow, the Board, acting on behalf of the Director, has decided not to institute an *inter partes* review. 35 U.S.C. § 314.

OPINION

I. INTRODUCTION

A. Background

Petitioner requests *inter partes* review of claims 1-14 and 17-20 of the '882 patent alleging that each of the claims is unpatentable under 35 U.S.C. §§102 and 103 based on the following prior art references: U.S. 5,960,191 (Ex. 1002) ("Sample '191") including U.S. 5,475,830 (Ex. 1003) ("Chen") incorporated by reference; U.S. 6,020,760 (Ex. 1004) ("Sample '760"); and U.S. 5,761,484 (Ex. 1005) ("Agarwal"). Of the challenged claims, claims 1 and 5 are independent, claims 2-4 depend from claim 1, and claims 6-14 and 17-20 depend from claim 5. The grounds specified by the Petitioner are detailed below.

Reference	**Claims challenged under §§ 102 and 103**
Sample '191 including Chen	1-14, 17-20
Sample '760	5-8, 17-20
Agarwal	5-8, 17, 20

The '882 patent is involved in concurrent district court litigation. On August 17, 2012, Mentor Graphics filed an infringement complaint against EVE-USA, Inc. and Emulation and Verification Engineering, S.A. *Mentor Graphics v. EVE-USA, Inc.*, 12-cv-01500 (D. Or.). That proceeding has not been stayed and currently has a Markman hearing scheduled for July 23, 2013 and a five day jury trial set for June 16, 2014. Minutes of Tel. Conference, *Id.* (Dec. 12, 2012), ECF No. 60.

B. The ’882 patent (Ex. 1001)

The ’882 patent generally relates to systems for emulating integrated circuit designs. ’882 col. 1, ll. 8-9. In particular, the patent describes a “regionally time multiplexed emulation system”—an emulation system with increased capacity over the prior art due to an emulator separated into different regions, each region constituting a separate time domain. *See* ’882 Abstract; col. 11, 41-42. The patent states that this separation of the emulator into separate time domain regions allows asynchronous logic to be emulated without hard-wiring signals to dedicated pins and reduces the problem of synchronizing clock signals across a large area. ’882 col. 11, ll. 41-49.

The challenged claims encompass two independent claims, reproduced below, with emphasis added:

1. An emulation system comprising:

   a first plurality of reconfigurable logic devices;

   a second plurality of reconfigurable logic devices;

   a third plurality of reconfigurable logic devices;

   a first time multiplexed interconnection coupled to and situated between the first plurality of reconfigurable logic devices and the second plurality of reconfigurable logic devices; and

   a second time multiplexed interconnection coupled to and situated between the second plurality of reconfigurable logic devices and the third plurality of logic devices, *wherein clocking of the second time multiplexed interconnection is independent of clocking of the first time multiplexed interconnection*.

5. An emulator for emulating a circuit design, comprising:

a first reconfigurable logic device that includes a first plurality of reconfigurable logic elements and first input/output circuitry;

a second reconfigurable logic device that includes a second plurality of reconfigurable logic elements and second input/output circuitry;

a first clock signal for clocking the first plurality of reconfigurable logic elements;

a second clock signal for clocking the second plurality of reconfigurable logic elements; and

at least one signal routing clock signal for clocking at least one of the first input/output circuitry and the second input/output circuitry, *wherein the signal routing clock signal is independent of the first clock signal and the second clock signal*.

II. DECISION ON PETITION

A. Overview

For the reasons described below, we decline to institute an *inter partes* review of any of the challenged claims based on any of the proposed grounds.

B. Claim Construction

As a step in our analysis for determining whether to institute a trial, we determine the meaning of the claims. Consistent with the statute and the legislative history of the AIA, the Board will interpret claims using the broadest reasonable construction. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48756, 48766 (Aug. 14, 2012); 37 CFR § 100(b). There is a "heavy presumption" that a claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp*., 288 F.3d 1359, 1366 (Fed. Cir. 2002). By "plain meaning" we refer to the

ordinary and customary meaning the term would have to a person of ordinary skill in the art. Such terms have been held to require no construction. *See, e.g., Biotec Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc.*, 249 F.3d 1341, 1349 (Fed. Cir. 2001) (finding no error in non-construction of "melting"); *Mentor H/S, Inc. v. Med. Device Alliance, Inc.*, 244 F.3d 1365, 1380 (Fed. Cir. 2001) (finding no error in court's refusal to construe "irrigating" and "frictional heat").

Petitioner submits that for purposes of this review, the claim terms take on the ordinary and customary meaning that the terms would have to one of ordinary skill in the art. Pet. 5. Patent Owner does not appear to dispute this. *See generally* Prelim. Resp. With one exception, we agree that for purposes of this decision the claim terms require no construction and we give those claims their plain and ordinary meaning in the context of the specification.

The one exception is "wherein clocking of the second time multiplexed interconnection is independent of clocking of the first time multiplexed interconnection" as required by independent claim 1 or "wherein the signal routing clock signal is independent of the first clock signal and the second clock signal" as required by independent claim 5 (collectively, the "independent clock signal limitation"). Petitioner implicitly asserts that the independent clock signal limitation encompasses asynchronous clock signals originating from a single clock. For example, in a claim chart, Petitioner cites, without further explanation, the following text in Sample '191 and Chen as disclosing the independent clock signal limitation.

A High Speed Asynchronous Clock Signal **144** is distributed to all chips in

> the system. **Unlike the Mux Clock 44 described earlier with reference to FIG. 2, Asynchronous Clock Signal 144 need not be synchronized between any two chips in the system or even between two pins on the same chip.** Therefore, there is no need for a SYNC-Signal **48** as described earlier with reference to FIG. **2**. Also, Asynchronous Clock Signal **144** may operate at any speed as long as the minimum pulse width produced on External Signal **144** will pass through the interconnect without undue degradation.

Pet. 17, 25 (citing Sample '191 col. 11, ll. 41-51) (emphasis added by Petitioner).

> **Any pair of clock signals from different clock trees are assumed "asynchronous."**

Pet. 17, 25 (citing Chen col. 10, ll. 18-19) (emphasis added by Petitioner).

According to Patent Owner, asynchronous clocks are not necessarily independent. Prelim. Resp. 8, 18. And in the context of the '882 specification, the independent clock signal limitation does not encompass asynchronous signals created by a single clock. *Id.* at 8, 18.

We agree with Patent Owner that the term "asynchronous" is not synonymous with "independent." The plain and ordinary meaning of "independent" is "not affiliated with a larger controlling unit."[1] Thus, the plain and ordinary meaning of the independent clock signal limitation requires that the two independent clock signals are not affiliated with one controlling clock and instead the signals originate from separate clocks. Nothing in the specification indicates

[1] See Mirriam-Webster dictionary definition of independent "not affiliated with a larger controlling unit." http://www.merriam-webster.com/dictionary/independent?show=0&t=1358972086 (last visited Jan. 28, 2013).

that "independent" should be interpreted in another way. For instance, when describing Figure 5, the specification refers to clock signals 508 and 509 as independent of each other and clock signal 510 as independent of clocks 508 and 511. '882 patent col. 6, ll. 18-21; col. 7, ll. 21-24. Figure 5 is reproduced below:

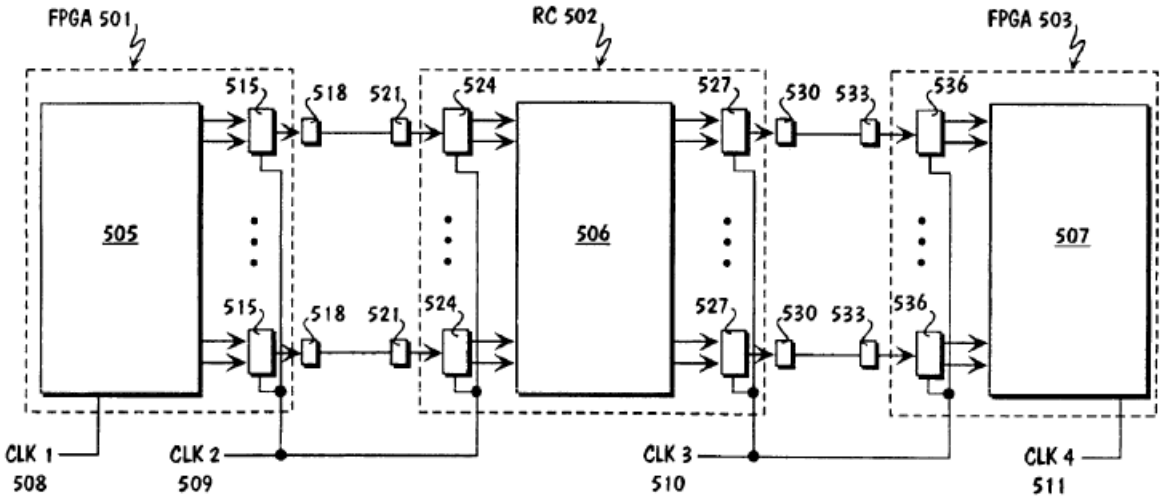

Figure 5, above, is a block diagram illustrating the concept of regional time multiplexing according to one embodiment of the '882 invention. '882 patent, col. 2, ll. 42-44. None of the clocks, 508-511, are shown as being derived from a single controlling clock. Petitioner does not provide analysis or direct us to any persuasive evidence that the independent clock signal limitation should be construed to include signals that are derived from a single clock. *See generally*, Pet. Thus, for purposes of this decision, we interpret the independent clock signal limitation to require that each of the independent clock signals have as a source a separate and independent clock.

C. Sample ’191

1. The petition’s Arguments Regarding Sample ’191 Were not Previously Considered by the Office

Patent Owner asserts that all the references asserted in the petition are the same or substantially the same as prior art considered during prosecution. In particular, Sample ’191 was applied as a basis of rejecting the disputed claims during prosecution of the ’882 patent. Prelim. Resp. 7-10.

“In determining whether to institute or order a proceeding . . . the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments were presented to the Office.” 35 U.S.C. § 325(d). Although applied during prosecution, the Examiner cited Sample ’191 explicitly for the disclosure of a “bidirectional transfer connection” limitation contained in claims that were subsequently cancelled in response to a restriction requirement. *See* Ex. 1010, 1011, 1012. While the Examiner later rejected the challenged claims over Sample ’191, these claims do not contain the “bidirectional transfer connection” limitation; therefore this appears to be an oversight. *See* Response to Office Action, Ex. 1014 at 11-12 (“[T]he Office’s remarks relating to the rejection based on Sample . . . do not appear to relate in any respect to the content of independent claims 13 and 23 in this application. Rather, these remarks appear to relate to the content of non-elected claims 17-22.”).

Thus, we are not persuaded that the petition’s arguments regarding Sample ’191 and the challenged claims were previously considered by the Office. We decline to reject the petition solely on the ground that Sample ’191 was considered

by the Examiner during prosecution.

2. Anticipation

Petitioner asserts that claims 1-14 and 17-20 are anticipated by Sample '191. Sample '191 describes a "hardware emulation system which reduces hardware cost by time-multiplexing multiple design signals onto physical logic chip pins and printed circuit board." Abstract.

Petitioner asserts that because Sample '191 incorporates Chen by reference Chen is "part of the anticipatory disclosure" of Sample '191. Pet. 11. "To incorporate material by reference, the host document must identify with detailed particularity what specific material it incorporates and clearly indicate where that material is found in the various documents." *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000). "The standard is whether one reasonably skilled in the art would understand the application as describing with sufficient particularity the material to be incorporated." *Harari v. Lee*, 656 F.3d 1331, 1334 (Fed. Cir. 2011). The language used in Sample '191 unambiguously incorporates the entire Chen specification. Sample '191 col. 2, ll. 27-31 ("A method for performing this analysis and separation is disclosed in U.S. Pat. No. 5,475,830 by Chen et al, which is assigned to the same assignee as the present invention. The disclosure of U.S. Pat. No. 5,475,830 is herein incorporated by reference in its entirety."). Because a document incorporated by reference "becomes effectively part of the host document as if it were explicitly contained therein," *Telemac Cellular Corp. v. Topp Telecom, Inc.* 247 F.3d 1316, 1329 (Fed. Cir. 2001), we agree, and Patent Owner does not dispute, that Chen, in its entirety,

constitutes part of the Sample ’191 reference for purposes of anticipation analysis.

Patent Owner argues that Sample ’191, even including the disclosure of Chen, does not anticipate the challenged claims. Prelim. Resp. 13-26. Specifically, Patent Owner asserts that Sample ’191 does not disclose the independent clock signal limitation required by all the challenged claims. Prelim. Resp. 13-14, 22-23.

Petitioner’s argument that Sample ’191 anticipates the challenged claims states that Sample ’191 “explicitly or inherently discloses every element of each challenged claim, including the alleged point of novelty—independent clocks.” Pet. 11. Petitioner does not specifically identify which, if any, element of the claims is not explicitly, but is inherently disclosed by Sample ’191. *See* Pet. 10-13, 14-39 (claim chart for Sample ’191). Thus, we assume that Petitioner’s argument is that every element is explicitly disclosed. As described above, in a claim chart, Petitioner cites, without further explanation, the following text in Sample ’191 and Chen as disclosing the independent clock signal limitation.

> A High Speed Asynchronous Clock Signal **144** is distributed to all chips in the system. **<u>Unlike the Mux Clock 44 described earlier with reference to FIG. 2, Asynchronous Clock Signal 144 need not be synchronized between any two chips in the system or even between two pins on the same chip.</u>** Therefore, there is no need for a SYNC-Signal **48** as described earlier with reference to FIG. **2**. Also, Asynchronous Clock Signal **144** may operate at any speed as long as the minimum pulse width produced on External Signal **144** will pass through the interconnect without undue degradation.

Pet. 17, 25 (citing Sample ’191 col. 11, ll. 41-51) (emphasis added by Petitioner).

> **<u>Any pair of clock signals from different clock trees are assumed “asynchronous.”</u>**

Pet. 17, 25 (citing Chen col. 10, ll. 18-19) (emphasis added by Petitioner).

Patent Owner asserts that both Sample '191 and Chen use the term "asynchronous" only to describe a single global clock whose input at different chips or pins does not have to be synchronized. Prelim. Resp. 8. We agree. Petitioner does not explain why the cited language of Sample '191 and Chen discloses the independent clock signal limitation as opposed to just clock signals from a single clock source that are not synchronized. Thus, based on our construction of the independent clock signal limitation, we are not persuaded that the language quoted above supports a finding that the limitation is explicitly disclosed by Sample '191 or Chen.

The only other language cited by Petitioner as disclosing the independent clock signal limitation is:

> On control board **600**, a Mux chip **12** is used to **select a combination of clocks** from all of the different potential sources. **The system may have up to thirty-two distinct clock sources. Any eight of these may be used** on a pair of emulation boards **200**. **This allows different pairs of emulation boards 200 to have different clocks as might be required, for example, when more than one chip design was being emulated** in a single hardware emulation system. Clocks are routed through programmable delay element **604** and buffers **614** then through backplane **800** or **802** to emulation boards **200**.

Pet. 17, 25(citing Sample '191 col. 19, ll. 56-66) (emphasis added by Petitioner).

Patent Owner argues that the quoted language discloses a general capability of the system to use different clocks, but does not explicitly disclose that the different clock signals are used simultaneously, by the same logic device, or to clock different multiplexed interconnects. Prelim. Resp. 20. While we agree with

the Petitioner that the quoted language explicitly describes at least two independent clock signals, we are not persuaded that any of the quoted language explicitly describes (1) that the independent clock signals are used to clock different multiplexed interconnects as required by claim 1, or (2) that the signals are used as a routing signal independent from two clock signals for clocking reconfigurable logic elements as required by claim 5. As pointed out by the Patent Owner, anticipation requires more than simply disclosing every element of the challenged claims, it also requires that the anticipatory reference disclose those elements "arranged as in the claim." *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369-70 (Fed. Cir. 2008).

Petitioner does not explain how Sample '191 or Chen explicitly discloses that the several distinct clocks are used "to clock different multiplexed interconnects" or as "a routing signal independent from two clock signals for clocking reconfigurable logic elements" as required by the challenged independent claims. In fact, the cited text of Sample '191 states only that the independent clocks may be used on different emulation boards to be used when "for example, more than one chip design was being emulated." The '882 specification, however, makes it clear that the independent clock signal limitation may be used with the emulation of a single circuit design. *See, e.g.*, '882 patent, col. 2, ll. 13-19 ("The reconfigurable logic devices are reconfigurable to emulate *a circuit design* using at least one user clock . . . and at least one signal routing clock . . . being independent of the at least one user clock."); Fig. 5. The language Petitioner cited from Sample '191, however, is silent as to whether the independent clocks may be used on two multiplexed

interconnections within a single emulation system as required by claim 1, or on the input/output circuitry of the reconfigurable logic devices within an emulator as required by claim 5.

We are therefore not persuaded by Petitioner's argument that these elements are "arranged as in the claim," therefore precluding anticipation of claims 1-14 and 17-20 by Sample '191 and Chen.

3. Obviousness

Petitioner asserts that, under 35 U.S.C. § 103, to the extent not anticipated by Sample '191, claims 1-14 and 17-20 would have been obvious to a person of ordinary skill in the art in view of Sample '191. Pet. 10. Patent Owner argues that Petitioner provides no rationale to support such an assertion. Prelim. Resp. 12-13, 22, 26.

Petitioner refers to the ground of obviousness over the '191 patent in several places. For example, in the Section entitled "The specific art and statutory ground(s) on which the challenge is based," Petitioner asserts that "[t]he '191 patent both anticipates (under 35 U.S.C. ¶102) and renders obvious (under 35 U.S.C. § 103) claims 1-14 and 17-20 of the '882 patent." Pet. 4. Next, in the section of the petition entitled "Summary of Invalidity Arguments," Petitioner states that "[t]o the extent not anticipated by the '191 patent, each of the claims would have been obvious to a person of ordinary skill in the art in view of the '191 patent" (Pet. 10) and "[a]t a minimum, each challenged claim element would have been obvious to a person of ordinary skill in the art in view of the '191 patent" (Pet. 11). However, Petitioner does not clearly explain the reasoning behind these unsupported

assertions.

The petition must identify with particularity each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim. 35 U.S.C. § 312(a)(3). Per 37 C.F.R. § 42.22(a), each petition must include a statement of the precise relief requested and a full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, the governing law, rules, and precedent. Under 37 C.F.R. § 42.104(b)(4), the petition must specify where each element of a challenged claim is found in the prior art patents or printed publications. In accordance with 37 C.F.R. § 104(b)(5), the relevance of the evidence supporting the challenge must be provided including identification of specific portions of the evidence that support the challenge.

Petitioner's conclusory statements, without more detail, fail to satisfy any of the above-noted requirements and are irreparably lacking in detail. Petitioner does not clearly provide analysis to support the assertion of obviousness over Sample '191. The petition does not clearly point out the differences between the claimed invention and Sample '191. Nor does Petitioner explain why a person of ordinary skill in the art would have found the claimed subject matter obvious in spite of those differences. Petitioner has not provided sufficient reasoning or facts on which to base a conclusion that a person of ordinary skill in the art would have found it obvious, in light of Sample '191's disclosure of independent clocks, to use clock signals from any of the described clocks in the manner required by the challenged claims. Because Petitioner has failed to demonstrate a reasonable likelihood that it

would prevail on such ground of unpatentability, we decline to institute an *inter partes* review on the basis that claims 1-14 and 17-20 are obvious over Sample ’191.

D. Sample ’760

1. Anticipation

Petitioner asserts that claims 5-8 and 17-20 are anticipated by Sample ’760. Sample ’760 describes an “integrated circuit for implementing reconfigurable logic . . . with flexible input/output buffers.” Abstract. We are not persuaded that there is a reasonable likelihood that the challenged claims are anticipated by Sample ’760.

For example, it is unclear from the petition, what signal in Sample ’760 equates to the “first clock signal for clocking the first plurality of reconfigurable logic elements” or the “second clock signal for clocking the second plurality of reconfigurable logic elements” as required by all the challenged claims. The only specific discussion of these elements is found in the claim chart. Pet. 41-42. The claim chart cites to language in Sample ’760 referring to the “I/O CLK(I) and I/O CLK(O) signals.” Pet. 41 (citing Sample ’760 col. 11, ll. 9-14). However, Petitioner appears to equate those signals to the “at least one signal routing clock signal” also required by the claims. Pet. 42. The claim chart also cites, in the sections corresponding to the claimed first and second clock signals, to Figure 5, a timing diagram with a list of at least 11 signals. *Id.* (citing Sample ’760 Fig. 5). Petitioner does not specify which of these signals is purported to map to the claimed first and second clock signal. *Id.* Finally, Petitioner cites to language in Sample

’760 referring to “A and B signals,” which are described as data, not clock, signals. *Id.* (citing Sample ’760 col. 10, ll. 21-23); ’760 col. 2, ll. 59-63. Thus, it is unclear which of the many signals listed in the claim chart Petitioner is relying on to disclose the claimed first and second clock signal. Moreover, it is not clear on its face that Sample ’760 discloses all the signals as claimed.

Because the petition does not clearly point to specific language in Sample ’760 that anticipates each element of claims 5-8 and 17-20, we decline to institute an *inter partes* review on the basis of anticipation by Sample ’760.

2. Obviousness

Petitioner asserts that, under 35 U.S.C. § 103, to the extent not anticipated by Sample ’760, claims 5-8 and 17-20 would have been obvious to a person of ordinary skill in the art in view of Sample ’760. Petitioner does not clearly explain the reasoning behind this assertion. The Petitioner does not clearly point out the differences between the claimed invention and Sample ’760. Nor does Petitioner explain why a person of ordinary skill in the art would have found the claimed subject matter obvious in spite of those differences. Petitioner has failed to demonstrate a reasonable likelihood that it would prevail on such ground of unpatentability. Thus, we decline to institute an *inter partes* review on the basis that claims 5-8 and 17-20 are obvious over Sample ’760.

E. Agarwal

1. Anticipation

Petitioner asserts that claims 5-8, 17, and 20 are anticipated by Agarwal.

Agarwal describes "virtual interconnections" to overcome device pin limitations for reconfigurable logic systems. Abstract. We are not persuaded that there is a reasonable likelihood that the challenged claims are anticipated by Agarwal.

Similar to the deficiencies discussed with respect to the Petitioner's argument corresponding to Sample '760, the petition also does not specify what signals in Agarwal equate to the "first clock signal for clocking the first plurality of reconfigurable logic elements" or the "second clock signal for clocking the second plurality of reconfigurable logic elements" as required by all the challenged claims. Again, the only specific discussion of these elements is found in the claim chart. Pet. 50-52. The claim chart cites to Figure 4 and corresponding language in the text of Agarwal. Pet. 50-51 (citing Agarwal Fig. 4, col. 4, ll.3-4, col. 5, ll. 25-39, col. 6, ll. 26-49). This Figure and text, however, describes "an emulation phase clocking scheme" with an "emulation clock," and a "pipeline clock." It is unclear, which, if any of these signals is being relied upon for disclosing the claimed first and second clock signal because these same portions of Agarwal are cited in the claim chart as supporting the disclosure of the claimed "the signal routing clock signal." Pet. 52-53. In addition to not mapping the cited signals of Agarwal to the claimed signals, the claim chart does not make clear how Agarwal discloses that the claimed "signal routing clock signal" is "independent of the first clock signal and the second clock signal" as required by all the challenged claims. Moreover, it is not clear on its face that Argawal discloses these signals as claimed.

Because the petition does not clearly point to where each element of the claim is found in Agarwal that anticipates each element of claims 5-8, 17, and 20,

we decline to institute an *inter partes* review on the basis of anticipation by Agarwal.

2. Obviousness

Petitioner asserts that, under 35 U.S.C. § 103, to the extent not anticipated by Agarwal, claims 5-8, 17, and 20 would have been obvious to a person of ordinary skill in the art in view of Agarwal. Again, Petitioner does not clearly explain the reasoning behind this assertion. The Petitioner does not point out the differences between the claimed invention and Agarwal. Nor does Petitioner explain why a person of ordinary skill in the art would have found the claimed subject matter obvious in spite of those differences. Petitioner has failed to demonstrate a reasonable likelihood that it would prevail on such ground of unpatentability. Thus, we decline to institute an *inter partes* review on the basis that claims 5-8, 17, and 20 are obvious over Agarwal.

F. Conclusion

Because the petition does not demonstrate that there is a reasonable likelihood that at least one of the challenged claims is unpatentable based on the asserted grounds, we decline to institute *inter partes* review as to any of the challenged claims.

III. DECISON

In consideration of the foregoing, it is hereby

ORDERED that the petition is denied as to claims 1-14 and 17-20 of the ’882 patent.

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