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Paper No. 34
Filed: December 14, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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DIABLO TECHNOLOGIES, INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

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Case IPR2014-01011
Patent 7,881,150 B2

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Before LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

BRADEN, *Administrative Patent Judge*.

# FINAL WRITTEN DECISION
*35 U.S.C. § 318 and 37 C.F.R. § 42.73*

# I. INTRODUCTION

We have jurisdiction to hear this *inter partes* review under 35 U.S.C. § 6(c). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons that follow, we determine that Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of US Patent No. 7,881,150 B2 (Ex. 1001, "the '150 patent") are unpatentable.

## *A. Procedural History*

Diablo Technologies, Inc. ("Petitioner") filed a Corrected Petition (Paper 5, "Pet.") to institute an *inter partes* review of claims 15–17, 22, 24, 26, and 31–33 of the '150 patent. Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 9, "Prelim. Resp."). Pursuant to 35 U.S.C. § 314(a), we instituted an *inter partes* review of all challenged claims on the following grounds alleged in the Petition.

| References | Basis | Claims Challenged |
|---|---|---|
| Ludwig[1] and Amidi[2] | § 103 | 15–17, 22, 24, 26, and 31–33 |
| Amidi | § 102(e) | 22, 24, and 26 |

Paper 12 ("Dec. to Inst."), 29.

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 26, "PO Resp."), to which Petitioner filed a Reply (Paper 28, "Reply"). An oral argument was held on July 28, 2015, consolidated with

[1] US Patent No. 5,581,498, iss. Dec. 3, 1996 (filed Oct. 20, 1994) ("Ludwig," Ex. 1011).

[2] US Patent Publication No. 2006/0117152 A1, pub. June 1, 2006 (filed Jan. 5, 2004) ("Amidi," Ex. 1008).

the oral hearings for IPR 2014-00882 and IPR2014-00883. *See* Paper 31. A transcript ("Tr.") of the oral argument is included in the record. Paper 32.

*B. Related Proceedings*

The parties informs us that the '150 patent is involved in the following federal district court cases: *Diablo Technologies, Inc. v. Netlist, Inc.*, Case No. 4:13-CV-03901-YGR (N.D. Cal.); and *Netlist, Inc. v. Smart Modular Technologies,* Case No. 4:13-CV- 05889-YGR (N.D. Cal.). Papers 10, 1; 33, 2. In addition, Petitioner filed two other petitions requesting *inter partes* review of the '150 patent. Paper 10, 2. These cases are: IPR 2014-00882 and IPR2014-00883. *Id.* We consolidated the oral hearings for IPR2014-00882, IPR2014-00883, and IPR 2014-01011. *See* Paper 31.

Petitioner further informs us that related US Patent Nos. 7,619,912 and 7,636,274 are the subjects of *inter partes* reexaminations (95/000,578 and 95/001,337). Pet. 10–11. Petitioner also informs us that related US Patent No. 7,289,386 is the subject of district court case *Google, Inc. v. Netlist, Inc*., Case No. C 08-4144-SBA (N.D. Cal.). *Id*. at 14–15.

*C. The '150 Patent*

The '150 patent relates to a memory module of a computer system with improved performance and memory capacity. Ex. 1001, 1:30–34. Memory module 10 includes a plurality of memory devices 30 (arranged in ranks 32) and circuit 40. *Id.* at 4:56–65; Fig. 1. Circuit 40 is electrically coupled to the memory devices 30 and memory controller 20 of a computer system. *Id.* The memory module improves performance and memory capacity by isolating electrical loads of the memory devices from the computer system. *Id.* at 4:65–66.

Circuit 40 receives input signals from memory controller 20. *Id.* Figure 1, reproduced below, illustrates input signals (corresponding to a number of memory devices) from memory controller 20, such as chip select signals ("cs#"), that are directed to memory module 10, which can act as a virtual memory module. *Id*. at 16:47–57; Figs. 1, 9A, 9B.

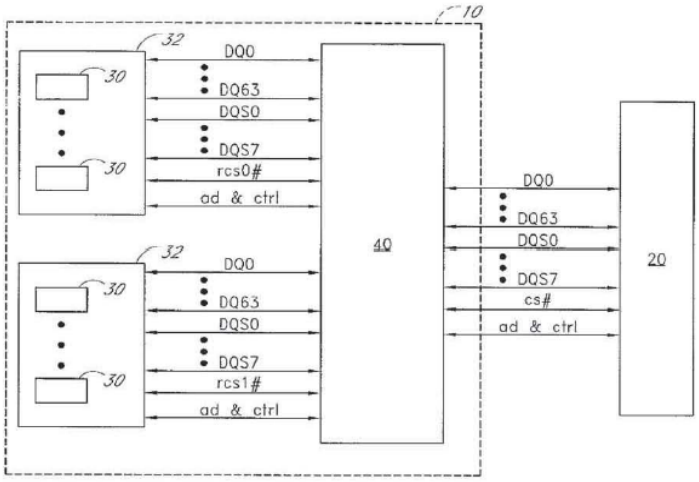


Figure 1 is a schematic of a memory module with circuit 40 and memory devices 30 and connectable to memory controller 20.

As shown in Figure 1 above, based on the received input signals from memory controller 20, circuit 40 generates output signals corresponding to memory devices 30 on the memory module. *Id*. at Fig. 1. The output signals include a different number of chip select signals (e.g., "rcs0#" and "rcs1#") corresponding to memory devices 30 shown in ranks 32. *Id*. at 16:66–17:4; Fig. 1.

Circuit 40 includes a logic element, such as a programmable logic device (PLD), an application-specific integrated circuit (ASIC), a field programmable gate array (FPGA), or a complex programmable-logic device (CPLD). Ex. 1001, 6:4–18. As shown in Figure 9A, reproduced below, circuit 40 may also include register 230 and phase-lock loop device (PLL) 220. *Id.* at 15:35–41; Fig. 9A.

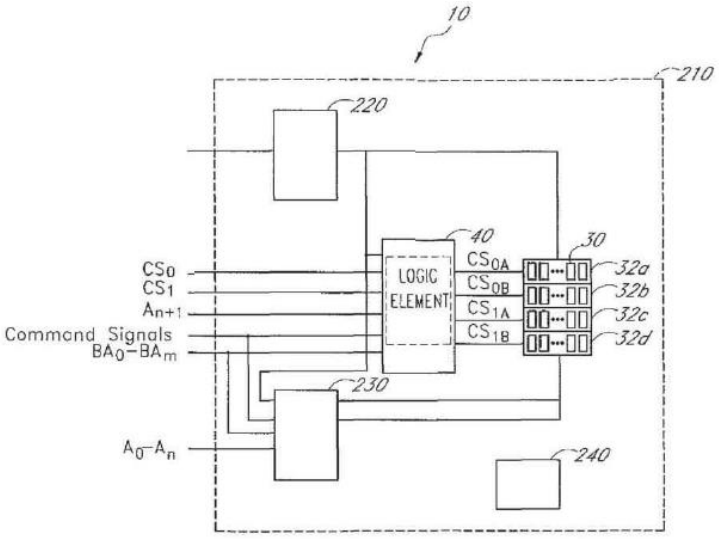


Figure 9A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system.

Figure 9A above illustrates circuit 40 receiving a set of input command signals, address signals ($A_{n+1}$), including bank address signals ($BA_0$-$BA_m$), row address signals ($A_0$-$A_n$), column address signals, gated column address strobe signals, and chip-select signals ($CS_0$, $CS_1$), from memory controller 20 of the computer system. *Id.* at 16:24–29, 17:11–26. "In response to the set of input address and command signals, circuit 40 generates a set of output address and command signals." *Id.* at 16:31–33.

With the output address and command signals, circuit 40 isolates the electrical loads of some memory devices 30 from the computer system. *Id.* at 6:48–62. According to the '150 patent, load isolation may result in specific benefits including reduced load related to data signal lines. *Id*. at 14:34–40. In order to isolate the loads, the logic element of circuit 40 translates between a system memory domain of the computer system and a physical memory domain of memory module 10. *Id*. at 6:48–62. As shown in Figure 3, reproduced below, the circuit isolates the load of a memory

device by isolating one or both of DQ data signal lines 102a, 102b of two memory devices 30a and 30b from common DQ data signal line 112 that is coupled to the computer system. *Id.* at 6:63–7:2, Fig. 3A.

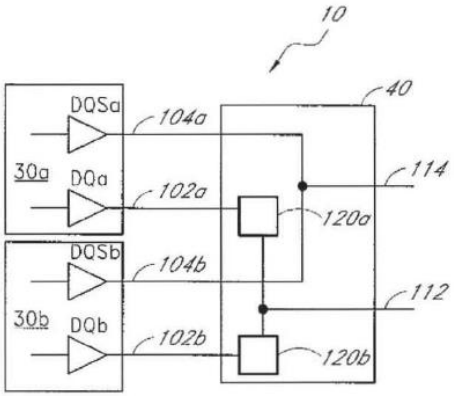


Figure 3A is a schematic of circuit 40 receiving a set of input command signals from memory controller 20 of the computer system.

Circuit 40, shown in Figure 3A above, can electrically couple one or both of DQ data signal lines 102a, 102b of memory devices 30a and 30b to common data signal line 112, at the same time. *Id.* at 7:22–26; Fig. 3A. Circuit 40 also allows a DQ data signal to be transmitted from memory controller 20 of the computer system to one or both of DQ data signal lines 102a, 102b. *Id.* at 7:2–5. The logic element of circuit 40 uses switches 120a, 120b in order to isolate or couple one or both of DQ data signal lines 102a, 102b of memory devices 30a and 30b from common data signal line 112. *Id.* at 7:2–12.

*D. Illustrative Claim*

As noted above, *inter partes* review was instituted for claims 15–17, 22, 24, 26, and 31–33 of the ’150 patent, of which claims 15, 22, and 31 are independent claims. Claim 15 is illustrative of the challenged claims and is reproduced below:

> 15. A circuit configured to be mounted on a memory module so as to be electrically coupled to a first double-data-rate (DDR) memory device having a first data signal line and a first data strobe line, to a second DDR memory device having a second data signal line and a second data strobe line, and to a common data signal line, the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals comprising row address signals, column address signals, bank address signals, and chip-select signals, the set of input signals compatible with a system memory domain of the computer system, the circuit comprising:
>
> a logic element;
>
> a register;
>
> a phase-lock loop device configured to be operationally coupled to the first DDR memory device, the second DDR memory device, the logic element, and the register,
>
> wherein the circuit is configurable to be responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the circuit configurable to translate between the system memory domain of the computer system and a physical memory domain of the memory module, wherein the system memory domain has a first memory density per memory device, and the physical memory domain has a second memory density per memory device less than the first memory density per memory device.

Ex. 1001, 42:41–43:2.

## II. DISCUSSION

### *A. Claim Construction*

In an *inter partes* review, claim terms in an unexpired patent are interpreted according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see also In re Cuozzo Speed Techs., LLC*, 793 F.3d 1268, 1278–79 ("Congress implicitly approved the broadest reasonable interpretation standard in

enacting the AIA," and "the standard was properly adopted by PTO regulation."). Under this standard, claim terms generally are given their ordinary and customary meaning, as understood by one of ordinary skill in the art in the context of the patent's entire written disclosure. *In re Translogic Tech., Inc*., 504 F.3d 1249, 1257 (Fed. Cir. 2007). Yet a "claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history." *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002).

In the Decision to Institute, we construed the terms "Memory Module," "Circuit Configured to be Mounted on a Memory Module," and "Selectively Electrically Coupling," which are recited in all the challenged independent claims. *See* Dec. to Inst. 8–12. During the course of the trial, Patent Owner argued for altered constructions of these claim terms. PO Resp. 4–15. Therefore, we address these contentions and construe each claim term as discussed below.

*1. "Memory Module"*

In the Decision to Institute, we construed the term "memory module," as "a plurality of memory devices and a circuit" thereby encompassing "additional circuitry and multiple printed circuit boards." Dec. to Inst. 8–9.

Petitioner agrees with the construction set forth in the Decision to Institute. Reply 2; Tr. 5:25–6:10. Patent Owner, however, contends that "memory module" should be construed as "a packaging arrangement of one or more memory device(s) for use in a computer socket." PO Resp. 4; Tr. 47:5–7. According to Patent Owner, the construction of "memory module" in the Decision to Institute is unreasonably broad, because it is inconsistent

with the ordinary and customary meaning of the term as it would be understood by a person of ordinary skill in the art. PO Resp. 4–10. Patent Owner argues the Board erred in construing the term by analyzing each component of the word separately (*id.* at 5) and relying on the '150 patent specification (Tr. 47:17–20), whereas a person of ordinary skill in the art would have understood "memory module" to be a term of art (PO Resp. 5–6; Ex. 2002 ¶ 52 (Declaration of Dr. Carl Sechen)). Patent Owner explains that under the Board's construction of "memory module," the term would encompass a memory controller and associated memory devices. PO Resp. 9–10.

Patent Owner further contends that the Board's construction of "memory module" is inconsistent with the '150 patent disclosure. *Id.* at 10. Patent Owner notes that claims 15, 22, and 31 recite "the memory module configured to be electrically coupled to a memory controller of a computer system so as to receive a set of input signals." *Id.* (emphasis omitted). According to Patent Owner, due to the use of different terms in the '150 patent, "memory module" would not be read as including the '150 patent's "memory controller" by a person of ordinary skill in the art. *Id.*; Ex. 2002 ¶ 57.

We are charged with interpreting claim terms according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Additionally, when construing claim terms, we "should also consult the patent's prosecution history in proceedings in which the patent has been brought back to the [U.S. Patent and Trademark Office] for a second review." *Microsoft Corp. v. Proxyconn, Inc.*, 789 F.3d 1292, 1298 (Fed. Cir. 2015). Yet, we must be careful not to

improperly import limitations into the claims or to read a particular embodiment appearing in the written description into the claim, if the claim language is broader than the embodiment. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

The specification of the '150 patent does not define explicitly the term "memory module." The specification does, however, teach embodiments that describe a memory module as comprising a plurality of memory devices on a carrier and a circuit. Ex. 1001, 2:63–64; 3:7–9; 4:59–63. In another embodiment, a memory module comprises (i) a printed circuit board on which memory devices are mounted, (ii) a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and (iii) a plurality of electrical conduits which electrically couple the memory devices to the circuit and which electrically couple the circuit to the edge connectors. *Id*. at 5:24–32. The '150 patent also teaches that memory modules in the disclosed embodiments are compatible with at least single in-line memory modules (SIMMS) and dual in-line memory modules (DIMMS). *Id*. at 5:32–39.

Although the embodiments disclosed in the '150 patent are instructive, the claims recite language broader than that found in the embodiments. *See In re Van Geuns*, 988 F.2d at 1184. Therefore, we decline to adopt Patent Owner's claim construction as it would import limitations improperly from the specification into the claims and unnecessarily limit the scope of the claims. We credit, however, the testimony of Patent Owner's Declarant, Carl Sechen, Ph.D. ("Dr. Sechen"), who explains the state of the art and the customary meaning of "memory module" as it would be understood by one of ordinary skill in the art to

encompass at least a "removable circuit board, cartridge, or other carrier that contains one or more RAM memory chips." *See* Ex. 2002 ¶¶ 39–57. Therefore, we modify the construction of "memory module" from that set forth in the Decision to Institute, wherein we construed the term as "a plurality of memory devices and a circuit" that "encompass[es] additional circuitry and multiple printed circuit boards." Dec. to Inst. 9. Rather, we construe the term "memory module" as "one or more memory devices on a carrier," because such a construction is consistent with the disclosure of the '150 patent and with the ordinary and customary meaning of "memory module."

*2. "Selectively Electrically Coupling" and "Selectively Electrically Isolating"*

In the Decision to Institute, we construed the term "selectively electrically coupling," as "making a selection between at least two components so as to transfer power or signal information from one component to at least one other component." Dec. to Inst. 9–11.

Petitioner agrees with the construction set forth in the Decision to Institute. Reply 2; Tr. 5:25–6:10. Patent Owner, however, contends that "selectively electrically coupling" should be construed as "electrically coupling in response to a selection." PO Resp. 12–15; Tr. 70:4–9. According to Patent Owner, the Board's construction is unreasonably broad, whereas its proffered construction is more consistent with the disclosure of the '150 patent. PO Resp. 13–14 (citing Ex. 1001, 5:29–30, 7:22; Ex. 2002 ¶ 66), 26–28. Patent Owner specifically argues that "electrically coupling" in the '150 Patent is provided by a structural pathway for electricity, and this is also consistent with the meaning of "electrically coupling" as a term of art. *Id.* at 14 (citing Ex. 2002 ¶ 66). Patent Owner further argues that a

person of ordinary skill in the art would understand the act of electrically coupling to take place between strictly two components, between which a structural pathway for electricity would be formed. *Id.*

We are unpersuaded by Patent Owner's position. The specification of the '150 patent does not define explicitly the term "selectively electrically coupling." Therefore, we refer to its ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d at 1257. A technical dictionary, IEEE Dictionary[3], defines "electrical coupling" as "[e]lectrical charges in conductors of a disturbed circuit formed by electrical induction." Ex. 3001. The IEEE Dictionary explains that "[s]ince the ratio of a conductor's electrostatic charge to the potential difference between conductors (required to maintain that charge) is the general definition of capacitance, electrical coupling is also called capacitive coupling." *Id.* The IEEE Dictionary defines "coupling capacitance (1) (ground systems)" ("capacitive coupling") as "[t]he association of two or more circuits with one another by means of capacitance mutual to the circuits." Ex. 3002. We understand this to mean that the two or more circuits are associated in such a way that power or signal information may be transferred from one circuit to another. The Oxford English Dictionary defines "selectively" as "[i]n a selective manner; by selection." Ex. 3003. The Oxford English Dictionary also defines "select" as "[t]o choose or pick out in preference to another or others." Ex. 3004.

[3] IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, Standards Information Network, IEEE Press (2000).

Accordingly, we modify slightly the construction from the Decision to Institute of "selectively electrically coupling," as "making a selection between at least two components so as to transfer power or signal information from one selected component to at least the other selected component," because such a construction is consistent with the ordinary and customary meaning of "selectively electrically coupling."

Based on the same reasoning, we construe "selectively electrically isolating" as "making a selection between at least two components and not transferring power or signal information from one selected component to the other selected component."

*3. "Circuit Configured to be Mounted on a Memory Module"*

In the Decision to Institute, we construed the term "a circuit configured to be mounted on a memory module," to encompass "circuitry configured to be mounted on at least a portion of a memory module." Dec. to Inst. 11–12. We determined such construction is consistent with the ordinary and customary meaning of "a circuit configured to be mounted on a memory module." *Id.* at 12.

Petitioner agrees with the construction set forth in the Decision to Institute. Reply 2; Tr. 5:25–6:10. Patent Owner, however, contends that "a circuit configured to be mounted on a memory module" should be construed as "an entire circuit configured to be mounted on a single memory module." PO Resp. 18–19; Tr. 68:1–18.

Patent Owner notes that our claim construction, as set forth in the Decision to Institute, is ambiguous in that it can be read two ways:

> One might read the Board's construction as meaning that the circuit is mounted on and occupies at least a portion of the memory module (Ex. 2002, ¶ 62), which may be consistent with

> Netlist's construction. On the other hand, one might read the Board's construction as encompassing portions of the circuit to be mounted off-module, which would be unreasonably broad to a [person of ordinary skill in the art].

*Id*. at 11 (citing Ex. 2002 ¶ 62). According to Patent Owner, "memory module" is a term of art that would have had a well-understood meaning to a person of ordinary skill in the art at the time of the invention and a person of ordinary skill in the art would not have understood "a circuit configured to be mounted on a memory module" to include circuit parts off of that memory module or on a different memory module. *Id.* at 12 (citing Ex. 2002 ¶ 60). Patent Owner contends that such a construction could include situations that defeat the purpose of a memory module to make removing and installing memory upgrades easy and error-free. *Id*. (citing Ex. 2002 ¶ 61).

We decline to adopt Patent Owner's claim construction as it is inconsistent with the definition of "circuit" as found in the specification of the '150 patent. The '150 patent defines "circuit" as "a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions." Ex. 1001, 5:9–13. The '150 patent does not limit a "circuit" to only a configuration of electrical components or devices that are mounted on a single memory module. Therefore, applying the broadest reasonable interpretation consistent with the specification of the '150 patent, we construe the claim element "a circuit configured to be mounted on a memory module," as we did in the Decision to Institute, but we further

clarify the construction to encompass "a portion of circuitry configured to be mounted on at least a portion of a memory module."

*4. Other Claim Terms*

We determine that no express constructions of any other claims terms are required for our analysis, and we apply the ordinary and customary meaning of each claim term.

*B. Principles of Law*

To prevail in its challenges to the patentability of the claims, a petitioner must establish facts supporting its challenges by a preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A claim is unpatentable under 35 U.S.C. § 102 if a prior art reference discloses every limitation of the claimed invention, either explicitly or inherently. *Glaxo Inc. v. Novopharm Ltd.*, 52 F.3d 1043, 1047 (Fed. Cir.1995). Furthermore, the prior art reference—in order to be anticipatory—must disclose every limitation of the claimed invention arranged or combined in the same way, as in the claim. *Net MoneyIN, Inc. v. VeriSign, Inc*., 545 F.3d 1359, 1371–72 (Fed. Cir. 2008). A reference can anticipate a claim, however, even if it "'d[oes] not expressly spell out' all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would 'at once envisage' the claimed arrangement or combination." *Kennametal, Inc. v. Ingersoll Cutting Tool Co*., 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering,* 49 CCPA 993, 301 F.2d 676, 681 (1962)). Additionally, "the reference need not satisfy an *ipsissimis verbis* test." *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (internal citation omitted).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

We analyze the instituted ground of unpatentability in accordance with the above-stated principles.

*C. Level of Ordinary Skill in the Art*

In determining whether an invention would have been obvious at the time it was made, we determine the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere*, 383 U.S. at 17. "The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry." *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991).

Petitioner's Declarant, Srinivasan Jagannathan, Ph.D. ("Dr. Jagannathan"), testifies that a person of ordinary skill in the art at the time of the '150 patent:

> would understand basic memory and data communication concepts, with a bachelor's degree in any of electrical engineering, computer engineering, computer science, or related field. Course work for one of ordinary skill in the art

> would have included a course on computer organization, principles of digital design, or computer architecture. One of ordinary skill in the art would also have around one year of experience related to computer memory systems. For example, such experience may include experience in DRAM memory technology and related industry standards such as JEDEC standards for DRAM memories and memory modules.

Ex. 1007 ¶ 53. Patent Owner' Declarant, Dr. Sechen, testifies that one of ordinary skill in the art at the time of the '150 patent would have had an undergraduate degree in electrical engineering or computer engineering, at least two years of professional experience in the design of memory systems, familiarity with the latest JEDEC standard specifications for memory devices and modules, and familiarity with the latest DRAM memory devices widely available in the market. Ex. 2002 ¶ 14. Dr. Sechen further testifies that a person of ordinary skill in the art would have design proficiency in memory modules comprising double-data rate (DDR) memory technology, such as memory modules with JEDEC standard DDR SDRAM devices. *Id.* ¶ 15.

Based on our review of the '150 patent and the types of problems and solutions described in the '150 patent and cited prior art, we conclude a person of ordinary skill in the art at the time of the '150 patent would have a Bachelor's degree in electrical engineering, computer engineering, computer science, or related field, and at least one year of work experience, including familiarity with computer memory systems and related industry standards such as JEDEC standards for DRAM memories and memory modules. We further note that the applied prior art reflects the appropriate level of skill at

the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

*D. Expert Testimony*

Patent Owner argues that Petitioner's Declarant, Dr. Jagannathan, does not qualify as a person of ordinary skill in the art at the time of the invention because of his alleged lack of experience designing memory modules. PO. Resp. 16–17. According to Patent Owner, Dr. Jagannathan's experience and background is directed to software and is not relevant to the case. *Id.* at 18–23. Patent Owner argues that, unlike Dr. Jagannathan, its Declarant Dr. Sechen has significant practical experience designing memory modules. *Id.* at 18; Ex. 2001 ¶¶ 3, 4, Exhibit A.

As to his hardware and memory design experience, Dr. Jagannathan was awarded a Doctorate degree in Computer Science, and has "two decades of experience in the design, development, and analysis of a wide range of hardware, software, network and database systems." Ex. 1007 ¶ 2. He has designed and implemented hardware virtual memory caches, and researched theoretical performance measures of various cache coherency protocols. *Id.* Dr. Jagannathan also stated during his deposition that he has experience in the design of memory systems. Ex. 2003, 124:12–126:1. Patent Owner contends, however, that Dr. Jagannathan fails to qualify as a person of ordinary skill in the art because he lacks sufficient professional experience physically designing (i.e., "actually putting down a design and saying this is what it would be") a memory module. PO Resp. 21 (citing Ex. 2003, 125:14–17). We disagree.

To testify as an expert under FRE 702, a person need not be a person of ordinary skill in the art, but rather must be "qualified in the pertinent art."

*Sundance, Inc. v. DeMonte Fabricating Ltd.*, 550 F.3d 1356, 1363–64 (Fed. Cir. 2008); *see SEB S.A. v. Montgomery Ward & Co.*, 594 F.3d 1360, 1372–73 (Fed. Cir. 2010) (upholding a district court's ruling to allow an expert to provide testimony at trial because the expert "had sufficient relevant technical expertise" and the expert's "knowledge, skill, experience, training [and] education . . . [wa]s likely to assist the trier of fact to understand the evidence"); *Mytee Prods., Inc. v. Harris Research, Inc.*, 439 Fed. App'x 882, 886–87 (Fed. Cir. 2011) (non-precedential) (upholding admission of the testimony of an expert who "had experience relevant to the field of the invention," despite admission that he was not a person of ordinary skill in the art). We find that, although Dr. Jagannathan is less experienced than Dr. Sechen in the area of memory module design, he is qualified sufficiently to testify about memory systems and memory modules.

*E. Alleged Obviousness of Claims 15–17, 22, 24, 26, and 31–33 in view of Ludwig and Amidi*

Petitioner alleges claims 15–17, 22, 24, 26, and 31–33 of the '150 patent are unpatentable under 35 U.S.C. § 103 over the combination of Ludwig and Amidi. Pet. 21–40. Patent Owner disputes Petitioner's position, arguing that a person of ordinary skill in the art would not have had reason to combine the references in the manner proposed by Petitioner (PO Resp. 39–44) and further that the combination of the references fails to teach or suggest all of the claim limitations (*id.* at 24–26, 32–39).

We have reviewed the Petition, the Patent Owner Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers. For reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 15–17, 22, 24, 26, and 31–33 of

the ’150 patent would have been obvious to a person of ordinary skill in the art at the time of the invention in view of the combination of Ludwig and Amidi.

*1. Overview of Ludwig*

Ludwig discloses the use of integrated circuit (IC) chips stacked together, and which act as a single memory chip (VIC). Ex. 1011, 1:9–12; 1:43–48. Ludwig further discloses that the stacked chips have four memory layers, with each layer including four DRAM memory chips that receive and transmit data using data lines DQ1-DQ4. *Id.* at 9:31–39. One embodiment of the stacked chips is shown in Figure 3, reproduced below.

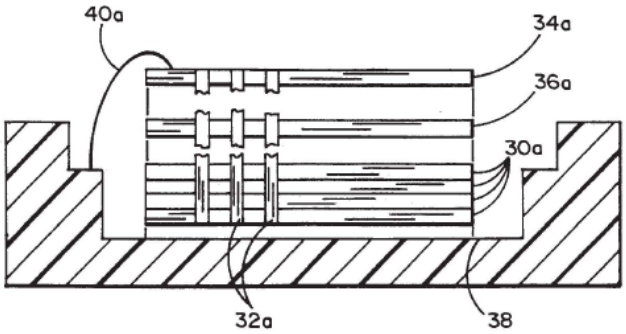


Figure 3 illustrates stacked memory chips 30a with ceramic cap layer 34a and VIC chip 36a located between the four memory chips.

As shown in Figure 3, VIC chip 36a is an interface chip that is electronically interposed between memory chips 30a and the host system and provides appropriate connections between memory chips 30a and the host system. *Id.* at 2:6–7; 4:60–65; 5:9–11; 5:36–43; 5:64–67.

Another embodiment of the stacked chips is shown in Figure 7, reproduced below.

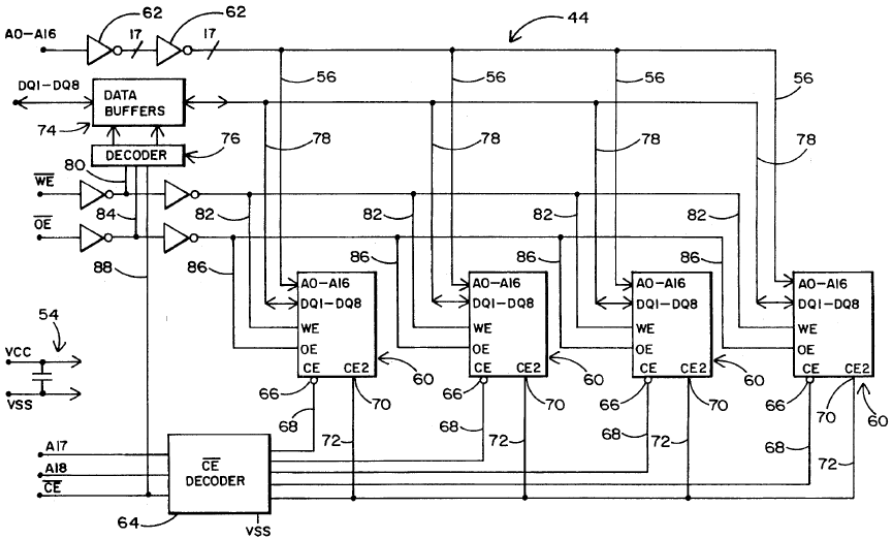


Figure 7 illustrates the circuitry associated with the stacked chips, including the four IC memory chips and VIC chip 44. *Id.* at 5:63–65.

VIC chip 44, shown in Figure 7, provides connections between the host system and stacked memory chips 60 (*id.* at 5:65–67), while the four IC memory chips provide memory capacity (*id.* at 6:11–12). According to Ludwig, "recapitulating the use of the VIC chip to cause the four chip stack to be addressed as if there were a single higher capacity chip, there are address lines (A0-A18) available at the chip stack." *Id.* at 6:28–36. Ludwig discloses that A17 and A18 are decoded in the VIC chip to select one of the four chips in the stack, while the remaining address lines, A0-A16, feed into all four memory chips. *Id.* at 6:31–33. Thus, per this embodiment in Ludwig, A17 and A18 select the stack layer and A0-A16 select the memory location. *Id.* at 6:34–35.

Ludwig further discloses that another portion of the memory interface is focused on data transmission, which can flow in both directions, i.e., from the host "system into the stacked chip package, or out of the package into the host system." *Id.* at 6:40–43. As shown in Figure 7 above, data buffer decoder 76 controls data flow, while the data travels along 8 parallel lines,

DQ1—DQ8. *Id.* at 6:44–51. According to Ludwig, these data lines in the VIC chip are buffered by "tri-state" buffers 74. *Id.*

Another embodiment of the stacked chips is shown in Figure 11, reproduced below.

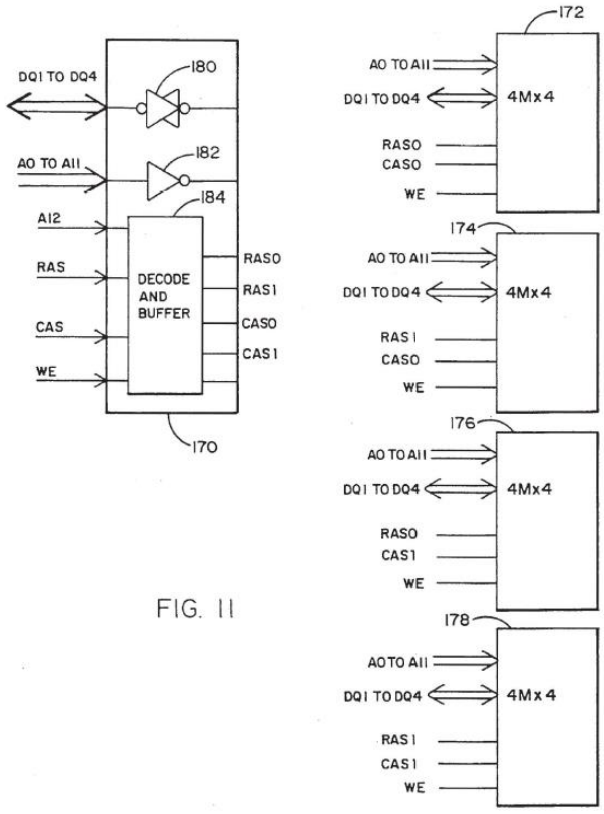


FIG. 11

Figure 11 illustrates a diagram of DRAM memory package organized with a VIC chip and four stack DRAM IC chips.

As illustrated in Figure 11, stacked memory chips 172, 174, 176, 178 are connected to data lines DQ1–DQ4. *Id.* at 9:37–39. VIC chip 170 provides address decoding, so that decoding of data takes place by routing the input of VIC buffers to the appropriate memory chip in the stack. *Id.* at 9:13–23.

*2. Overview of Amidi*

Amidi discloses a memory interface system with a processor, a memory controller, and a memory module. Ex.1008 ¶¶ 2, 3. According to

Amidi, a prior art memory interface system is shown in Figure 1, reproduced below.

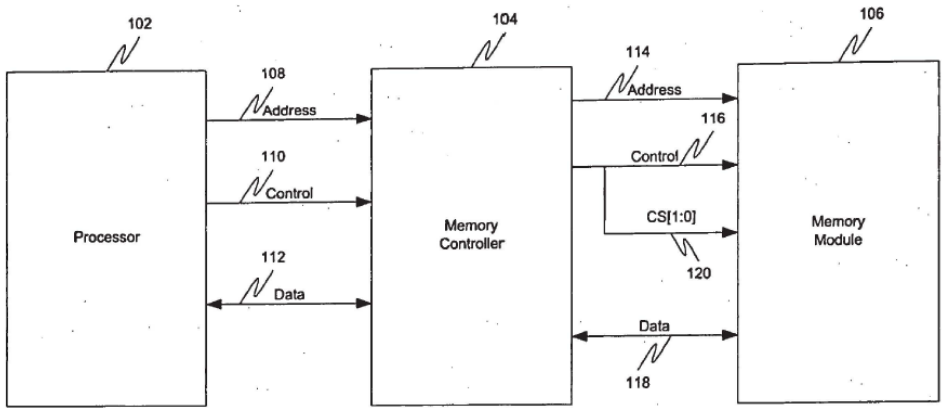


Figure 1 is a schematic of a standard prior art memory interface system.

The prior art system in Figure 1 includes memory module 106 with controller address bus 114, controller control signal bus 116, and controller data bus 118. *Id*. ¶ 2, Fig. 1. As illustrated in Figure 1, memory module 106 communicates with memory controller 104 via busses 114, 116, 118. *Id*. at Fig. 1. Amidi teaches that each stack of DDR memory devices has a data signal line and a data strobe line DQS. *Id*. ¶ 32; Fig. 2. Amidi also teaches that at least two DDR memory devices are connected to a common data memory bus. *Id*. ¶ 34; Fig. 3.

Amidi further discloses multiple memory devices mounted on the front and back side of memory module 400 as shown in Figure 4A reproduced below. *Id*. ¶¶ 34, 37.

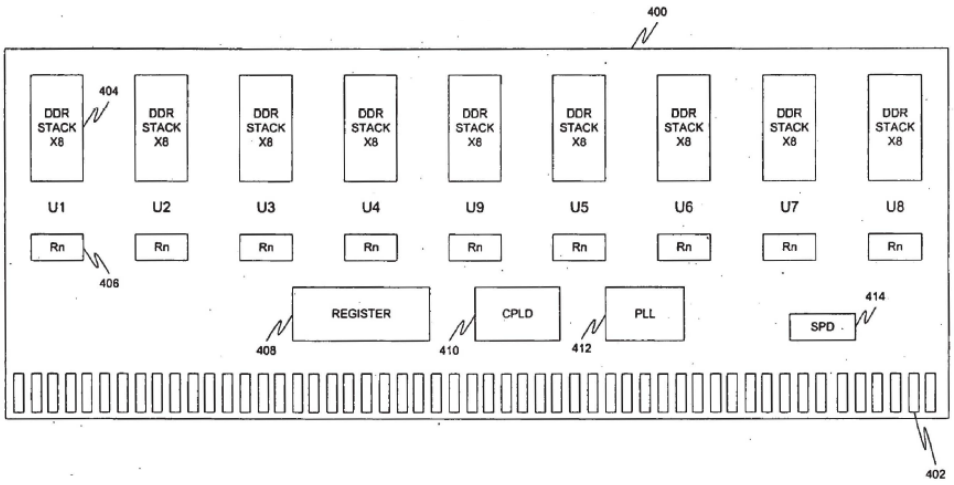


Figure 4A is a schematic of a DDR memory module.

Figure 4A, above, illustrates one embodiment of Amidi where memory module 400 includes memory devices 404, resistor network 406, register 408, complex programmable logic device (CPLD) 410, phase-locked loop (PLL) 412, and SPD 414[4]. *Id.* According to Amidi, memory module 400 receives input signals, including address (Add(n)) signals, row address strobe (RAS) signal, column address strobe (CAS) signal, and bank address (BA[1:0]) signals. Ex. 1008 ¶ 50; Fig. 6A.

Another embodiment of Amidi's memory interface system is shown in Figure 6A, reproduced below.

[4] According to Amidi, SPD 414 is a simple "interface Electrically Erasable Programmable Read-Only Memory (EEPROM) to hold information regarding memory module for BIOS during the power-up sequence." Ex. 1008 ¶ 40.

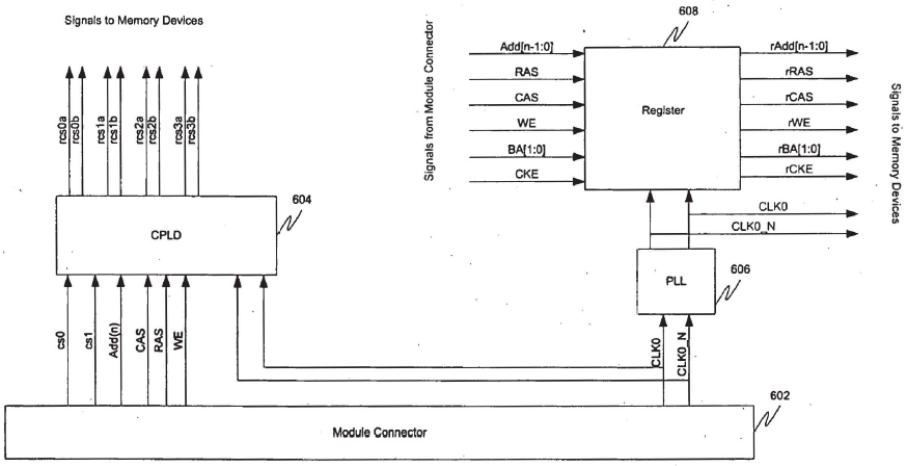


Figure 6A is a schematic of a row address decoding system for a transparent four rank memory module.

As illustrated in Figure 6A above, module connector 602 sends signals to CPLD 604, PLL 606, and register 608. *Id.* CPLD 604 also ensures that all commands for a two rank memory module conveyed by module connector 602 are performed on the four rank memory modules. *Id.* ¶ 52. Amidi explains that the system chip select signals control the ranks of individual memory modules. *Id*. ¶¶ 2, 3.

*3. Analysis*

*a. Ludwig and Amidi Teach or Suggest All the Recited Limitations of Independent Claims 15, 22, and 31*

Petitioner contends the combined disclosures of Ludwig and Amidi, as summarized above, teach or suggest each limitation of independent claims 15, 22, and 31 of the ’150 patent. Pet. 21–40. Petitioner first argues that Ludwig discloses an interface chip that qualifies as a circuit that is mounted on a stacked chip memory module, where the stack is a plurality of DDR memory devices arranged in one or more ranks. Pet. 21–23 (citing Ex. 1011, 2:1–9; 12:29–44). According to Petitioner, the VIC chip (“circuit”) of Ludwig includes logic elements, a register, a PLL, and a memory element in

the form of a memory cache. *Id.* at 21–22 (citing Ex. 1011, 7:1–4; 7:16–19; 7:44–55; Figs. 7, 8); Ex. 1007 ¶¶ 103, 106, 107, 108. Petitioner then explains that Amidi discloses a circuit mounted on a memory module, where the circuit includes a logic element, a register, and a phase-lock loop device. *Id.* at 22 (citing Ex. 1008, ¶¶ 2, 37; Figs. 4A, 6A); Ex. 1007 ¶¶ 58, 64. Petitioner also contends that the system described in Amidi includes a memory module having one or more ranks of DDR memory devices, which are electrically coupled to the components of the circuit (CPLD). *Id.* at 22–23 (citing Ex. 1008, Figs. 4A, 4B, 6A.)

Petitioner then argues that Ludwig discloses memory devices having data signal lines and data strobe lines. Petitioner specifically points out that Ludwig discloses a strobe signal used in the form of combinations of CAS with WE and OE pins. *Id.* at 25 (citing Ex. 1011, 8:44–56; 6:50–52; 7:43–61; Fig. 9). Petitioner notes that Amidi also discloses memory devices having data signal lines and data strobe lines. *Id.* at 27 (citing Ex. 1008 ¶¶ 29, 32; Figs. 2, 3). According to Petitioner, Amidi discloses that each stack of DDR memory devices has a data signal line and a data strobe line DQS. *Id.* at 26 (citing Ex. 1008 ¶ 32; Fig. 3). Amidi also discloses that at least two DDR memory devices are connected to the same (common) memory bus ("common data signal line"). *Id.* (citing Ex. 1008 ¶¶ 34–35; Fig. 3). According to Petitioner, a person of ordinary skill in the art would recognize that each DDR memory device has its own data pins (data bus), that the memory devices are connected to a common data signal line, and that the circuit of Amidi is "electrically coupled" to the common data bus. Pet. 26; *see* Ex. 1007 ¶¶ 63, 72.

Petitioner provides arguments that the sending and receiving of input signals by the systems occurs in Ludwig and Amidi, and explains how each reference teaches a circuit that is responsive to such input signals. Pet. 27–38. Petitioner specifically argues that Ludwig teaches a circuit that is "responsive to the set of input signals by selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line." Petitioner makes this argument because Ludwig discloses decoder 64 is part of the circuit and responds to (i) address lines A17, A18 and chip enable CE as input signals, and (ii) chip select signals CEM 1–4 as output signals to drives buffers 113, 114 to selectively couple data signal line DQ1A–DQ8A of memory chip layer A to common data signal line DQ1–DQ8. *Id.* at 29–30 (citing Ex. 1011, 7:16–48; Fig. 8); Ex. 1007 ¶¶ 105, 112.

Petitioner also argues that Amidi teaches "selectively coupling" because Amidi discloses that CPLD 404, 604 is responsive to a set of input signals (address signal Add(b) and chip select signals cs0, cs1) to determine ("selectively electrically coupling") an active rank of the four ranks and inactivating the other three ranks of memory devices from the computer system. *Id.* at 31–32 (citing Ex. 1008 ¶¶ 43, 44, 62); Ex. 1007 ¶ 66. According to Petitioner, the act in Amidi of activating one rank while deactivating other ranks constitutes "selectively coupling" and "selectively isolating." *Id.* at 31–32.

Similarly, Petitioner cites to Ludwig's disclosure of tri-state buffers in the VIC chip that isolate the loads of memory devices that are not enabled, to support Petitioner's contention that Ludwig "selectively isolates one or

more loads of the DDR memory devices from the computer system." *Id.* at 32.

According to Petitioner, a person of ordinary skill in the art would have been motivated to combine the teachings of Ludwig and Amidi, because (1) both references relate to a memory module including circuitry that is configurable to control one or more sets of memory devices based on signals provided by a connected computer and (2) both references are directed to solving the same problem of using additional memory devices in a memory module to include the overall memory density of the memory module without hindering the ability of the memory module to interface with a pre-existing memory controller. *Id.* at 39–40 (citing Ex. 1011, 2:10–22, 3:65–4:15; Ex. 1008 ¶¶ 38, 39, 43, 44, 62; Ex. 1009 ¶¶ 9,10,28); Ex. 1007 ¶¶ 116–119.

Petitioner supports its position with the Declaration of Dr. Jagannathan, who testifies that a person of ordinary skill in the art would have understood that the teachings of Amidi could have been advantageously applied to Ludwig. Ex. 1007 ¶ 117. In particular, Dr. Jagannathan opines that the teachings of Ludwig and Amidi could have been combined "to have more than one rank of memory devices such as the DDR SDRAM memories of Amidi, that can include more than one bank of memory arrays inside the DRAM device, and receive one of the chip select signals obtained by translating the input chip select and address signals." *Id.* According to Dr. Jagannathan, the benefit of this combination is to apply the teachings of Ludwig to DDR SDRAM memories having faster access times. *Id.* Dr. Jagannathan concludes that one of ordinary skill would have been motivated to combine the architecture in Amidi with the VIC chip of

Ludwig to yield a circuit mounted in a memory module as disclosed by both Amidi and Ludwig. *Id.* ¶ 119.

Patent Owner contests Petitioner's position, arguing that the combination of Ludwig and Amidi fails to teach or suggest a "circuit configured to be mounted on a memory module[,] . . . the circuit . . . selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal to the common data signal line," as recited in the challenged independent claims. PO Resp. 24. Patent Owner specifically argues that the Petition is deficient because the Petition's mapping of "selectively electrically coupling" to buffers 113 and 114 in Ludwig's Fig. 8 was incorrect. *Id.* at 25. According to Patent Owner, by equating the "selectively electrically coupling" to the buffers, Petitioner identified the "selectively electrically coupling" performed in Ludwig as being accomplished via circuitry internal to a memory chip (*i.e.*, via buffers 113 and 114) and not by the identified "circuit" (*i.e.*, VIC chip 90). *Id.* at 26. Patent Owner argues, however, claims 15 and 31 require the "circuit," not the "DDR memory device," to perform the "selectively electrically coupling." *Id.* Patent Owner further argues that the Petition fails to identify a "second data line" in Ludwig as required by the claims. *Id.*

We are unpersuaded by Patent Owner's position, because the arguments presented by Patent Owner generally attack the references individually, rather than in combination. Nonobviousness cannot be established by attacking the references individually when a challenge is predicated upon a combination of prior art disclosures. *See In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). In attacking the references

individually, Patent Owner fails to address Petitioner's actual challenges and establish an insufficiency in the combined teachings of the references. Despite Patent Owner's focus on Ludwig, we note that the Petition challenges the patentability of the claims based on the combination of Ludwig and Amidi. *See* Pet. 21–40. Based on Petitioner's arguments, we are satisfied that Amidi teaches or suggests : (i) a memory module with multiple ranks of DDR SDRAM memory devices 404 (Ex. 1008 ¶¶ 37, 42); (ii) CPLD 604 (*see id.* ¶ 28), register 608, and PLL 606 that can be implemented as a single component (*id.* ¶¶ 37, 50, Figs. 4A, 6A; *see* Ex. 1027, 38:1–39:15, 41:1–6); and (iii) electrically coupling CPLD 604, PLL 606, and register 608 to the ranks of DDR memory devices 404 (*id.* at Figs. 4A, 4B, 6A). We also credit the testimony of Dr. Jagannathan, who explains that "[w]hen Amidi's CPLD provides a chip select signal to a rank of memory devices, it selects the rank and thereby causes it to be coupled to the data bus." Ex. 1028 ¶ 32 (citing Ex. 1008 ¶ 62). Thus, we are persuaded by Petitioner that Ludwig in combination with Amidi discloses or suggests a "circuit configured to be mounted on a memory module[,] . . . the circuit . . . selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal to the common data signal line," as recited in the challenged independent claims.

Petitioner further argues that Petitioner fails to identify a disclosure in Figure 8 of Ludwig of a "second data signal line" required by the challenged independent claims. PO Resp. 26. Patent Owner's position, however, appears to be premised on selected embodiments (specifically Figure 8) from Ludwig, rather than Ludwig's disclosure as a whole. Instead, we are persuaded by Petitioner's contention that certain embodiments from Ludwig

teach read and write lines DQ1–DQ4, which qualify as "first data signal lines" and "second data signal lines." Pet. 24–25 (citing Ex. 1011, 9:31–40; Fig. 11).

Patent Owner also contends that under its proposed construction of "selectively electrically coupling," neither Ludwig nor Amidi meets the claim limitation. PO Resp. 26–28. According to Patent Owner, the teachings of Ludwig are more similar to the generation of a signal, while Amidi is more similar to the transmitting of signals. *Id.* at 27. Patent Owner, then argues that "[t]he '150 Patent discloses that 'electrically couple' is provided by structure (*e.g.*, "a plurality of electrical conduits which electrically couple" (Ex. 1001, 5:29–30), not by Ludwig's signal generation and not by Amidi's signal transmission. PO Resp. 27–28. Patent Owner explains that "[a]n electrical conduit in the '150 Patent is a structural pathway for electricity, but the cited signals from Ludwig and Amidi are flows of electricity" (Ex. 2002 ¶ 79) and "[a] pathway for electricity (as for "selectively electrically coupling" in the '150 Patent) is not a flow of electricity (as for the cited signals from Ludwig and Amidi) (*id*.)." PO Resp. 28.

Patent Owner then argues that the combination of Ludwig and Amidi fails to disclose "selectively electrically coupling" in the context of "signal line" as recited in claims 15 and 31. *Id.* at 28–29. According to Patent Owner, (i) such "signal line" structural elements are wholly missing from the teachings of Ludwig, because "memory layers and memory devices are not 'signal line' structural elements" and (ii) the data lines of Amidi are hard-wired in permanent coupling to the same data bus and are never subject to acts of "selectively electrically coupling." *Id.* at 29–30. Patent Owner,

thus, concludes that "selectively electrically coupling" as in the '150 Patent is distinct from the teachings of Ludwig and Amidi. *Id.* at 31.

As discussed previously, we do not agree with Patent Owner's narrow construction of "selectively electrically coupling." *See supra*, Section II.A.2. Rather, we construe the term as "making a selection between at least two components so as to transfer power or signal information from one selected component to at least the other selected component," because such a construction is consistent with the ordinary and customary meaning of "selectively electrically coupling." *Id.* Given our claim construction, we are unpersuaded by Patent Owner's argument that the flow of electricity on hard-wired, permanent data signal lines does not constitute the electrical coupling of two selected components.

We also credit the testimony of Dr. Jagannathan, who states that Ludwig discloses VIC receiving chip-select signals and address signals as "selectively electrically coupling." Ex. 1007 ¶ 115 (citing Ex. 1011, 7:16–30; Figs. 8, 10). According to Dr. Jagannathan, in response to one chip-select signal and two address signals, the VIC then generates chip-select signals that selectively enable one of four memory layers and selectively isolate the other memory devices in other ranks. We are persuaded that Ludwig's teachings of "selectively enabling" and "selectively isolating" fall within the scope of the term "selectively electrically coupling" as we have construed the term. Furthermore, Amidi's disclosure of directing signals down a specific signal line or data bus in order to determine an active rank within the memory devices falls within the scope of the term "selectively electrically coupling" as we have construed this term.

Patent Owner further contends that Ludwig and Amidi fail to disclose two separate "selectively electrically coupling" actions. PO Resp. 33. Patent Owner notes that claims 15 and 31 recite "the circuit . . . selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line." *Id.* Patent Owner, thus, argues that the claims require that "the circuit" perform two separate acts of "selectively electrically coupling": 1) a first act of "selectively electrically coupling" the first data signal line to the common signal line; and 2) a second act of "selectively electrically coupling" the second data signal line to the common signal line. *Id.* According to Patent Owner, Ludwig's tri-state buffers 180 cannot "selectively electrically couple" a first data signal line to a common data signal line, and separately "selectively electrically couple" a second data signal line to the common data signal line because any selective electrical coupling that tristate buffers 180 may perform is performed collectively on both the first data signal line and the second data signal line. *Id*. at 38 (citing Ex. 2002 ¶ 82). As such, Patent Owner argues that the tri-state buffers 180 (and thus VIC chip 170) in Ludwig cannot perform two separate acts of "selectively electrically coupling" to couple a first data signal line and a second data signal line to a common data signal line, as required in challenged claims 15 and 31. *Id.* Patent Owner further argues that Amidi fails to make up for the deficiency of Ludwig, because Amidi simply discloses various signals and determining an active rank, and signals are not lines. *Id*. at 39.

We do not agree. To the contrary, we find that Ludwig teaches separate coupling actions. Specifically, Ludwig Figure 8 discloses that each

data signal line DQ1A-D has a respective data buffer to couple a corresponding memory chip from Layers A-D to common data bus DQ1, and each data buffer has a control logic that determines which of the four chips within the stack (Layers A-D) to couple. *See* Ex. 1011, 7:33–43, 7:56–65, Fig. 8. We further credit the testimony of Dr. Jagannathan, who states

> Ludwig does disclose multiple acts of coupling. This is because Ludwig discloses selecting the active chip thereby causing selectively electrically coupling the data signal line of the active chip to the common data signal line. A [person of ordinary skill in the art] would understand that when a different active chip is selected, a different act of selectively electrically coupling is performed.

Ex. 1028 ¶ 55.

Finally, Patent Owner contends that Ludwig and Amidi are improperly combined by Petitioner. PO Resp. 39. Patent Owner explains that the Petitioner's combination is based on unsupported speculation and would result in a malfunctioning and inoperable system requiring heady redesign beyond the skill of a person of ordinary skill in the art. *Id.* at 42–43. Specifically, Patent Owner argues that Ludwig's older VIC interface chip signals are fundamentally different from the advanced DDR SDRAM technology disclosed in Amidi, and therefore, would not have been compatible or interchangeable. *Id.* at 40–43. According to Patent Owner, Amidi' DDR SDRAM technology is not backward compatible with the asynchronous DRAM technology of Ludwig, thus, the two technologies would be an inoperable combination. *Id.* at 39–40. Patent Owner specifically argues that in order to communicate properly with Amidi's DDR SDRAM devices, Ludwig's VIC chip would need to be modified to input

and output DDR command-based signals, requiring a redesign of the "fundamental operating principles of Ludwig's VIC chip." *Id.* at 42–43. According to Patent Owner, such a redesign would "undesirably gut the original design of Ludwig's VIC chip." *Id.* at 43.

Patent Owner relies on the Declaration of Dr. Sechen to support its position. Dr. Sechen testified that

> A [person of ordinary skill in the art] would understand that such a redesign of Ludwig's VIC chip and its components would change their fundamental operating principle from asynchronous to synchronous operation. Such a fundamental change would require a significant amount of complexity and design work to achieve a successful transformation in the fundamental aspect of timing. For example, where Ludwig's VIC chip relies on its input and output signals to convey timing information by their own asynchronous waveforms, such timing information has to be conveyed through an entirely different mechanism in a synchronous environment where DDR commands are not designed to convey such timing information. A [person of ordinary skill in the art] might imagine that such a mechanism could be embodied into more logic, but it would not be readily apparent from Ludwig or Amidi how to implement such additional logic, thus requiring undue experimentation.

Ex. 2002 ¶ 93.

Despite Dr. Sechen's explanation of asynchronous and synchronous memory (*see id.* ¶¶ 87–92), we do not agree that the teachings of Ludwig are incompatible with the synchronous memory of Amidi, because Ludwig expressly suggests apply its VIC chip to synchronized memory. *See* Ex. 1001, 10:10–13 ("A valuable added function might be synchronized memory signals to enhance the speed of the memory."). We also credit the testimony of Dr. Jagannathan, who states

> "[t]here was sufficient motivation for one of ordinary skill to apply the circuit including a CPLD, a PLL, and a register in Amidi to the interface chip in Ludwig. One of ordinary skill would recognize the benefits of doing so as taught in Ludwig. For example, Ludwig teaches 'a valuable added function [of the VIC chip] might be synchronized memory signals to enhance the speed of the memory function.'"

Ex. 1007 ¶ 118 (citing Ex. 1011, 10:11–13). Therefore, we are persuaded that the teachings of Ludwig and Amidi are combinable.

Based on the evidence of record, we agree with Petitioner's position that challenged independent claims 15, 22, and 31 would have been obvious over Ludwig and Amidi. Specifically, we are persuaded by Petitioner's reasoning and the evidentiary record that Amidi teaches a circuit mounted on a memory module that is electrically coupled to a first DDR memory device and a second DDR memory device. We are further persuaded that Amidi teaches a circuit with a logic element, a register, and a PLL. We also are persuaded that the teachings of Amidi could have been implemented using the common data signal line and tri-state buffer system disclosed in Ludwig so that by (i) selectively electrically coupling a first data signal line to the common data signal line and (ii) selectively electrically coupling a second data signal line to the common data signal line, the circuit is responsive to a set of input signals. Additionally, we credit the testimony of Dr. Jagannathan that a person of ordinary skill in the art would have had reason to combine the teachings of Ludwig and Amidi, which both relate to memory modules, and are directed to solving the same problem of using additional memory devices in a memory module to increase the overall memory density of the module without hindering the ability of the module to interface with a pre-existing memory controller. *See id.* ¶ 116.

Additionally, we note that the testimony of Patent Owner's Declarant, Dr. Sechen, is based on the claim constructions proffered by Patent Owner and not on the constructions set forth in the Decision to Institute. *Compare* Ex. 2002 ¶¶ 38–72, *with* Dec. to Inst. 7–12. We have considered as relevant, however, the portions of his analysis regarding the prior art and alleged non-obviousness of the claims and accorded the appropriate weight to that particular testimony.

Accordingly, we hold that Petitioner has shown by a preponderance of the evidence that claims 15, 22, and 31 of the '150 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Ludwig and Amidi.

*b. Ludwig and Amidi Teach or Suggest All the Recited Limitations of Dependent Claims 16, 17, 24, 26, 32, and 33*

Claims 16, 24, and 32 recite "wherein the two or more of the logic element, the register, and the phase-lock loop device are portions of a single component." Ex. 1001, 43:3–5, 44:1–3, 44:58–60. Petitioner contends the combined disclosures of Ludwig and Amidi, as summarized above, teach or suggest each limitation of dependent claims 16, 17, 24, 26, 32, and 33 of the '150 patent. Pet. 38–40. Petitioner contends that Ludwig discloses that the VIC chip has functions for buffering, decoding ('logic element'), refreshment for memory retention ('register'), and synchronized memory signals ('PLL'). *Id.* at 38 (citing Ex. 1004, 10:4–13). Petitioner further contends that Amidi discloses that the CPLD ("logic element"), register, and PLL are all mounted on a memory module. *Id.* (citing Ex. 1008 ¶¶ 37, 39, 40, Figs. 4A, 4B, 6). According to Petitioner, a person of ordinary skill in

the art would have recognized that at least the register and PLL could be portions of a single component. *Id.* (citing Ex. 1007 ¶¶ 58, 108).

Dependent claim 17 recites that the circuit includes "one or more switches selectively electrically coupling the first data signal line to the common data signal line and selectively electrically coupling the second data signal line to the common data signal line, the one or more switches operatively coupled to the logic element to receive control signals from the logic element." Dependent claim 33 recites a similar limitation. Ex. 1001, 43:6–12. Petitioner contends Ludwig meet the limitations of claims 17 and 33, because a person of ordinary skill in the art would have recognized the tri-state buffers in Ludwig are "operatively coupled" to the logic element to receive control signals from the logic element. Pet. 39 (citing Ex. 1011, 7:33–45, 9:37–39, Figs. 7, 8, 11; Ex. 1007 ¶¶ 105, 112).

Dependent claim 26 further recites that the claimed circuit is "configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system." Ex. 1001, 44:8–11. Petitioner contends Ludwig discloses that decoder 64 ("circuit") enables one of four memory chips 60 and disenables ("selectively isolate[s]") the other three memory chips ("a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system"). Pet. 39 (citing Ex. 1011, 6:15–20). Petitioner further contends that Amidi teaches that the PLL and register isolate the loads of the memory devices that are not enabled by the chip select signal generated by the CPLD. *Id.* at 39–40 (citing Ex. 1008 ¶¶ 38–39, 43, 62, Figs. 4A and 5). According to Petitioner, a person of ordinary skill in the art would have recognized that selectively isolating the loads of the memory devices would

require isolating the data signal lines of the memory devices from the computer system. *Id.* at 40 (citing Ex. 1007 ¶¶ 72, 105).

Patent Owner does not provide separate contentions regarding the limitations recited in the dependent claims, but relies on the arguments made in support of patentability of independent claims 15, 22, and 31. *See generally* PO Resp.

After consideration of the language recited in claims 16, 17, 24, 26, 32, and 33 of the '150 patent, the Petition, the Patent Owner Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers, we find that one of ordinary skill in the art would have considered these dependent claims obvious over the combination of Ludwig and Amidi. Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that claims 16, 17, 24, 26, 32, and 33 of the '150 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combination of Ludwig and Amidi.

*F. Asserted Anticipation of Claims 22, 24, and 26 in view of Amidi*

Petitioner alleges claims 22, 24, and 26 of the '150 patent are unpatentable under 35 U.S.C. § 102(e) in view of Amidi. Pet. 40. Patent Owner disputes Petitioner's position, arguing that Amidi fails to disclose all of the claim limitations. PO Resp. 24–26, 32–39.

We have reviewed the Petition, the Patent Owner Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers. For reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that claims 22, 24, and 26 of the '150 patent are anticipated by Amidi.

*1. Overview of Amidi*

*See* Section II.D.2., discussed above.

*2. Analysis*

Petitioner contends Amidi, as summarized above, discloses each limitation of claims 22, 24, and 26 of the '150 patent. Pet. 40 (citing *id*. at 21–40). Petitioner first argues that Amidi discloses a circuit mounted on a memory module, where the circuit includes a logic element, a register, and a phase-lock loop device. *Id.* at 22 (citing Ex. 1008 ¶¶ 2, 37, Figs. 4A, 6A); Ex. 1007 ¶¶ 58, 64. Petitioner also argues that the system described in Amidi includes a memory module having one or more ranks of DDR memory devices, which are electrically coupled to the components of a circuit. *Id.* at 22–23 (citing Ex. 1008, Figs. 4A, 4B, 6A.) Petitioner supports its position with the declaration of Dr. Jagannathan, who testifies that Amidi teaches a circuit that includes a CPLD, a register, and a PLL circuit. Ex. 1007 ¶ 58. Dr. Jagannathan further testifies that "[o]ne of ordinary skill would understand that these electrical components or devices are electrically coupled together to form a 'circuit.'" *Id.* (citing Ex. 1008 ¶¶ 34–39, 41).

Petitioner then argues that Amidi also discloses memory devices having data signal lines and data strobe lines. *Id.* at 27 (citing Ex. 1008 ¶¶ 29, 32, Figs. 2, 3). According to Petitioner, Amidi discloses that each stack of DDR memory devices has a data signal line and a data strobe line DQS. (*id.* at 26 (citing Ex. 1008 ¶ 32, Fig. 3)), and that at least two DDR memory devices are connected to the same (common) memory bus ("common data signal line") (*id.* (citing Ex. 1008 ¶¶ 34–35, Fig. 3)). According to Petitioner, each DDR memory device has its own data pins (data bus) that are connected to a common data signal line, and the circuit of Amidi is

"electrically coupled" to the common data bus. *Id.* at 26; *see* Ex. 1007 ¶¶ 63, 72.

Petitioner provides arguments for the sending and receiving of input signals by the system in Amidi, and explains how Amidi discloses a circuit that is responsive to such input signals. *Id.* at 27–38. Petitioner also argues that Amidi teaches "selectively coupling" because Amidi discloses that CPLD 404, 604 is responsive to a set of input signals (address signal Add(b) and chip select signals cs0, csl) to determine ("selectively electrically coupling") an active rank of the four ranks and inactivating the other three ranks of memory devices from the computer system. *Id.* at 31–32 (citing Ex. 1008 ¶¶ 43, 44, 62); Ex. 1007 ¶ 66. According to Petitioner, the act in Amidi of activating one rank while deactivating other ranks constitutes "selectively coupling" and "selectively isolating." *Id.*

Petitioner then contends Amidi discloses that "memory module 400 includes 92 contact pins 402 on the front side for connecting with a memory socket," which is a system memory domain. *Id.* at 37 (citing Ex. 1008 ¶ 37). According to Petitioner, Amidi discloses that module connector 602 (contact pins 402 and 416) sends cs0 and cs1 signals, which can be considered "first number of chip-select signals," to CPLD 604. *Id.*

Patent Owner contests Petitioner's position, arguing that Amidi fails to disclose a "circuit . . . selectively isolating one or more loads of the DDR memory devices from the computer system," as recited in the challenged claims. PO Resp. 46–50. According to Patent Owner, "choosing a rank of memory devices and inactivating other ranks is not selectively isolating a load of DDR memory circuits, because neither involves electrical separation from the computer system." *Id.* at 47. Patent Owner contends that Amidi

only teaches hard-wired lines in permanent connection to the same 72-line data bus. *Id.* at 47–48 (citing Ex. 1008 ¶¶ 34, 35, Fig. 3). Patent Owner supports its position with the declaration of Dr. Sechen, who testifies that

> the data bus lines from the memory controller at all times are electrically coupled to the memory devices. That's because there are no switches on the chip select signal lines nor the data bus lines to make possible any type of electrical decoupling.

Ex. 2002 ¶ 78. Patent Owner, thus, concludes that due to the permanent electrical connections of Amidi's data bus, there would never be electrical separation and, thus, the memory devices could never be subject to acts of "selectively isolating." PO Resp. 48.

Patent Owner further contends the limitation "selectively isolating one or more loads" is distinct from the term "selectively electrically coupling" and is not disclosed by Amidi. *Id.* at 46–47. Patent Owner argues that the rank activation and inactivation in Amidi is "some kind of operational isolation" but is not a load isolation within the scope of the claims. *Id.* at 49.

We do not agree with Patent Owner's position that hard-wired data signal lines cannot be electrically isolated in a selective fashion. As discussed above, we construe "selectively electrically isolating" as "making a selection between at least two components and not transferring power or signal information from one selected component to the other selected component." *See supra*, Section II.A.2. Amidi's disclosure of directing electrical signals down a specific signal line or data bus in order to electrically activate a rank within the memory devices and electrically inactivate other ranks falls within the scope of the term "selectively electrically isolating" as we have construed the term. We are further unpersuaded by Patent Owner's argument that "selectively isolate" or

"selectively electrically isolating" is limited narrowly to a particular kind of load isolation. The '150 patent defines the term "load" broadly and includes "*without limitation*, electrical load, such as capacitive load, inductive load, or impedance load." Ex. 1001, 5:3–5 (emphasis added). Thus, Patent Owner's arguments are not commensurate with the '150 patent definition of "load" or with the scope of the challenged claims.

Based on the evidence of record, we agree with Petitioner's position that challenged claims 22, 24, and 26 are anticipated by Amidi. First, we are persuaded by Petitioner's reasoning and the evidentiary record that Amidi discloses the recited limitations of claim 22. *See* Ex. 1001, 43:35–61. Specifically Amidi discloses: (i) a circuit with a logic element, a register, and a PLL (*see* Ex. 1008 ¶¶ 34–39, 41, Fig. 4A); (ii) a circuit mounted on a memory module that is electrically coupled to a plurality of DDR memory devices arranged in ranks on a memory module (*see id.* ¶¶ 4, 12, 34–39, Fig. 4A); (iii) the memory module electrically coupled to a memory controller (*see id.* ¶¶ 29–32, 41); (iv) the memory module received a set of input signals (*see id.* ¶¶ 29–32, 50, 58, Fig. 3); (v) the circuit responsive to the input signals by selectively isolating one or more loads of the DDR memory devices from the computer system (*see id.* ¶¶ 38, 39, 43, 44, 62, Fig. 6A); and (vi) the circuit translates between the system memory domain of the computer system and a physical memory domain of the plurality of the DDR memory devices (*see id.* ¶¶ 34, 35, 37, 41–43, 49, 50, 52, 57, 60, 62, Figs. 5, 7).

Second, we are persuaded by Petitioner's reasoning and the evidentiary record that Amidi discloses the additional recited limitations of claim 26. Dependent claim 26 further recites that the claimed circuit is

"configurable to selectively isolate a data signal line of a DDR memory device of the plurality of DDR memory devices from the computer system." Ex. 1001, 44:8–11. Amidi teaches that the PLL and register isolate the loads of the memory devices that are not enabled by the chip select signal generated by the CPLD. *See* Ex. 1008 ¶¶ 38–39, 43, 62, Figs. 4A, 5. According to Petitioner, a person of ordinary skill in the art would recognize that selectively isolating the loads of the memory devices would necessarily require isolating the data signal lines of the memory devices from the computer system. Pet. 39-40 (citing Ex. 1007 ¶¶ 72, 105). We agree.

We are not persuaded, however, by Petitioner's reasoning and the evidentiary record that Amidi discloses the additional limitations of claim 24 as specifically recited and arranged in claim 24. Dependent claim 24 recites "wherein the two or more of the logic element, the register, and the phase-lock loop device are portions of a single component." Ex. 1001, 44:1–3. Amidi discloses that the CPLD ("logic element"), register, and PLL are all mounted on a memory module. Ex. 1008 ¶¶ 37, 39, 40, Figs. 4A, 4B, 6). According to Petitioner, a person of ordinary skill in the art would recognize that at least the register and PLL could be portions of a single component. Pet. 38 (citing Ex. 1007 ¶¶ 58, 108). Amidi, however, does not disclose specifically, nor is it inherent in Amidi, that two or more of the logic element, the register, and the phase-lock loop device mounted on a single memory module are portions of a single component. Therefore, we are not persuaded Petitioner has carried its burden to demonstrate, by a preponderance of the evidence, that Amidi anticipates claim 24 of the '150 patent.

Accordingly, we hold that Petitioner has shown by a preponderance of the evidence that claims 22 and 26 of the ’150 patent are unpatentable under 35 U.S.C. § 102(e) as anticipated by Amidi.

## III. CONCLUSION

We conclude Petitioner has shown by a preponderance of the evidence that (1) claims 15–17, 22, 24, 26, and 31–33 of the ’150 patent are unpatentable under 35 U.S.C. § 103(a) as having been obvious over the combinations of Ludwig and Amidi and (2) claims 22 and 26 of the’150 patent are unpatentable under 35 U.S.C. § 102(e) as anticipated by Amidi.

## IV. ORDER

For the reasons given, it is

ORDERED that, by a preponderance of the evidence, claims 15–17, 22, 24, 26, and 31–33 of the ’150 patent are unpatentable; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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