Trials@uspto.gov
Tel: 571-272-7822

Paper 10
Entered: September 10, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HEWLETT-PACKARD COMPANY
Petitioner

v.

MCM PORTFOLIO, LLC
Patent Owner

Case IPR2013-00217
Patent 7,162,549

Before SCOTT R. BOALICK, JONI Y. CHANG, and JENNIFER S. BISK, *Administrative Patent Judges*.

BISK, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

Hewlett-Packard Company ("HP") filed a petition (Paper 2) ("Pet.") to institute an *inter partes* review of claims 7, 11, 19, and 21 of Patent 7,162,549 (the "'549 patent"). 35 U.S.C. § 311. MCM Portfolio, LLC ("MCM") timely filed a Preliminary Response (Paper 9) ("Prelim. Resp."). We conclude that HP has satisfied its burden to show that, under 35 U.S.C. § 314(a), there is a reasonable likelihood that it would prevail with respect to at least one of the challenged claims.

HP contends that the challenged claims are unpatentable under 35 U.S.C. §§102 and/or 103 based on the following specific grounds (Pet. 7):

Reference[s] [1]	**Basis**	**Claims challenged**
AwYong	§ 102	7, 11, 19, and 21
Battaglia	§ 103	7, 11, 19, and 21
Battaglia and the Samaung Datasheet	§ 103	7, 11, 19, and 21
Kobayashi and Kikuchi	§ 103	7, 11, 19, and 21

[1] U.S. Patent 6,987,927 (Ex. 1004) ("Battaglia"); U.S. Patent 6,199,122 (Ex. 1005) ("Kobayashi"); WO 98/03915 (Ex. 1007) ("Kikuchi"); Chee-Kong AwYong, An Integrated Control System Design of Portable Computer Storage Peripherals, Master's Thesis, National Chiao-Tung University, published Dec. 22, 2000 (Ex. 1003) English Translation (Ex. 1002) ("AwYong"); Samsung SmartMedia Card Model No. K9D1208V0M-SSB0 Datasheet (Nov. 20, 2000) (Ex. 1006) ("Samsung Datasheet").

For the reasons described below, we institute an *inter partes* review of claims 7, 11, 19, and 21 based on obviousness over Kobayashi combined with Kikuchi.

We decline to institute *inter partes* review based on the following grounds: (1) anticipation by AwYong; (2) obviousness over Battaglia; and (3) obviousness over Battaglia combined with the Samsung Datasheet.

B. Related Proceedings

The parties list several cases pending in the Eastern District of Texas that would affect or be affected by the decision in this proceeding, including *Technology Properties Limited, LLC v. Hewlett-Packard Co.*, Docket No. 6:12-cv-208 (E.D. Tex. Mar. 28, 2012), in which the '549 patent is asserted against Petitioner. *See* Pet. 1; Paper 6 at 1. That case currently is stayed pending resolution of a related proceeding before the United States International Trade Commission ("ITC") that also involves the '549 patent, ITC Inv. No. 337-TA-841. *Id.* In addition, the '549 patent is the subject of a pending reissue proceeding, U.S. Application No. 12/351,691. The Board ordered a stay of that proceeding pending the termination or completion of this proceeding. Paper 8.

C. The Invention

The '549 patent relates to controllers for flash-memory cards. Ex. 1001, col. 1, ll. 21-22. As described in the "Background of the Invention," at the time of the invention, removable flash-memory cards commonly were used with digital cameras to allow for convenient transfer of images from the camera to a personal computer. *Id.* at col. 1, ll. 26-56. These prior art flash-memory cards were available in several formats, including CompactFlash, SmartMedia, MultiMediaCard (MMC), Secure Digital Card (SD), and Memory Stick card. *Id.* at col. 2, ll. 28-55. Each of the card formats required a different interface adapter

to work with a personal computer. *Id*. at col. 3, ll. 9-25. The Specification describes a need for a flash-memory card reader that accepts flash-memory cards of several different formats using a universal adapter. *Id*. at ll. 52-63. In response to this need, the '549 patent describes various improvements to flash-memory card readers, including by determining whether a particular flash-memory card includes a controller, and if not, performing operations to manage error correction for the flash-memory card. *Id*. at col. 3, l. 53- col. 4, l. 26; col. 28, ll. 42-60.

Claims 7 and 11, reproduced below, are illustrative of the claimed subject matter:

7. A method comprising:

using a controller chip to interface a flash storage system with or without a controller to a computing device, the controller chip comprising a flash adapter, wherein the flash storage system comprises a flash section and at least a medium ID;

determining whether the flash storage system includes a controller for error correction; and

in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

11. A system comprising:

a computing device;

a flash storage system comprising a flash section and at least a portion of a medium ID; and

a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device, the controller chip comprising an interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems, a detector to determine whether the flash storage system includes a controller

> for error correction and a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

D. Claim Construction

As a step in our analysis for determining whether to institute a trial, we determine the meaning of the claims. Consistent with the statute and the legislative history of the AIA, the Board will interpret claims using the broadest reasonable construction. *See* 37 C.F.R. § 42.100(b); *Office Patent Trial Practice Guide*, 77 Fed. Reg. 48756, 48766 (Aug. 14, 2012).

1. "Flash Adapter" and "Flash Adapter Section"

HP proposes that the broadest reasonable construction of "flash adapter" and "flash adapter section" is that adopted in the related ITC Investigation—"a section of the controller chip that enables communication with the flash storage system." Pet. 8 (citing Ex. 1030, pp. 73-77). MCM agrees with that construction. Prelim. Resp. 11. We find that this definition is reasonable and supported by the claim language, and thus adopt this definition for purposes of this decision.

2. "Error Correction" and "Bad Block Mapping"

HP does not set forth an explicit construction for the terms "error correction" or "bad block mapping." MCM, however, argues that HP incorrectly construes the term "bad block mapping" as distinct from "error correction." Prelim. Resp. 11. (citing Ex. 1008 ("Banjeree Decl.") ¶ 28). MCM instead proposes a construction of the term used by the examiner during original prosecution—"bad block mapping is a form of error correction." Prelim. Resp. 11-12 (citing Ex. 1015 at 415).

"Bad block mapping" is not defined explicitly in the written description of

the '549 patent. The plain and ordinary meaning of "bad block" is "a faulty memory location." MICROSOFT COMPUTER DICTIONARY 41 (4th ed. 1999). The plain and ordinary meaning of "a memory map" is "a description of the layout of objects in an area of memory." *Id*. at 281. Thus, the plain and ordinary meaning of "bad block mapping" is a description of the layout of those faulty memory locations, kept so that they are not accessed. Under a broadest reasonable construction, bad block mapping is thus a type of error correction.

This construction also is consistent with the Specification, which states that "the primary reason for including a controller section in a flash medium is for error correction. This task is now shifted either to firmware 4012*b* of the host computer, which now on top of its normal access section software, also manages error correction and bad block mapping of chip(s) 4022 and stores those parameters in flash medium 4020*b* itself." Ex. 1001, col. 28, ll. 53-58. This is the only place, outside the claims, that the term "bad block mapping" is used in the '549 patent. However, the claim language also supports this construction. Claim 7 recites "using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section," and claim 11 recites "operations to manage error correction of the flash section, including bad block mapping of the flash section."

For these reasons, for purposes of this decision, we construe the term "bad block mapping" to be a type of "error correction."

II. ANALYSIS

A. 35 U.S.C. § 315(b)

MCM argues that institution of an *inter partes* review is barred under 35 U.S.C. § 315(b).[2] Section 315(b) states as follows:

> An inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.

MCM asserts that Pandigital, Inc. is a privy of HP and, therefore, a complaint served on Pandigital by MCM in 2011, more than one year prior to the filing of the Petition in this case, filed by HP on March 27, 2012, should trigger § 315(b). Prelim. Resp. 5 (citing Ex. 2001 (*Technology Properties Limited LLC v. Pandigital, Inc.*, No. 2:11-cv-00372-TJW (E.D. Tex. 2011) (the "Texas Action"))). MCM bases this allegation on the fact that HP resells Pandigital products accused of infringing the '549 patent in the Texas Action. *Id.* at 5-6 (citing Ex. 2003 at 20 (HP User Guide)). According to MCM, the Petition in this case is filed more than one year after service of the complaint on Pandigital, a privy of HP. Prelim. Resp. 5-9.

MCM does not provide persuasive evidence that HP and Pandigital are privies for purposes of § 315(b). "Whether a party who is not a named participant in a given proceeding nonetheless constitutes a 'real party-in-interest' or 'privy' to that proceeding is a highly fact-dependent question." *Office Patent Trial Practice Guide*, 77 Fed. Reg. 48759 (citing *Taylor*, 553 U.S. 880). "The Office intends to

[2] MCM asserts that HP "lacks standing" to bring this IPR. Standing technically is not a requirement in an IPR. *See, e.g., Office Patent Trial Practice Guide*, Fed. Reg. at 48759 ("[The notion of 'real party-in-interest'] reflects standing concepts, but no such requirement exists in the IPR or PGR context.").

evaluate what parties constitute 'privies' in a manner consistent with the flexible and equitable considerations established under federal caselaw." *Id*. Petitioner provides no persuasive evidence that HP could have exercised control over Pandigital's participation in the Texas Action. Thus, § 315(b) does not bar institution of *inter partes* review based on HP's Petition.

MCM bases its privity argument solely on its assertion that HP and Pandigital are successive owners of the same allegedly infringing property. Prelim. Resp. 7 (citing *Taylor v*. *Sturgell*, 553 U.S. 880, 894 (2008)). We are not persuaded that this allegation alone is enough to confer privity for purposes of § 315(b). *See Synopsys v*. *Mentor Graphics Corp*., IPR2012-00042, Decision to Institute, Paper 16 (Feb. 22, 2013) ("*Synopsis*"). Under *Synopsis* "any potentially infringing products are irrelevant to the issues raised in the Petition, all of which involve patentability." *Synopsis* at 17.

B. *Priority Date for the '549 Patent Claims*

The '549 patent claims the benefit of one provisional application and is a continuation-in-part of four non-provisional applications. Ex. 1001, col. 1, ll. 6-17; Certificate of Correction (Jan. 9, 2007). MCM asserts that the effective filing date of the challenged claims is the earliest filing date of these applications—application No. 09/610,904, filed July 6, 2000 (now U.S. Patent 6,438,638) (the "'904 application"). Prelim. Resp. 17-18. HP, on the other hand, asserts that the challenged claims are entitled to an effective filing date no earlier than June 4, 2002. Pet. 3.

In this case, the effective filing date of the '549 patent (i.e., whether it is entitled to the benefit of the '904 application's filing date) is relevant because several of the asserted references post-date the filing date of the '904 application. In particular, although AwYong is stamped with a date of June 2000, HP states that

it was "published and publicly available as of December 22, 2000," several months after the filing of the '904 application. In addition, Battaglia has a filing date of July 13, 2000, and HP states that the Samsung Datasheet was available by November 20, 2000—both of which are after the '904 application's filing date.

HP provides little explanation regarding its proposed effective date, basing its entire argument on the statement that "[i]n the related ITC Investigation, the Patent Owner's exclusive licensee – Technology Properties Limited, LLC ('TPL') – agreed that June 4, 2002 is the effective filing date of the '549 Patent." Pet. 3 (citing Ex. 1008 ("Banerjee Decl.") ¶ 33). HP does not explain why the actions of MCM's licensee in another proceeding would be applicable here; nor does HP provide any evidence, aside from one conclusory statement by an expert, Dr. Banerjee, to support this assertion. *Id*.

Other than the conclusory statement regarding the related ITC Investigation, we find no other evidence in the record[3] to support the proposed 2002 effective date except the testimony of Dr. Banerjee, who states that "Claims 7, 11, 19, and 21 of the '549 Patent are entitled to a priority date of no earlier than June 4, 2002" because the concepts of interfacing with "intelligent" and "dumb" flash cards do not appear until a provisional application on June 4, 2002. Ex. 1008 ¶¶ 33-34. HP, however, does not provide any of the underlying evidence upon which these conclusions are based. We, therefore, give them minimal weight. 37 C.F.R. § 42.65. None of the applications to which the '549 patent claims benefit have been entered into the record in this case. Moreover, Dr. Banerjee's statement does not refer to all those applications. Specifically, Dr. Banerjee does not mention the

[3] HP did not cite to any other testimony in its Petition, but MCM does refer to other testimony by disputing that testimony in its response. Prelim. Resp. 17-18.

'904 application, included in the certificate of correction, which has the earliest filing date—July 6, 2000; instead, he specifically discusses only the applications listed in the first column of the '549 patent. *Id*. at ¶ 34. Thus, it is unclear from the testimony whether Dr. Banerjee studied or was aware of the earliest claimed application.

Because we are not persuaded by HP's contention that the challenged claims are not entitled under 35 U.S.C. § 120 to the benefit of the filing date of the '904 application, HP has not shown sufficiently that AwYong, Battaglia, or the Samsung Datasheet are eligible as prior art for purposes of this decision. Thus, we decline to institute *inter partes* review based on any of those references.

C. Obviousness over Kobayashi and Kikuchi

HP argues that claims 7, 11, 19, and 21 of the '549 patent are obvious over Kobayashi combined with Kikuchi. Both Kobayashi and Kikuchi pre-date the filing date of the '904 application. Kobayashi is a U.S. patent that was filed July 22, 1998 and Kikuchi is a PCT application published January 29, 1998.

1. Kobayashi

Kobayashi describes a memory device for a computer with a converter that converts serial commands of the computer to parallel commands that then are used to control a storage medium (which can be a flash-memory card). Ex. 1005, col. 2, ll. 55-64; col. 3, ll. 63-65. This configuration is shown in Figure 1.

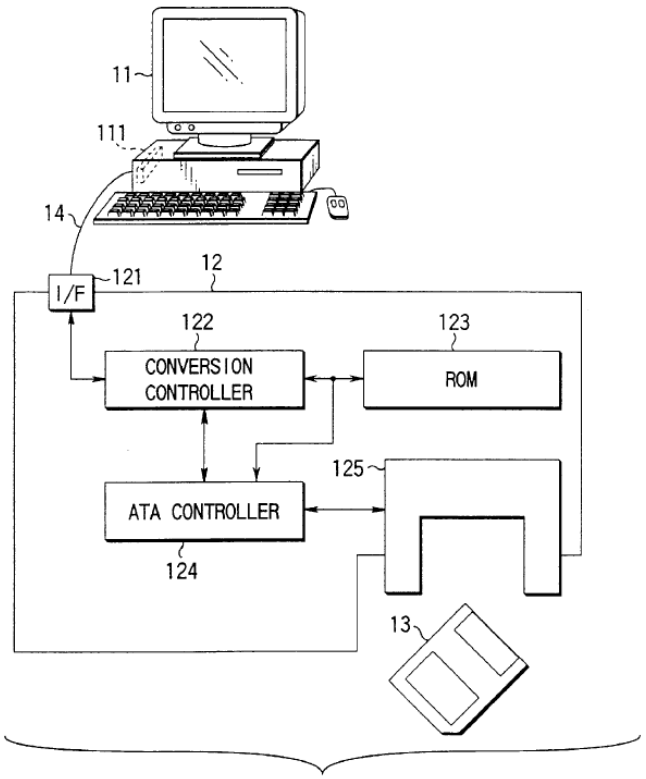


FIG. 1

Figure 1 of Kobayashi, reproduced above, is a block diagram of a computer 11 with a reader/writer 12 and flash-memory card 13. Ex. 1005, col. 5, ll. 54-58. The reader/writer includes a conversion controller 122, an ATA (AT Attachment) controller 124, and a connector 125 for reading a flash-memory card 13. *Id*. at col. 6, ll. 5-9. In the first of several embodiments described by Kobayashi, the flash-memory card 13 does not have a controller on the card. *Id*. at col. 6, ll. 1-4 ("The memory card 13 functions as what is called a silicon disk or a PC card according to the ATA standard, and stores data and reads, outputs and erases the stored data under an *external control*.") (emphasis added). A second embodiment described by Kobayashi includes a flash-memory card 13 with a controller arranged in the memory card. *Id*. at col. 12, ll. 44-46, 59-63. A third embodiment is shown in Figure 11.

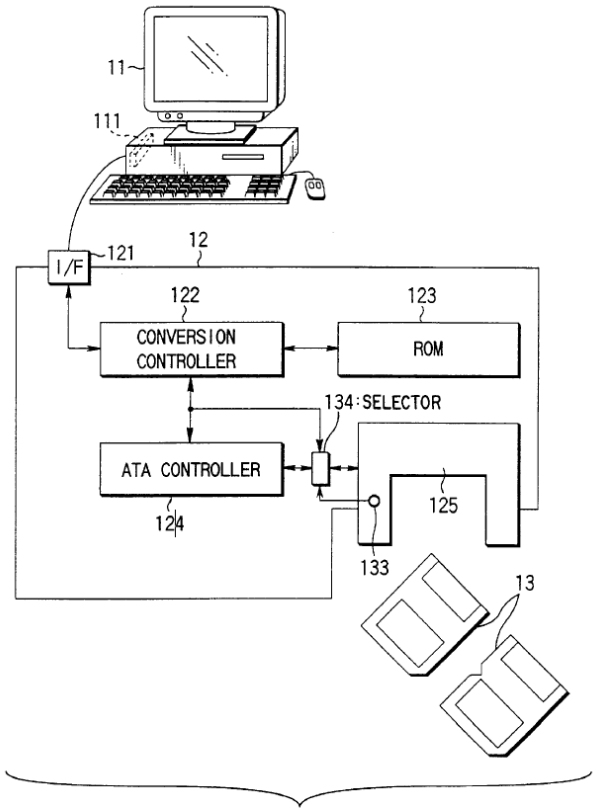


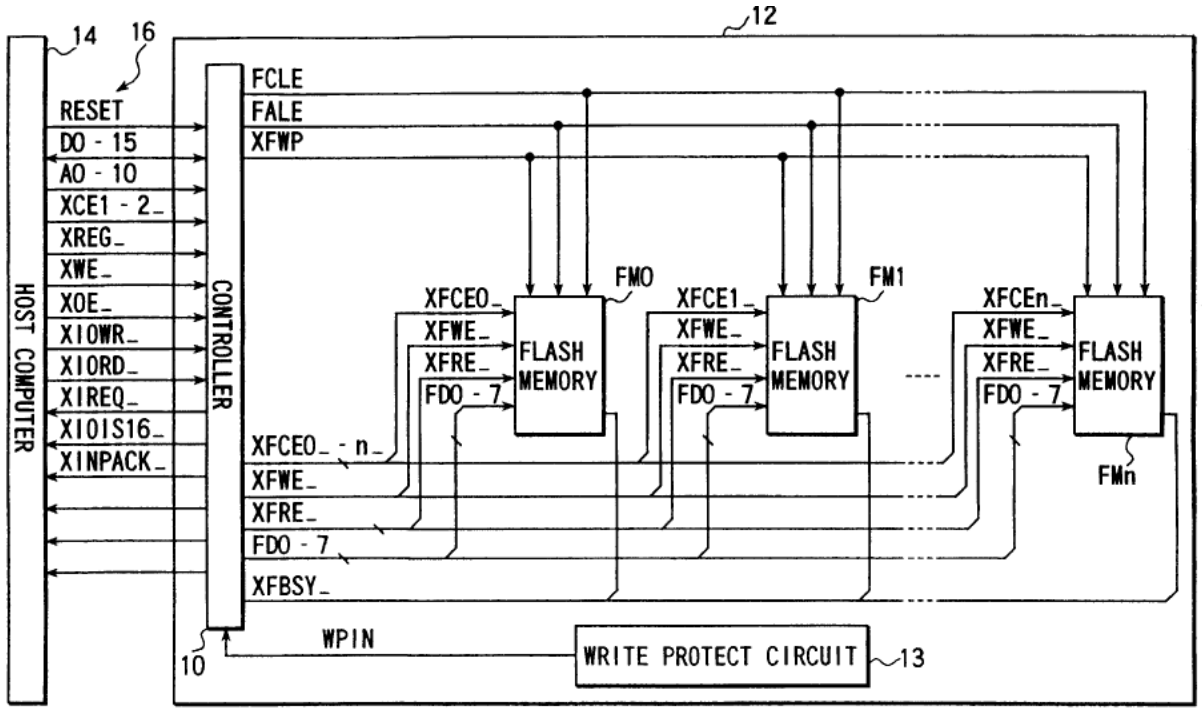
FIG. 11

In this third embodiment, flash-memory cards 13 both with and without controllers may be used. *Id*. at col. 12, ll. 59-65. A sensor 133 determines the type of flash-memory card 13 mounted on the connector 125. *Id*. at col. 12, l. 59 – col. 13, l. 2. When a flash-memory card with no controller is detected, a selector 134 connects the ATA controller 124 and the connector 125. *Id*. at col. 13, ll. 2-5. When a flash-memory card with a controller is detected, a selector 134 connects the conversion controller 122 and the connector 125.

2. Kikuchi

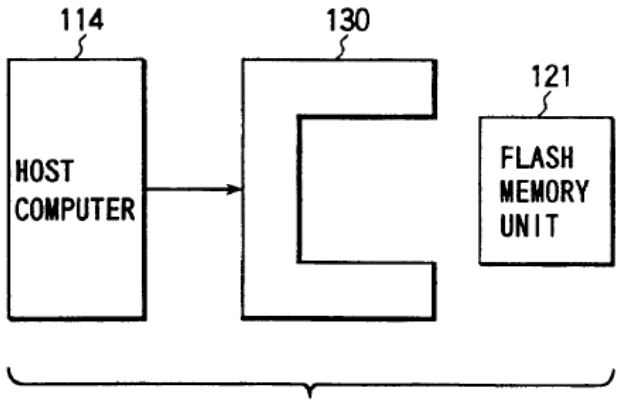
Kikuchi describes a flash-memory card and a controller 10 having an interface connected to a host computer 14. Ex. 1007, Abstract. Figure 1 of Kikuchi, reproduced below, shows the flash memory card with a controller on the

flash-memory card. *Id*. at p. 9, ll. 10-15.



F I G. 1

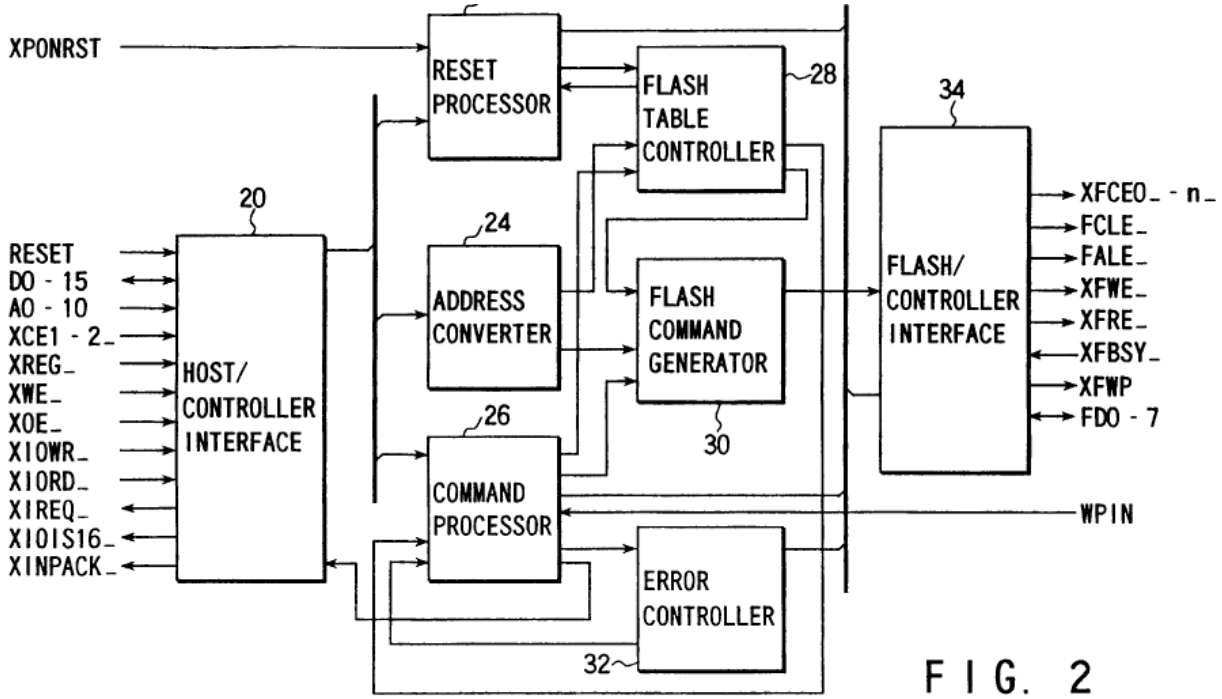
Figure 15A of Kikuchi, reproduced below, shows a flash-memory card with no controller. Ex. 1007, p. 33, ll. 22-25.



F I G. 15B

Figure 2, reproduced below, is a block diagram showing the functional

arrangement of the controller 10.



F I G. 2

In Figure 2, above, the error controller 32 performs error control in read and write operations and performs bad block mapping, for example, "a block substitute process or the like in the event of a failure or error." Ex. 1007, p. 13, ll. 17-21. Further, in another embodiment, controller 10 "refers to the block quality flag contained in the block status information of the redundant portion of the readout information . . . to check whether the head block BL0 is non-defective or not" and "detects a non-defective block BLj having the highest address rank." *Id*. at p. 22, l. 20 – p. 23, l. 5.

3. The Combination of Kobayashi and Kikuchi

HP asserts that Kobayashi discloses every limitation recited by all the challenged claims, except that HP concedes that Kobayashi is silent on the details of how error correction is performed and, in particular, does not mention bad block mapping. Pet. 47-48. HP relies on Kikuchi for teaching the details of error

correction, including bad block mapping, done in firmware. Pet. 48-50. HP contends that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the two references, which both describe ATA controllers that work with flash-memory cards with or without on-card controllers, in order to "reliably retain stored data." Pet. 50 (citing Banerjee Decl. ¶ 121 (quoting Ex. 1007 (Kikuchi), p. 6, ll. 1-3)). We have reviewed HP's evidence in relation to each of the challenged claims and find that the evidence supports HP's contentions.

MCM argues that Kobayashi does not disclose using firmware to perform the error correction in the event that the flash-memory card is without a controller, as required by all the challenged claims. Prelim. Resp. 29. This argument is not persuasive because MCM concedes that Kikuchi discloses a controller using firmware to perform error correction. *Id*. at 29-31 (stating that Kikuchi discloses "a controller in a card reader that has a microprocessor that conducts bad block mapping in firmware").

MCM argues that Kikuchi's controller chip could not be incorporated into Kobayashi's controller. Prelim. Resp. 31-32. Moreover, MCM adds that even if Kikuchi's controller chip could be incorporated into Kobayashi's controller, it would not yield the claimed invention because Kobayashi discloses two controllers—a conversion controller 122 and an ATA controller 124—not one controller chip with all the required functionality. Prelim. Resp. 33-34.

Neither argument is persuasive. "It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (citing *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (noting that the criterion for obviousness is not whether the references can be

combined physically, but whether the claimed invention is rendered obvious by the teachings of the prior art as a whole)). On this record, we determine that the petition and supporting evidence demonstrate sufficiently that combining the teachings of Kobayashi and Kikuchi merely is a predictable use of prior art elements according to their established functions—an obvious improvement. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

Finally, MCM argues that Kobayashi was considered by the Examiner during prosecution (Prelim. Resp. 25) and Kikuchi is cumulative of art that was before the Examiner during prosecution (Prelim. Resp. 29-30). While we are mindful of the burden on MCM and the Office in analyzing previously considered prior art, substantially the same prior art and arguments were not before the Office previously. *See* 35 U.S.C. § 325(d). Moreover, for the reasons explained above, we conclude that HP's arguments based on the combination of Kobayashi and Kikuchi have merit.

III. CONCLUSION

We institute an *inter partes* review of claims 7, 11, 19, and 21 based on obviousness over Kobayashi combined with Kikuchi.

IV. ORDER

For the reasons given, it is

ORDERED that the Petition is granted as to claims 7, 11, 19, and 21 of the '549 patent on the alleged ground of obviousness over Kobayashi combined with Kikuchi under 35 U.S.C. § 103.

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '549 patent hereby is instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice

hereby is given of the institution of a trial.

FURTHER ORDERED that an initial conference call with the Board is scheduled for **2 PM Eastern Time** on **October 9, 2013**. The parties are directed to the *Office Trial Practice Guide*, 77 Fed. Reg. at 48765-66 for guidance in preparing for the initial conference call, and should come prepared to discuss any proposed changes to the Scheduling Order entered herewith and any motions the parties anticipate filing during the trial.

PETITIONER:

Robert L. Hails, Jr.
T. Cy Walker
KENYON & KENYON LLP
HP549IPR@kenyon.com

PATENT OWNER:

Edward P. Heller III
Christopher Brittain
Alliacense Limited LLC
ned@alliacense.com
chris@alliacense.com