United States Court of Appeals for the Federal Circuit

00-1078

OAK TECHNOLOGY, INCORPORATED,

Appellant,

v.

INTERNATIONAL TRADE COMMISSION,

Appellee,

and

MEDIATEK, INC., UNITED MICROELECTRONICS CORP., LITE-ON TECHNOLOGY CORP., and AOPEN, INC.,

Intervenors.

Joel M. Freed, Howrey Simon Arnold & White, LLP, of Washington, DC, argued for appellant. With him on the brief were Michael J. Songer, Christopher L. Kelley, and Thomas C. Fiala.

Timothy P. Monaghan, Attorney, Office of the General Counsel, U.S. International Trade Commission, of Washington, DC, argued for appellee. With him on the brief were Lyn M. Schlitt, General Counsel; and James A. Toupin, Deputy General Counsel. Of counsel was Andrea C. Casson, Attorney.

James C. Otteson, Wilson Sonsini Goodrich & Rosati, of Palo Alto, California, argued for intervenors. With him on the brief were Michael A. Ladra, and Lisa G. McFall.

Appealed from: United States International Trade Commission

United States Court of Appeals for the Federal Circuit

00-1078

OAK TECHNOLOGY, INCORPORATED,

Appellant,

v.

INTERNATIONAL TRADE COMMISSION,

Appellee,

and

MEDIATEK, INC., UNITED MICROELECTRONICS CORP.,
LITE-ON TECHNOLOGY CORP., and AOPEN, INC.,

Intervenors.

DECIDED: May 2, 2001

Before NEWMAN, CLEVENGER, and BRYSON, Circuit Judges.

CLEVENGER, Circuit Judge.

Oak Technology, Incorporated ("Oak") appeals from the final determination of the United States International Trade Commission ("Commission") that Oak's United States Patent No. 5,581,715 ("the '715 patent") is not infringed by Intervenors MediaTek, Inc., United Microelectronics Corporation, Lite-On Technology Corporation, and AOpen, Inc. (together "MediaTek"). We hold that the Commission correctly interpreted the asserted claims of the '715 patent, and that substantial evidence supports the Commission's finding of noninfringement. Consequently, we conclude that the Commission correctly determined that no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337,[1] has been proven. We therefore affirm.

I

Section 337 of the Tariff Act of 1930 prohibits, inter alia, importation of articles into the United States which infringe the claims of valid and enforceable U.S. patents. 19 U.S.C. § 1337(a)(1)(B). The Commission is authorized to conduct investigations to determine whether

violations of section 337 have occurred, and if so to issue orders enjoining such violations. 19 U.S.C. § 1337(b). In this case, the Commission instituted an investigation at the behest of Oak, which alleged that MediaTek violated section 337 by importation of electronic products and/or components that infringe claims of the '715 patent. After an evidentiary hearing conducted in January 1999, the administrative law judge issued a preliminary determination finding no infringement of the claims of the '715 patent, and holding that the claims at issue are invalid on several grounds as well as not enforceable by reason of inequitable conduct arising during prosecution of the '715 patent.

Oak sought review by the Commission of the adverse preliminary determination. The Commission reversed the administrative law judge's invalidity and unenforceability decisions, but affirmed the finding of no infringement and consequently of no violation of section 337. Oak timely appealed the Commission's final determination to this court. We have jurisdiction over this appeal pursuant to 28 U.S.C. § 1295(a)(6).

II

The technology in this case concerns the transfer of information stored on a CD-ROM disk to a host computer, such as a typical personal computer. The acronym "CD-ROM" stands for "compact disk, read only memory." A host computer in the context of this case contains a CD-ROM drive, which manages the communication of data between the CD-ROM disk and the host computer. The CD-ROM drive itself contains a device known as a CD-ROM drive controller, typically implemented as a semiconductor integrated circuit ("IC" or "chip"). The invention described and claimed in the '715 patent relates to an improved CD-ROM drive controller which provides faster and simplified data communication.

As noted in the written description, before the invention claimed in the '715 patent, "[c]onventional CD drive designs support[ed] the Industry Standard Architecture (ISA) bus convention and

require[d] the insertion of an interface card or host adapter card into an ISA input/output bus slot of the host personal computer." '715 patent, col. 1, ll. 60-63. By 1994, the filing date of the application that matured into the '715 patent, an alternative and improved bus structure known as the IDE/ATA interface (which stands for "integrated drive electronics with an AT attachment interface"), was widely available. '715 patent, col. 2, ll. 20-26. As noted in the '715 patent, prior art CD-ROM drives had thus far failed to take advantage of the improved and widely available IDE/ATA standard bus structure:

> Conventional CD drives in the prior art failed to make use of the IDE/ATA bus. However, now that the [IDE/ATA] standard has become widely used in many personal computers, it would be desirable to provide a CD drive with built-in controller functionality and a standard connector. This would
>
> obviate the need for an additional host adapter card and associated electronics.

'715 patent, col. 2, ll. 35-41. Accordingly, the '715 patent describes and claims such an improved CD-ROM controller which incorporates the IDE/ATA bus structure.

The improved drive controller structure invention is not, however, the focus of this appeal. Instead, the manner in which the claimed CD-ROM controller achieves error detection and correction is at the heart of this case.

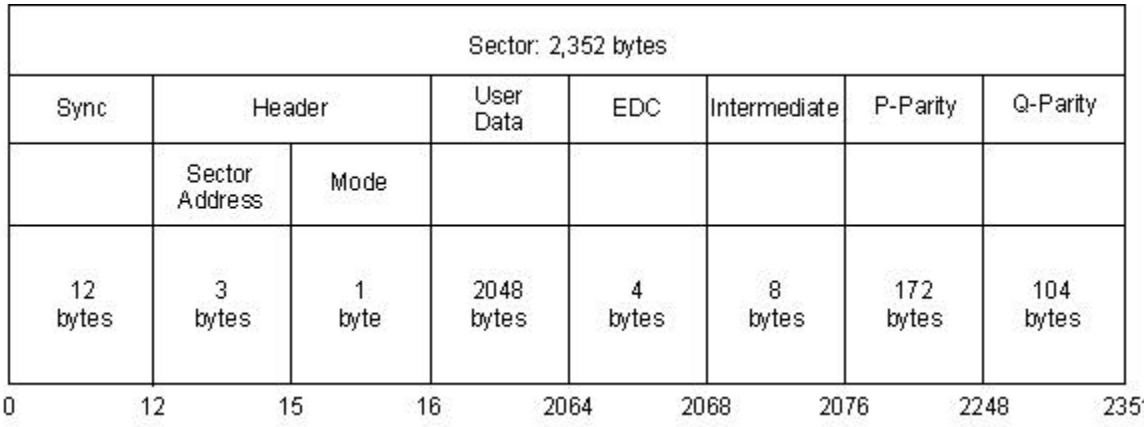
Well before the application for the '715 patent was filed, there is no dispute that it was commonly known that errors can be present in data that is retrieved by laser beam from a CD-ROM disk for communication with a host computer. Such errors can arise from a number of causes, including defects in the manufacture of a CD-ROM disk, scratches or dust particles on the disk surface, or electronic noise in the CD-ROM drive controller or in the host computer. Unless such errors are detected and corrected, the errors are likely to compromise the veracity of the information transferred from the disk to the host computer. Before 1994, persons of ordinary skill in the art knew how to construct CD-ROM controllers capable of retrieving digital data from a CD-ROM disk, temporarily storing the retrieved data in random access memory of the host computer,

checking such data for errors, and correcting the detected errors, if possible.

To a novice, it may seem fantastic that a CD-ROM controller could detect an error among the billions of bits on a CD-ROM disk, comprehend the nature of the mistake, and correct the error by supplying the correct information. How is such a fantasy made real?

As is common in many fields of endeavor, there are standard-setting bodies and standards that govern industry practice of storing information digitally on CD-ROM disks. By 1994, it was common to store information on such disks, and the industry had developed standards for the storage and formatting of data on such disks. One of those standards is International Standard ISO/IEC10149, also referred to as the "Yellow Book" standard, named after the color of the binder in which the standard commonly appears. The Yellow Book requires, among other things, that data be encoded onto CD-ROM disks in a specific format, and to that end it lays down specific standards for the storage of data on a CD-ROM disk. Oak readily admits that "Oak's patent contemplates Yellow Book compliance."

The Yellow Book specifies that digital data to be recorded on a CD-ROM "shall be represented by 8-bit bytes and grouped into Sectors," and that "[a] Sector is the smallest addressable part of the information area that can be accessed independently." A Sector (also referred to as a "block"),[2] contains 2352 bytes of data, and is subdivided into specifically identified regions. In the relevant operating mode (known as "Sector Mode 01") these regions are denominated as follows: Sync field, Header field, User Data field, EDC field, Intermediate field, P-Parity field and, finally, Q-Parity field. Reproduced immediately below is Figure 11 as set forth in the Yellow Book, which graphically illustrates the structure of a Sector in Sector Mode 01:



ed for synch 2-byte patter nique synch ector if synch ess (3 bytes) and Mode (1 byte). In general terms, the Sector Address indicates the elapsed time since the beginning of a data track on the disk (expressed in minutes, seconds, and fractions of a second). The 1-byte Mode field indicates whether a data track is formatted according to Sector Mode 00, 01, or 02. Since only Sector Mode 01 supports error detection and correction, it is the only mode of operation that is relevant to this appeal.

The User Data field contains the subject matter data of the CD-ROM, whether it be a portion of a text document, application software, or any other kind of information that is susceptible to digital encoding. The EDC ("error detection code") field "shall consist of 4 bytes recorded in positions 2 064 to 2 067. The error detection code shall be a 32-bit CRC [cyclic redundancy code] applied on bytes 0 to 2 063." The Intermediate field, containing 8 bytes of data, simply contains a string of sixty-four 0's, recorded in byte positions 2068 through 2075. The P-Parity and Q-Parity fields use, respectively, 172 and 104 bytes of data in order to facilitate error correction, as will be described in more detail later. Together, the Sync, Header, User Data and EDC fields form what is referred to as the "EDC codeword."

Among the reasons for the specific information formatting requirements of the Yellow Book is the need to address the problem of errors existing on the disk. To this end, the Yellow Book specifies that all Sectors of data encoded on a CD-ROM disk using Sector Mode 01 must support specific error detection and error correction functions. In general terms, error detection can be used to determine the presence, but not the location, of errors in the user data that has been read from a

CD-ROM disk. Specifically, error detection pursuant to the Yellow Book involves comparing the EDC code word to the user data using a cyclic redundancy code to determine the presence of errors. Error correction can also determine the location of errors in the user data, and can even attempt to reconstruct the correct user data.

To accomplish the function of error correction, the Yellow Book specifies a Reed-Solomon code. Reed-Solomon error correction has been in widespread use since the 1960s, and was the only type of error correction performed on CD-ROM disks as of 1994. Conceptually, to understand the theory and operation of this complex technology, an analogy may be drawn between aspects of Reed-Solomon error correction and aspects of the English language. In particular, the English language exhibits redundancy in spelling, such that not every combination of letters in the alphabet forms a valid word. Consequently, by taking advantage of this linguistic feature, a person is able to read a document containing numerous spelling mistakes, detect the spelling errors, correct those errors mentally, and understand the intended meaning of the text.

For example, "dig" and "dog" are valid words in the English language, but "dag" is not commonly used as a valid word in English. A typical person reading a document containing the phrase "the dag wagged his tail" would conclude that a spelling error had occurred, and would be able to correct it. This is true because the typical reader would be knowledgeable about the structure of the English language. Specifically, such a reader would know that only certain combinations of letters form valid words, and that only certain words are appropriate in a given context (e.g., that the correct substitution for "dag" in the above phrase is "dog" and not "dig").

A Reed-Solomon error correcting code ("ECC") is a very analogous structure, based on numbers instead of letters. With Reed-Solomon error correction, given a relatively long record of numbers (such as the 16,512 bits comprising bytes 12 through 2075 of each Sector of CD-ROM data), additional numbers are appended to the end of that record. These additional numbers are cross-checks on the numbers that are desired, and these cross-checks can be used to infer an

incorrect sequence of numbers overall, and therefore to correct the errors. In the context of CD-ROM technology based on the Yellow Book standard, the P-Parity and Q-Parity fields in each Sector mentioned earlier are used to perform this "cross-checking" function on the portion of each Sector which includes the Sector Address, Mode, User Data, and EDC fields (i.e., on bytes 12 through 2075 of each Sector).

For error detection, the Yellow Book requires a specific binary mathematical operation known to those of skill in the art as a "cyclic redundancy check." As of 1994, the most commonly available hardware structure for performing a cyclic redundancy check was known as a "linear feedback shift register." Conceptually, a cyclic redundancy check operation can be thought of as a form of long division operation. However, the relevant result for this operation is not the quotient, but the remainder. In the context of error detection, a zero-remainder condition as the result of a cyclic redundancy code ("CRC") operation implies that it is highly likely that there are no errors in the data being processed.

When each Sector of user data is encoded on a CD-ROM disk by the manufacturer, the corresponding array of user data can be thought of as a single long string of bits. In turn, this string of bits (over 16,000 bits long) can be thought of as a single very large binary number (analogous to the dividend in common arithmetic).

The Yellow Book sets forth a specific formula to calculate a 33-bit binary number, referred to as the "check polynomial." The check polynomial can be divided into the single large binary number represented by the long string of user data to obtain a remainder. The check polynomial is thus analogous to the divisor in the context of ordinary arithmetic. To ensure that the user data will be evenly divisible by the check polynomial (i.e., to ensure that the remainder will be zero), the Yellow Book requires that CD-ROM manufacturers append 32 bits (4 bytes) to the end of the user data. These additional 32 bits are known as the "error detection code" ("EDC"), which is stored in the EDC field of each Sector. As mentioned earlier, the user data and the EDC (along with

header and synchronization bytes) together make up what is known as the "EDC codeword."

The 4-byte error detection code appended to each Sector of data is unique for each Sector, because its value is equal to the binary number that must be added to the end of the user data to make the entire EDC codeword evenly divisible by the check polynomial. A resulting zero remainder would indicate that it is highly likely that no errors were introduced at read time. Thus, every Sector of CD-ROM data encoded on a disk at the time of manufacture includes its own 4-byte error detection code at the end of the EDC codeword.

In summary, the Yellow Book imposes very stringent data formatting requirements on each Sector of data on a CD-ROM disk, and certain regions of a Sector are used for error correction, while others are used for error detection. Specifically, the P-Parity and Q-Parity fields are used for error correction, while the EDC field is primarily used for error detection. However, it should also be noted that the Yellow Book specifies that the Reed-Solomon error correction code operates on bytes 12 through 2075 of each Sector, a portion of the Sector which necessarily includes the EDC field (which is stored at byte positions 2064 through 2067). To a person of ordinary skill in the art, this technical fact strongly implies that Reed-Solomon error correction should be performed by a CD-ROM controller before performing any CRC error detection. Thus, the structure of the data in a Sector is arranged in such a way pursuant to the Yellow Book so as to lead an ordinarily skilled artisan to visualize the error correction function taking place first, followed by the error detection function.

III

With this preliminary technical background in mind, we now turn to claim 1 of the '715 patent, the primary claim at issue on appeal. [4] Claim 1 states in its entirety as follows:

> 1. A compact disk drive controller to control the communication of data between a compact disk in a compact disk drive and a host computer via an

> IDE/ATA data bus, said data bus for receiving and transmitting data between said controller and said host computer, said disk drive having drive electronics that include a digital signal processor and a microcontroller, said controller comprising:
>
> a digital signal processor interface for receiving data from said digital signal processor, said digital signal processor interface descrambling and assembling data received from said digital signal processor;
>
> memory means for temporarily storing data, said memory means temporarily storing said assembled data;
>
> data error detection and correction means for correcting said assembled data, said detection and correction means including error correction circuitry for performing error correction on said assembled data and a cyclic redundancy checker for detecting errors in said assembled data after correction of said data by said correction circuitry for providing corrected data; and
>
> host interface means for connecting said host computer to said controller, said interface means adapted to receive data addresses and commands from said host computer and transmit corrected data to said host computer to insure an uninterrupted flow of data from said controller to said host computer.

'715 patent, col. 28, l. 64 – col. 29, l. 22. The limitations in claim 1 that provide for error correction and detection are not themselves new or novel. Instead, these limitations refer to the industry-standard procedures for achieving error correction and detection as of the date the application for the patent was filed.

As we noted above, the disagreement in this case is over the question of whether the accused MediaTek devices meet the limitations of claim 1 that require "performing error correction on said assembled data and . . . detecting errors in said assembled data after correction of said data by said correction circuitry . . . ."

IV

In order to resolve the dispute before it, the Commission first interpreted the key language in claim 1, the terms that require error correction and detection on "said assembled data" and that require error detection to occur, in the sequence of things, after correction of "said data." Oak appeals three of the Commission's rulings regarding claim interpretation.

First, Oak takes issue with the Commission's conclusion that "said assembled data" refers to an entire Sector of CD-ROM data, as opposed to an unspecified number of 8-bit bytes. Next, Oak disagrees with the Commission's interpretation of the "after" limitation. On this issue, the Commission ruled that the claim language requires that error correction occur first on an entire Sector of data, and that a cyclic redundancy check error detection operation is then performed on the corrected Sector of data. In contrast, Oak's position is that the claim language is broad enough to cover a situation in which the error detection operation commences before the error correction operation is completed. Finally, Oak argues that the Commission's interpretation of "cyclic redundancy checker" was overly narrow. The Commission concluded that "[t]he cyclic redundancy checker is hardware, commonly available in June 1994, that performs the division of a CRC generator binary polynomial into a 16,000-bit EDC code word to produce a CRC remainder." Instead, Oak argues that a cyclic redundancy checker is simply any circuitry that performs a cyclic redundancy check.

Based on the above legal conclusions with respect to claim interpretation, the Commission found that there was no infringement in this case, either literally or under the doctrine of equivalents, because the accused devices were found to lack a "data error detection and correction means" within the scope of claim 1. The Commission summarized its factual findings concerning the operation of the accused MediaTek devices as follows:

> As to the accused product, the MediaTek device first performs an error detection by a cyclic redundancy check on the entire CD-ROM block of data (generating an original CRC remainder), followed by Reed-Solomon error correction, followed by a second error detection. This second error detection is an update to the original CRC remainder with 20 bits of error location and error pattern data from the Reed-Solomon error correction operation. In this second error detection operation, the original CRC remainder is decremented until it equals zero, indicating that all errors have now been corrected.

Thus, the Commission found that the accused devices first perform a CRC error detection operation on a Sector of data, followed by Reed-Solomon error correction on the output of the first

error detection operation, followed by a second error detection operation.

After characterizing the accused devices, the Commission then applied the interpreted claims to the accused devices, and concluded that the second error detection in the accused devices was not a "cyclic redundancy check" as required by the claim. In essence, the Commission found that there was no literal infringement because the accused devices do not contain a cyclic redundancy checker that operates on a Sector of CD-ROM data after a Reed-Solomon error correction function has been completed on the Sector of data. Finally, as will be described in more detail later, the Commission also concluded that there was no infringement under the doctrine of equivalents because the differences between the accused devices and the asserted claims were not insubstantial with respect to the claimed "data error detection and correction means."

Oak appeals from the Commission's final determination, seeking review of the Commission's factual findings on infringement and of the underlying claim interpretation.

V

We review the Commission's factual findings under the "substantial evidence" standard. 5 U.S.C. § 706(2)(e); Intel Corp. v. United States Int'l Trade Comm'n, 946 F.2d 821, 832, 20 USPQ2d 1161, 1171 (Fed. Cir. 1991). Pursuant to this standard, we will not disturb the Commission's factual findings if they are supported by "such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." Finnigan Corp. v. United States Int'l Trade Comm'n, 180 F.3d 1354, 1362, 51 USPQ2d 1001, 1006 (Fed. Cir. 1999) (quoting Surface Tech., Inc. v. United States Int'l Trade Comm'n, 801 F.2d 1336, 1340-41, 231 USPQ 192, 196 (Fed. Cir. 1986)). Because findings on infringement, whether literal or under the doctrine of equivalents, are questions of fact, they are therefore reviewed under the substantial evidence standard in an appeal from a final determination of the Commission. SSIH Equip. S.A. v. United States Int'l Trade Comm'n, 718 F.2d 365, 371-72, 218 USPQ 678, 684 (Fed. Cir. 1983). Claim construction, however, is a question of

law, which we review de novo. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979, 34 USPQ2d 1321, 1329 (Fed. Cir. 1995), aff'd 517 U.S. 370, 38 USPQ2d 1461 (1996).

VI

As an initial observation regarding claim interpretation in this case, we note that the plain language of the disputed limitation of claim 1 explicitly requires certain interactions between the "error correction circuitry," the "cyclic redundancy checker," and "said assembled data." First, the "error correction circuitry" must "perform[ ] error correction on said assembled data." Next, the "cyclic redundancy checker" must "detect[ ] errors in said assembled data after correction of said data by said correction circuitry," and must ultimately "provid[e] corrected data." These required interactions, based solely on the plain language of the claim, support the Commission's observation that the claim language contemplates and explicitly describes a sequential process.

According to the plain language of the claim, the "assembled data" is processed by the "error correction circuitry" and converted into "corrected assembled data." This "corrected assembled data" is then processed by the "cyclic redundancy checker," which finally provides "corrected data." It should also be noted that the plain language of the claim indicates that the "cyclic redundancy checker" does not operate on the original "assembled data," but instead "detect[s] errors in said assembled data after correction of said data by said correction circuitry." In other words, the plain language of the claim specifies that the cyclic redundancy checker operates on the output of the "error correction circuitry."

A

We now focus on the correct interpretation of "said assembled data" in the context of the asserted claims of the '715 patent, and conclude that the Commission was correct in ruling that "said assembled data" refers to an entire Sector of CD-ROM data as it is stored in random access

memory ("RAM").

The intrinsic record in this case is entirely consistent with this interpretation. The '715 patent contemplates a two-step data "assembly" process as data is read from the CD-ROM disk. First, the bit-by-bit serial stream of CD-ROM data is assembled into 8-bit bytes. Then, as specified by the Yellow Book, a group of bytes of the appropriate size is assembled into a Sector and stored in RAM. The written description of the '715 patent confirms this two-step data assembly process:

> [T]he drive controller 10 accepts digital data from the CD drive's electronics 12, particularly the microcontroller 29 and DSP 28 in a serial stream, descrambles the data, and assembles it into 8-bit bytes. The controller 10 then stores the data into the DRAM buffer 50. The error correction and detection operations performed by the ECC 40 and EDC CRC 42 on each sector of data are managed by the DRAM controller 38, which insures, through the direction of the host interface or control 44, that a sector of data is being corrected while the transfer of previously corrected sectors of data is occurring in real-time and without interrupting the flow of data from the drive controller 10 to the IDE bus 16.

'715 patent, col. 7, ll. 15-26. In other words, immediately after mentioning that CD-ROM data is normally read from the disk as a serial stream, assembled into 8-bit bytes, and stored in a RAM buffer, the written description acknowledges that error correction functions (abbreviated as "ECC" in the written description) and error detection functions (abbreviated as "EDC" in the written description), in the context of CD-ROM technology, operate on a sector-by-sector basis. Id. at ll. 19-22. Thus, the claim language and the written description both describe a straightforward, sector-by-sector, sequential "assembly line" process. Specifically, the written description states that the "assembled data" (i.e., a Sector of data) is first processed by the "error correction circuitry." When this process is completed, the "cyclic redundancy checker" processes the output of the error correction circuitry and produces "corrected data."

Oak argues that the Commission's interpretation of "said assembled data" was "misguided from the outset." Oak's view is that "according to the specification, 'assembled data' is simply another term for CD-ROM data that is sent from the compact-disc drive's electronics to the controller serially (i.e. one bit at a time) and organized into 8-bit bytes, not an entire 16,000 bit

sector of data." (emphasis Oak's). In other words, Oak focuses on the first of the two steps in the data assembly process (i.e., converting a serial bit stream into a stream of 8-bit bytes), and ignores the second step (i.e., grouping a specified number of bytes into a Sector of data).

Based on the intrinsic record, support for the Commission's interpretation of "said assembled data" is overwhelming. First, the Yellow Book leaves no doubt that both error correction and error detection are to be performed on a sector-by-sector basis, and Oak readily admits that "Oak's patent contemplates Yellow Book compliance." Ordinarily skilled artisans would know that not every byte of a Sector is used for purposes of either error correction or error detection. Specifically, the Yellow Book plainly specifies that Reed-Solomon error correction operates on bytes 12 through 2075 of each Sector, while CRC error detection operates on bytes 0 through 2063.

Oak attempts to argue that interpreting "said assembled data" to refer to an "entire sector of data as a unit" would create "insurmountable" problems, because there are actually some bytes in each Sector that are not involved in the error correction or error detection operations at all. This argument has no merit, because it incorrectly assumes that ordinarily skilled artisans will not be able to select the appropriate bytes in the Sector for each of the two operations. Indeed, we believe that it is Oak's interpretation of "said assembled data" that presents insurmountable problems. Oak does not attempt to explain how error correction and detection, as defined in the Yellow Book and claimed in the '715 patent, could be performed on any grouping of data smaller than a Sector.

To support its position that "said assembled data" does not refer to a Sector, Oak relies solely on following portion of the written description:

> [T]he drive controller 10 accepts digital data from the CD drive's electronics 12, particularly the microcontroller 29 and DSP 28 in a serial stream, descrambles the data, and assembles it into 8-bit bytes. The controller 10 then stores the data into the DRAM buffer 50.

'715 patent, col. 7, ll. 15-19. From Oak's perspective, this passage is appealing because it does not specify exactly how much data is being stored in the DRAM ("dynamic random access memory") buffer. According to Oak's view, therefore, there is no legally valid reason to narrow the meaning of the claimed term "said assembled data" to any particular size, much less to an entire Sector of data.

In fact, the written description of the '715 patent itself describes how Sectors of data compliant with the Yellow Book can be broken up into their constituent parts and stored in RAM in a way that is conducive to sector-by-sector error correction and detection. The written description makes it clear that Sectors are read out of the CD-ROM disk, one Sector at a time, and that the data stored in the DRAM buffer each time a Sector is read takes up exactly 2048 bytes, an amount corresponding to the User Data in the Sector:

> FIG. 19 and FIG. 20 are ECC block pointer/write address counters. PTL and PTH form a pointer used by the ECC logic, and contain the 12 least significant address bits of the first header byte of the CD-ROM block that is being corrected. Due to the DRAM page organization of one embodiment of the controller, the value of PTH,PTL will always be 00,00h, making it unnecessary to read or write PTL or PTH. The starting location of each block is controlled by write block counter registers WBKL and WBKH (28h and 29h). Error correction is processed on the block before that indicated in the write block counter (WBKH,WBKL-1). The controller organizes the DRAM into 2048-byte pages, allowing PTL and PTH to remain unchanged. PTL and PTH are undefined following hardware reset or firmware reset.

'715 patent, col. 12, ll. 1-14 (emphasis supplied). In other words, in the only embodiment described in the '715 patent, there is a DRAM buffer for storing CD-ROM data that is organized into "pages" of memory, with each page containing exactly 2048 bytes. As mentioned earlier, the Yellow Book specifies that the User Data field in each Sector of data is exactly 2048 bytes long (at least in Sector Mode 01, which is the only relevant operating mode in this case). Lest there be any doubt about what is being stored in each 2048-byte DRAM buffer page, the '715 patent explains that "[t]he microcontroller writes the starting address that corresponds to the required

starting point in the CD-ROM block," and that "[t]he first byte of User Data is located at address 00h." '715 patent, col. 11, ll. 27-28; Id. at ll. 31-32.

In other words, the disclosed controller locates the beginning of the 2048-byte User Data field in each Sector of data based on its knowledge of Sector organization as specified by the Yellow Book, and lines up the data so that the User Data is stored starting at the first memory location in one of the 2048-byte pages of memory in the DRAM buffer. As each new Sector is read from the CD-ROM disk, a new page in the DRAM buffer is used to store the User Data in that Sector, and a set of "pointers" (i.e., high-byte pointer PTH and low-byte pointer PTL) is used to keep track of the particular page in the DRAM buffer currently being operated on. '715 patent, col. 12, ll. 2-5 ("PTL and PTH form a pointer used by the ECC [error correction code circuitry], and contain the 12 least significant address bits of the first header byte of the CD-ROM block that is being corrected.").

In short, we must reject Oak's allegation that "there is no support for [the Commission's interpretation of 'said assembled data'] in the '715 patent or prosecution history."

B

This brings us to the next claim interpretation dispute in this case: the significance of the word "after" in the phrase "a cyclic redundancy checker for detecting errors in said assembled data after correction of said data by said correction circuitry." As our sequential view of the claim language would indicate, we agree with the Commission, which found that the device claimed in the '715 patent first performs error correction on an entire Sector of data, and then performs error detection with a cyclic redundancy checker on the entire corrected Sector of data. Referring to an embodiment of the invention, the written description states as follows:

> The error correction circuitry would first perform Reed-Solomon error correction on each block of data. . . . Then, a cyclic redundancy check of the corrected data would be performed.

'715 patent, col. 6, ll. 30-39. Like the language of the claim, this passage demonstrates that the data error detection and correction circuitry first performs Reed-Solomon error correction on an entire block or Sector of CD-ROM data, and that after this first operation is complete, the error detection circuitry then performs a cyclic redundancy check on the output of the error correction operation.

As mentioned earlier, according to the Yellow Book, "P-codewords" and "Q-codewords" are associated with Reed-Solomon error correction, while the "EDC-codeword" is associated with error detection using a cyclic redundancy checker. With this in mind, the written description goes on to confirm the exact order of operations in the only embodiment disclosed in the '715 patent:

> E01RQ-bit 5-Error Detect and Correct Request "1" enables the error correction and detection (ECC and EDC) logic to process the following CD-ROM blocks, according to the settings of QRQ and PRQ. "0" disables the ECC and EDC logic. Changes to E01RQ control the CD-ROM blocks following the next data sync. If both QRQ and PRQ are enabled, the ECC/EDC sequence is Q-codewords, P-codewords, EDC-codeword. If QRQ is enabled but PRQ is disabled, the sequence is Q-codeword, EDC-codeword. If QRQ is disabled but PRQ is enabled, the sequence is P-codeword, EDC-codeword. If both QRQ and PRQ are disabled, only the EDC-codeword is checked. Normally, QRQ and PRQ are enabled whenever E01RQ is enabled in order to provide maximum correction capability.

'715 patent, col. 12, ll. 44-55 (emphasis supplied). As the above passage plainly indicates, the only embodiment described in the '715 patent always performs error correction before performing CRC error detection. There is no mention in the '715 patent of any embodiments where the sequence of operations is reversed, or where error detection begins before error correction has been completed. As the above passage indicates, the only variations mentioned in the '715 patent simply describe the possibility of eliminating some or all of the error correction steps. However, the embodiment where "both QRQ and PRQ are disabled" (i.e., where error correction is completely disabled) is inconsistent with the plain language of the asserted claims, which require that error correction take place, and that it be performed before CRC error detection.

Oak argues that reliance on the written description amounts to an impermissible

importation of limitations from the preferred embodiment. We disagree. The sequential limitation is imposed by the claim language itself, and the written description simply confirms this understanding. There is no discussion anywhere in the intrinsic record of embodiments of "error detection and correction means" which do not operate in a straightforward sequential manner. More importantly, even if such a disclosure existed, these embodiments would not be covered by the language selected by the claim drafter. In Oak's own words: "Specifications teach. Claims claim." See Texas Instruments Inc. v. United States Int'l Trade Comm'n, 988 F.2d 1165, 1171, 26 USPQ2d 1018, 1023 (Fed. Cir 1993) ("[T]o construe the claims in the manner suggested [by the patentee] would read an express limitation out of the claims. This we will not do because '[c]ourts can neither broaden nor narrow claims to give the patentee something different than what he has set forth.'" (quoting Autogiro Co. of Am. v. United States, 384 F.2d 391, 396, 155 USPQ 697, 701 (Ct. Cl. 1967))).

C

The final claim interpretation issue in this case concerns the claimed term "cyclic redundancy checker." On appeal, Oak contends that the term simply refers to "any circuitry that performs a cyclic redundancy check." Intervenors align themselves with the Commission's interpretation: "The cyclic redundancy checker is hardware, commonly available in June 1994, that performs the division of a CRC generator binary polynomial into a 16,000-bit EDC code word to produce a CRC remainder."

The '715 patent document does not provide much guidance on the meaning of "cyclic redundancy checker," and only states that "[t]hese ECC and EDC-CRC circuits are commonly available as hardware used in many other applications." '715 patent, col. 6, ll. 41-43. However, based on the correct interpretation of "said assembled data" and "after," we know that only those "cyclic redundancy checkers" which operate on an entire Sector of data once the Sector of data has been processed by the "error correction circuitry" are included within the scope of the

asserted claims.

Our review of the record indicates that several relevant facts are undisputed. First, there is no dispute that the common hardware implementation of a "cyclic redundancy checker" as of 1994 was a structure called a "linear feedback shift register," which was well known to ordinarily skilled artisans. Also, it is undisputed that as of 1994, certain "special case" variations of cyclic redundancy check operations were known in the art, which did not use the common linear feedback shift register. However, there is no evidence in the record that any of these alternative cyclic redundancy check operations were ever implemented in hardware. Moreover, as the Commission correctly pointed out, even the references relied upon by Oak to demonstrate the existence of these alternative embodiments explicitly admit that the "normal" way of performing a cyclic redundancy check operation is by using a linear feedback shift register.[5]

Most importantly, the definition of "cyclic redundancy checker" in this case is actually undisputed. The parties agree that the correct definition is set forth in the 1976 edition of the Encyclopedia of Computer Science:

> [In cyclic redundancy checking], all the characters in a message block are treated as a serial string of bits representing a binary number. This number is then divided modulo 2 by a predetermined binary number and the remainder of this division is appended to the block of characters as a cyclic redundancy check (CRC) character.

Oak attacks this reference on the basis that it illustrates a linear feedback shift register structure as the preferred embodiment of performing a cyclic redundancy check operation. However, Oak explicitly agrees with the Encyclopedia 's mathematical definition. The Commission's claim interpretation of "cyclic redundancy checker" is consistent with this definition, and we therefore affirm it.

We also note once again that--in this case--not every structure that literally fits the definition of "cyclic redundancy checker" set forth in the Encyclopedia is covered by the claim. Only those cyclic redundancy checkers which meet the additional interactive limitations explicitly imposed by

the claim language are within the properly construed scope of the claim. Specifically, the only cyclic redundancy checkers covered by the claim are those which operate on "said assembled data" (i.e., on a Sector's worth of data) "after" all such data has been processed by the "error correction circuitry," according to the manner in which we construe those terms herein.

Oak's broad interpretation that a cyclic redundancy checker is any circuitry that performs a cyclic redundancy check must be rejected. As we have already discussed, the claim language itself imposes significant restrictions on the "cyclic redundancy checker." Specifically, due to the "said assembled data" and "after" limitations in the claim which we have already resolved in favor of Intervenors and the Commission, the only cyclic redundancy checkers which can possibly be covered by the claim language--as a matter of simple logic--are those which operate on an entire Sector of data after the Sector of data has already been processed by error correction circuitry.

VII

With the proper interpretation of the disputed claim limitations in hand, we turn to the question of whether the Commission correctly concluded that the accused devices do not infringe the asserted claims of the '715 patent. The Commission made the following factual findings with respect to the accused MediaTek devices, which we conclude are supported by substantial evidence:

> As to the accused product, the MediaTek device first performs an error detection by a cyclic redundancy check on the entire CD-ROM block of data (generating an original CRC remainder), followed by Reed-Solomon error correction, followed by a second error detection. This second error detection is an update to the original CRC remainder with 20 bits of error location and error pattern data from the Reed-Solomon error correction operation. In this second error detection operation, the original CRC remainder is decremented until it equals zero, indicating that all errors have now been corrected.

This characterization of the accused MediaTek devices is consistent with the description of the devices as set forth in MediaTek's United States Patent No. 6,003,151 ("MediaTek's '151 patent").

There is no dispute that MediaTek's '151 patent accurately describes the operation of the accused devices in relevant part.[6]

In simple terms, the relevant portions of the accused MediaTek devices may be characterized as performing a three-step process. First, a cyclic redundancy check is performed on an entire Sector of CD-ROM data. Next, Reed-Solomon error correction operates on the output of the cyclic redundancy checker. Finally, a second error detection step is performed to account for the fact that the error correction and error detection steps are performed in the reverse order from that specified in the Yellow Book standard.

A

Given our agreement with the Commission's construction of the "data error detection and correction means," we conclude that substantial evidence supports the Commission's factual finding that MediaTek's devices do not literally infringe the asserted claims of the '715 patent. Specifically, substantial evidence supports the Commission's conclusion that the accused MediaTek devices do not meet the claim limitation which recites "a cyclic redundancy checker for detecting errors in said assembled data after correction of said data by said correction circuitry."

To be sure, the accused MediaTek devices admittedly contain a "cyclic redundancy checker." This is not surprising, because such a structure, or at least its functional equivalent, is required by the Yellow Book. However, the structure called a "cyclic redundancy checker" in the accused MediaTek device does not operate on "said assembled data after correction of said data by said correction circuitry" in accordance with the claim interpretation we set forth herein. Instead, there is no dispute that it operates on "said assembled data" before correction.

The parties also agree that there is another structure in the accused devices (the so-called Error Detection Processor, or "EDP"), which is "for" error detection, and which can be characterized, for the sake of argument, as performing a form of error detection after error correction. However, this

structure is not a "cyclic redundancy checker" as the term is interpreted herein, not because it has a different name ("EDP" versus "CRC"), but because substantial evidence supports the Commission's factual finding that the operation performed by MediaTek's EDP does not meet the definition of "cyclic redundancy checker" set forth in the Encyclopedia, and because the EDP does not operate on "said assembled data [i.e., on an entire Sector of CD-ROM data] after correction of said data by said correction circuitry [i.e., the error detection operation does not commence until after the error correction operation has completed]."

B

We also conclude that substantial evidence supports the Commission's factual finding that the accused devices do not infringe the asserted claims of the '715 patent under the doctrine of equivalents. To infringe under the doctrine of equivalents, the differences between MediaTek's devices and the claimed device must be "insubstantial," and the familiar three-part function/way/result test can be helpful in making that determination. Warner-Jenkins Co. v. Hilton Davis Chem. Co., 520 U.S. 17, 40-41, 41 USPQ2d 1865, 1875 (1997); Dawn Equip. Co. v. Kentucky Farms Inc., 140 F.3d 1009, 1015, 46 USPQ2d 1109, 1113 (Fed. Cir. 1998) (infringement may occur under doctrine of equivalents only if there are "insubstantial differences" between claimed invention and accused devices).

The Commission correctly identified several substantial differences between MediaTek's device and the CD-ROM controller claimed in the '715 patent, each of which relate to the way that the accused devices operate in comparison to the asserted claims. First, substantial evidence supports the Commission's finding that there are substantial differences between the binary mathematics performed by the accused devices and the mathematics in the claimed controller. The claimed controller uses the generator polynomial to perform a long division operation on the entire EDC codeword. In contrast, MediaTek's device divides the error location and pattern data obtained from each corrected P- or Q-codeword by the generator polynomial, and adds each

result to the initial EDC remainder obtained from the original error detection operation before error correction.

Second, substantial evidence supports the Commission's finding that the relevant circuitry in the devices is substantially different. The claimed controller as properly construed requires two circuits: Reed-Solomon error correction circuitry, followed by a cyclic redundancy checker. Although MediaTek's accused device contains these two circuits, the cyclic redundancy checker in the MediaTek device is not used for error detection on a corrected Sector of CD-ROM data, and the cyclic redundancy checker precedes, rather than follows, the Reed-Solomon error correction circuitry. To account for this reversal in the order of operations, the accused MediaTek device includes a circuit not contemplated by the '715 patent which uses update information from the Reed-Solomon decoder and updates the EDC remainder to remove the effect of the corrected error.

The third substantial difference correctly noted by the Commission is that the data processed by the devices is different. The claimed controller first performs error correction on an entire Sector of data, then detects errors in the corrected Sector of data. By contrast, MediaTek's device first detects errors in the uncorrected Sector of data to get an initial 32-bit EDC remainder, and then performs Reed-Solomon error correction while simultaneously using 20 bits of error pattern and location information from the error correction process to execute multiple updates to the 32-bit EDC remainder.

Fourth, substantial evidence supports the Commission's finding that the interrelationship between the error correction and detection operations in the respective devices is substantially different. The claimed controller performs a cyclic redundancy check after error correction. By contrast, MediaTek's device performs a cyclic redundancy check before error correction, and then updates the EDC remainder during and after error correction in a way that is dependent upon data obtained from the error correction process.

VIII

For the preceding reasons, the final determination of the United States International Trade Commission is affirmed.

AFFIRMED

---

[1] All statutory references are to the 1994 version of the United States Code, as modified by Supplement IV of 1998.

[2] The Yellow Book consistently uses the term "Sector," while the '715 patent uses the terms "block" and "Sector" interchangeably. There is no disagreement that these two terms refer to the same thing in the context of the '715 patent.

[3] As is commonly known in the art, a group of eight "bits" comprises one "byte." Each bit represents a single digital value, either 1 or 0. Thus, twelve bytes of data are represented by ninety-six bits. As indicated in the written description of the '715 patent, data is read out of a CD-ROM disk serially (i.e., one bit at a time). '715 patent, col. 7, ll. 15-17. However, data is normally stored in the memory of a CD-ROM drive and in a host computer in groups of bytes. '715 patent, col. 7, l. 18.

[4] Oak also asserted claims 2, 3, 4, 5, and 9, all of which depend from claim 1. Because we affirm the Commission's conclusion that claim 1 is not infringed, we need not address the dependent claims separately. See Jeneric/Pentron, Inc. v. Dillon Co., Inc., 205 F.3d 1377, 1383, 54 USPQ2d 1086, 1090 (Fed. Cir. 2000) (stating that it is a fundamental principle of patent law that dependent claims cannot be found infringed unless the claims from which they depend have been found to have been infringed).

[5] These references include (1) United States Patent No. 5,027,357; (2) D.R. Irvin, "Preserving the Integrity of Cyclic-redundancy Checks when Protected Text is Intentionally Altered," 33 IBM J. Res. Dev. (Nov. 1989); (3) C.L. Chen, "High-Speed Cyclic Redundancy Checking Scheme for Error Correcting Codes," 22 IBM Tech. Disclosure Bull. (Nov. 1979); and (4) M. Gutman, "A Method for Updating a Cyclic Redundancy Code," 40 IEEE Trans. on Comm. (June 1992).

[6] The '151 patent issued on December 14, 1999, while the Commission issued its final opinion in this case two months earlier, on October 20, 1999. A copy of the patent application which matured into the '151 patent is in the record, along with a Notice of Allowance dated March 29, 1999.