United States Court of Appeals for the Federal Circuit

00-1226, -1250

TECHSEARCH L.L.C.,

Plaintiff-Appellant,

v.

INTEL CORPORATION,

Defendant-Cross Appellant.

John C. Janka, Niro, Scavone, Haller & Niro, of Chicago, Illinois, argued for plaintiff-appellant. With him on the brief were Raymond P. Niro, and Robert P. Greenspoon. Of counsel was Joseph N. Hosteny.

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Appealed from: United States District Court for the Northern District of California

Senior Judge William H. Orrick

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DECIDED: April 11, 2002

Before NEWMAN, GAJARSA, and DYK, Circuit Judges.

Opinion for the court filed by Circuit Judge GAJARSA. Concurring opinion filed by Circuit Judge Dyk.

GAJARSA, Circuit Judge.

This is a patent infringement case dealing with complex computer microprocessor technology. After extensive submissions by the parties and numerous preliminary findings by the United States District Court for the Northern District of California, the court issued summary judgment of noninfringement of TechSearch's U.S. Pat. No. 5,574,927 ("the '927 patent"), issued to Henry L. Scantlin, in favor of Intel Corp. ("Intel") and dismissed as moot Intel's counterclaim for declaratory relief. TechSearch, L.L.C. v. Intel Corp., No. 98-CV-03484,

slip op. at 17-18 (N.D. Cal. January 31, 2000) (memorandum decision and order granting summary judgment) ("TechSearch-Judgment"). TechSearch L.L.C. ("TechSearch") appeals from the grant of summary judgment. For the reasons discussed below, we affirm the judgment of the district court.

BACKGROUND

In the early 1990's, International Meta Systems, Inc. ("IMS") sought to develop a microprocessor known as the "IMS 3250" that could "emulate," or behave like, popular microprocessors such as the Intel 80X86 and the Motorola 680X0. On March 25, 1994, IMS filed a patent application encompassing the IMS 3250 processor. The application issued as the '927 patent on November 12, 1996. The inventor, Henry L. Scantlin, assigned all rights in the '927 patent to IMS, his employer.

The patent is entitled "RISC Architecture Computer Configured for Emulation of the Instruction Set of a Target Computer." The acronym RISC stands for "Reduced Instruction Set Computer." The patent discloses a RISC architecture computer microprocessor that can emulate the architectural behavior of another microprocessor. The claimed RISC processor and emulation technique permit use of existing software written for a target computer, even if that computer is a Complex Instruction Set Computer or "CISC" microprocessor, while retaining the benefits inherent in RISC processors. '927 patent, col. 2, ll. 52-57.

CISC architecture requires an extensive fixed set of, as the name suggests, complex instructions that are either hardwired or microprogrammed into the logic of a single microprocessor. '927 patent, col. 1, ll. 54-60. A RISC architecture design has certain design benefits compared to CISC microprocessor designs because a RISC architecture reduces the complexity of the chip through the use of microinstructions that perform a limited

subfunction of a CISC instruction within a single clock cycle. '927 patent, col. 1, ll. 60-68. Thus, RISC architecture results in a microprocessor chip having fewer gates, using less power, and executing instructions significantly faster than a typical CISC microprocessor. '927 patent, col. 2, ll. 1-11.

Claims 1, 4 and 14 are the independent claims of the '927 patent, and read as follows:

1. A method for emulating the instruction set of a target computer on a RISC architecture computer, comprising the steps of:

1) fetching a target instruction of a format compatible with the instruction set of the target computer;
2) parsing and decoding said instruction into fields designating an opcode and operands;
3) converting said opcode into an address pointing to a sequence of one or more microcoded instructions;
4) decoding said microcoded instruction into a LHS instruction having fields essentially compatible with a RISC architecture and a RHS instruction having fields to select a plurality of indirect registers pointing to emulated registers;
5) processing said emulated registers with an arithmetic logic unit;
6) calculating a condition code as a function of the operation of said arithmetic logic unit and a selection field within said microcoded instruction;
7) storing a result of said processing by said arithmetic logic unit;
8) storing a result of said condition code calculation; and
9) repeating steps 4-8 with a next microcoded instruction until an end of said microcoded sequence is encountered and then continuing at step 1 with a next target instruction.

'927 patent, col. 52, l. 64 to col. 53, l. 23.

4. A RISC architecture computer having a native instruction width of N bits configured for emulating target instructions from the instruction set of a target computer, comprising:

a plurality of emulation registers capable of corresponding to registers in the target computer and having data widths greater than or equal to the data widths of the registers in the target computer;
a plurality of indirect registers for selection of said emulation registers;
parsing means to extract a plurality of data fields from a target instruction, at least one said field[s] including an opcode;
dispatching means using said opcode to direct the RISC architecture computer to select at least one M+N bit expanded RISC instruction from a microcode

memory;

an expanded instruction decoder for using said M bits from each said expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer, wherein said M bits define fields, said fields comprising a width field for designating the data width of said emulation registers and the data width of an arithmetic function, an indirect register field for designating said indirect registers, and a condition code field for designating a condition code emulation mode; and

condition code calculation means for determining the condition code for an arithmetic function according to said condition code field.

'927 patent, col. 53, ll. 33-61.

14. A RISC architecture computer having a native instruction width of N bits configured for emulating target instructions from the instruction set of a target computer, comprising:

a plurality of emulation registers capable of corresponding to registers in the target computer and having data widths greater than or equal to the data widths of the registers in the target computer;

a plurality of indirect registers for selection of said emulation registers;

parsing means to extract a plurality of data fields from a target instruction, at least one said field including an opcode;

dispatching means using said opcode to direct the RISC architecture computer to select at least one M+N bit expanded RISC instruction from a microcode memory;

an expanded instruction decoder for using said M bits from each said expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer; and

condition code calculation means for determining the condition code for an arithmetic function in accordance with the target computer.

'927 patent, col. 54, ll. 19-43.

As claimed, the invention includes a system or method for using a RISC architecture computer having a native instruction set including, inter alia, instructions of a width of N bits configured for emulating instructions from the instruction set of a target computer; a plurality of emulation registers for simulating registers of the target computer; a plurality of indirect registers for selecting the emulation registers; structure for extracting the data fields of a target instruction, including an opcode field; structure for using the opcode to direct the RISC

architecture computer to select at least one M+N bit expanded RISC instruction from memory; an expanded instruction decoder for using M bits from the expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer; a condition code field for designating a condition code emulation mode; and structure for determining the condition code for an arithmetic function according to a condition code field.

Intel's x86 CISC microprocessors share instructions, adding new instructions to those which comprise the instruction set of the previously issued microprocessor. In other words, with the introduction of each new member of the Intel x86 family of microprocessors, new instructions are added to the CISC x86 instruction set of the previous version of the microprocessors. Thus, the P6 instruction set includes instructions unique to that version of the processors, as well as those used by the P5 microprocessor. Like the P6, the P5 instruction set includes all of the instructions found in the instruction set of the 486 microprocessor, as well as each additional instruction unique to the P5. Thus, each new processor executes all of the instructions of its predecessor, without modification, as well as the new instructions unique to that device.

After working on several versions of the 3250, IMS's attempts to produce the microprocessor commercially failed. TechSearch purchased the '927 patent as an asset in the IMS bankruptcy proceeding. Subsequently, TechSearch filed a complaint against Intel in September 1998 alleging that Intel's P6 line of microprocessors infringed the claims of the '927 patent.

The district court held a Markman hearing in August 1999 and issued a Memorandum Decision and Order on November 1, 1999. Recognizing that one skilled in the art would typically identify a computer as RISC- or CISC-based upon its published instructions rather

than the microinstructions, the court concluded that, in the context of the patented invention, the classification of the microprocessor was properly assessed from the microcode level. The court concluded that the claims themselves confirm that it is the microcode, not the machine code (or "macro" level), that is relevant to whether a microprocessor is a CISC or RISC microprocessor, and is therefore covered by the patent's claims.

With regard to the term "emulation," the district court referenced the written description that defines the term as "a process in which one computer X behaves identically to another computer Y, as X executes the instructions of Y, where the internal architectures of computers X and Y are different." '927 patent, col. 2, ll. 30-33. Concerning the "LHS" (left-hand side) and "RHS" (right-hand side) of the coded instruction recited in claim 1, the court determined that those terms refer to the native instruction of a RISC microprocessor configured for emulation of a target computer's microprocessor. Thus, the court concluded that the LHS and RHS are two subdivisions of a single RISC microinstruction.

Independent claims 4 and 14 refer to the coded instruction as an M+N bit expanded RISC instruction. The court concluded that the M+N bit expanded RISC instruction is composed of N bits corresponding to the native instruction, or the instruction of the host microprocessor's instruction set used when the microprocessor is not in emulation mode, and M bits "which redefines the N bits" in the expanded RISC instruction, thereby enabling the host microprocessor to emulate a target computer.

The district court defined the term "condition code" as a summary of the effects of recently emulated target instructions. Although worded differently, the district court noted that the parties agreed that each independent claim requires a selection field within the microinstruction identifying the particular target computer being emulated so that the condition

code matches the operation that would have been performed had the same calculation been performed within the target computer. Finally, the district court interpreted the "expanded instruction decoder" as simply a decoder used in the execution of an M+N bit RISC instruction.

Subsequently, the parties filed cross-motions for summary judgment. On January 31, 2000, the district court issued a Memorandum Decision and Order granting Intel's motion for summary judgment of noninfringement. The district court concluded that to prove infringement of claim 1, TechSearch must show that the P6 microprocessors have "a plurality of indirect registers pointing to emulated registers," and that the accused products process the emulated registers with an arithmetic logic unit. TechSearch had maintained that the macro alias register file ("MAR") found in the P6 corresponds to the claimed indirect registers. The court determined that, even assuming that to be true, there is no dispute that the MAR does not point to emulated registers as required and that there are no registers in the P6 that are both pointed to by the indirect registers and processed with an arithmetic logic unit ("ALU"). Specifically, the court noted that the MAR does not point to any registers or to anything processed by the ALU and that the MAR are logical registers, which are not actual registers but merely references. Nor was the court persuaded that TechSearch had established that there are any emulated registers in the accused device. Therefore, the court determined that claim 1 is not infringed literally or under the doctrine of equivalents.

The court further concluded that the P6 microprocessors are not "configured to emulate the instruction set of a target computer" in accordance with claims 1, 4 and 14. The district court found that "it is beyond dispute that the P6 microprocessors are not configured to emulate in the manner claimed," TechSearch-Judgment, slip op. at 9, and therefore do no

infringe. The court noted that "[t]he 'patent specification makes clear that its emulation scheme entails modifying preexisting native instructions of a RISC architecture computer'" such that when the computer is emulating, "the native instructions are redefined by M bits in order to form an M+N bit expanded instruction that enables the host system to emulate the target system." Id. at 9-10. Accordingly, the court determined that to infringe claims 4 and 14, TechSearch must prove that the P6 microprocessor has both a native instruction of N bits and an expanded RISC instruction comprised of M+N bits to be used when the computer is emulating, or their equivalents.

The court determined that no reasonable jury could find that the P6 microprocessors have microinstructions comprised only of N bit instructions when operating in the native mode of the host processor, i.e., when not emulating, and microinstructions comprised of an M+N bit RISC instruction when emulating. The court noted that the format of the instructions that the P6 microprocessors use when executing an instruction from an "earlier version" of Intel's x86 instruction set are indistinguishable from the format of the instructions originating with the "current version." The court concluded that even were the testimony of TechSearch's expert to be accepted, asserting that the P6 microprocessors emulate, TechSearch has not shown infringement because it is "beyond question" that the P6 runs only one instruction set. Therefore, the court concluded that the P6 microprocessor does not emulate in the manner required by claims 4 and 14.

The district court further determined, in the alternative, that the P6 products do not have an "expanded instruction decoder" using M bits from each expanded RISC instruction to "redefine" the RISC architecture computer in terms of the target computer during emulation.

Thus, the court concluded that it is "beyond cavil" that the P6 microprocessor does not infringe.

The court stated that to prove infringement of claims 4 and 14 TechSearch must prove that: (1) the P6 microprocessor has an expanded instruction decoder; and (2) that the expanded instruction decoder uses M bits from each expanded RISC instruction to "redefine" the RISC architecture computer in terms of the target computer during emulation. The district court concluded that the P6 microprocessor does not have a decoder that can decode expanded instructions.

The court concluded that the P6 "alias multiplexer," alleged by TechSearch to correspond to the claimed decoder, differs materially from the decoder contemplated by the patent. Specifically, the court noted that the claimed invention translates the instructions into a form for processing by the ALU in a manner involving considerable interaction between the various elements of the microinstruction. Contrarily, the inputs of the multiplexer are simply routed to its outputs. The court noted that one of ordinary skill in the art would know that decoders and multiplexers perform substantially different functions and consist of substantially different structure.

The court noted that TechSearch's expert, Dr. Hoevel, did not contend that the multiplexer in the P6 microprocessor operates as a decoder and did not dispute that the function of multiplexing differs from the decoding claimed. While the court concluded that the claimed decoder combines the input signals to produce outputs that cause selection of the direct, indirect or emulation registers, it found that TechSearch did not dispute that the P6 microprocessor's alias multiplexer architecture does not combine input signals, but simply steers each signal to the appropriate output field. The court, therefore, found Dr. Hoevel's

testimony, and TechSearch's arguments based thereon, insufficient to avoid a grant of summary judgment of noninfringment.

Similarly, the court determined that TechSearch had failed to create a triable issue of fact by arguing that a multiplexer is capable of acting as a decoder, noting that TechSearch failed to provide evidence to explain how the multiplexer of the P6 functions in the manner describing the claimed decoder. The district court further concluded that Hoevel's conclusory allegations failed to raise a genuine issue of material fact.

Finally, noting that the claimed instruction decoder operates to "redefine" the microprocessor when emulating and that no redefinition of instructions is performed by the "decoder" in the P6 microprocessor, the court concluded that no part of the P6 can be found to infringe the instruction decoder recited in claims 4 and 14. Specifically, the court concluded that the P6 microprocessor does not use an additional M bits to redefine N bits of the instruction when "emulating." Although Hoevel asserted that the microinstructions found in P6 microprocessors, known as "Cuops," contain fields for performing register indirection, the court noted that in the P6 microprocessors those instructions are always the same size and use all of its bits, regardless of the version of microprocessor with which they were first introduced. Thus, the court determined that the Cuops microinstruction, and thus the P6 microprocessor instruction set, does not redefine or expand the microinstructions as claimed. Therefore, the court concluded that no reasonable jury could find that the Cuops are redefined "in any way."

In a Memorandum Decision and Order dated November 9, 1999, issued after the Markman hearing but before the grant of summary judgment, the district court informed the parties that it had decided to appoint its own "technical advisor." The court recognized that

such appointments should be reserved for the exceptional case, but deemed it appropriate in this particular case because infringement would be "a highly technical [issue] far beyond the boundaries of the normal questions of fact and law with which judges routinely grapple." The court noted that technical advisors "are not witnesses, and may not contribute evidence." As such, the court concluded that a technical advisor is not subject to the requirements set forth in Rule 706 of the Federal Rules of Evidence regulating the appointment of expert witnesses. The district court further explained that "[a] judge may not appoint a technical advisor to brief him on legal issues, or to find facts outside the record of the case; the advisor's role is to acquaint the judge with the jargon and theory disclosed by the testimony and to help think through certain of the critical technical problems." TechSearch, L.L.C. v. Intel Corp., No. 98-CV-03484, slip op. at 4 (N.D. Cal. November 9, 1999) (memorandum decision and order appointing technical advisor) ("TechSearch-Appointment"). Anticipating the difficulty in evaluating the "extremely complicated" technical evidence submitted by the parties involving "highly technical electrical engineering and microprocessor design," which the district court had to process to formulate its claim construction, the court retained the technical advisor to assist with evaluation of the technical matters before it when resolving pretrial motions, as well as during trial. Specifically, the court recognized that it would be "faced with expert testimony, scientific articles, and patents" the technology of which the court "urgently require[d]" the assistance of a technical advisor to understand. As an example, the court stated that evaluation of the prior art required consideration of technical concepts beyond normal questions of fact regularly addressed by the court.

The court determined that its technical expert, Dr. Hearn, was a neutral third party, and explained its reasoning for that determination in its memorandum decision.

TechSearch-Appointment, slip op. at 5-7. The court reiterated that Dr. Hearn had "agreed that he will not engage in any independent investigation of the underlying litigation, provide evidence to the Court, or contact any party or witness in this action." The court further agreed to identify any material relied upon by Dr. Hearn, other than that submitted by the parties or "those upon which a person versed in the relevant field of knowledge would be reasonably expected to rely." The court stated that Dr. Hearn would execute an affidavit indicating his understanding of that order before beginning his engagement, and would file an affidavit attesting to his compliance with its terms at the conclusion of his employment.

TechSearch appeals the district court's judgment. We have jurisdiction pursuant to 28 U.S.C. § 1295(a)(1).

STANDARD OF REVIEW

This court reviews a district court's grant of summary judgment without deference. Cortland Line Co. v. Orvis Co., 203 F.3d 1351, 1355, 53 USPQ2d 1734, 1746 (Fed. Cir. 2000). The moving party is entitled to summary judgment "if the pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law." Fed. R. Civ. P. 56(c). In reviewing the district court's grant of summary judgment, this court draws all reasonable inferences from the evidence in favor of the non-movant. Anderson v. Liberty Lobby, Inc., 477 U.S. 242, 255 (1986). Summary judgment is appropriate when it is apparent that only one conclusion as to infringement could be reached by a reasonable jury. ATD Corp. v. Lydall, Inc., 159 F.3d 534, 540, 48 USPQ2d 1321, 1324 (Fed. Cir. 1998). Summary judgment of noninfringement is also appropriate where the patent owner's proof is deficient in meeting an essential part of the legal standard

for infringement, because such failure will render all other facts immaterial. London v. Carson Pirie Scott & Co., 946 F.2d 1534, 1537, 20 USPQ2d 1456, 1458 (Fed. Cir. 1991).

A patent infringement analysis involves two steps: 1) claim construction; and 2) application of the properly construed claim to the accused product. Markman v. Westview Instruments, Inc., 52 F.3d 967, 976, 34 USPQ2d 1321, 1326 (Fed. Cir. 1995) (en banc), aff'd, 517 U.S. 370 (1996). The first step, claim construction, is a matter of law that this court reviews without deference. Cybor Corp. v. FAS Tech., Inc., 138 F.3d 1448, 1454, 46 USPQ2d 1169, 1172 (Fed. Cir. 1998) (en banc). Whether the accused device contains an element corresponding to each claim limitation or its equivalent is a question of fact, which, on summary judgment, is a question we review to determine whether a material factual issue remains genuinely in dispute. Roton Barrier, Inc. v. Stanley Works, 79 F.3d 1112, 1125, 37 USPQ2d 1816, 1826 (Fed. Cir. 1996).

DISCUSSION

I. Claim Construction

While the parties dispute the court's construction of many of the claim terms at issue before the district court, we address the construction of only those terms essential for disposition of this appeal.

The independent claims of the '927 patent recite a method or computer for "emulating" target instructions of the instruction set of a target computer using, inter alia, "emulation registers" capable of corresponding to registers in the target computer. The written description defines the term "emulation" generally as "a process in which one computer X behaves identically to another computer Y, as X executes the instructions of Y, where the

internal architectures of computers X and Y are different." '927 patent, col. 2, ll. 30-33. We adopt this construction and conclude that the district court correctly interpreted this term.

Claims 4 and 14 define the particular manner in which the claimed processor emulates. Specifically, both claims require a "M+N bit expanded RISC instruction" with N bits defining the "native instruction . . . configured for emulating target instructions from the instruction set of a target computer." Consistently, the claims require an expanded instruction decoder that uses "M bits from each said expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer." The written description of the '927 patent defines N bits of an expanded RISC instruction, also referred to as the LHS (left-hand side) of the instruction, as the number of bits of the instruction that the microprocessor uses "in its native mode." '927 patent, col. 5, ll. 1-2. With regard to the M bits of the expanded RISC instruction, also referred to as the RHS (right-hand side) of the instruction, the '927 patent states that "[c]ontained within the additional M bits [of the expanded RISC instruction] and used in conjunction with the N bits are directions on the use of resources within the RISC computer, peculiar to each emulated instruction." '927 patent, col. 5, ll. 6-9. The written description of the '927 patent explains that the M bits, or RHS, of the expanded RISC instruction are used "to redefine, during emulation of a target processor operation, the register data paths . . . of the LHS [or N bits of the expanded RISC instruction] to correspond to the target processor instruction being emulated, permitting the host processor to mirror, without physical changes, the target processor architecture being emulated." '927 patent, col. 8, ll. 31-37. Consistently, TechSearch's expert, Dr. Hoevel, recognizes that to emulate, "the host computer has to interpret and execute the target instruction set used in the target computer . . . and claims 1 through 3 of the '927 patent reveal the advantages of the special kind of emulation and

backwards compatibility found in the '927 patent."

We conclude, as the district court did, that the M+N bit expanded RISC instruction recited in claims 4 and 14 includes N bits corresponding to an instruction of the host microprocessor's instruction set, and M bits which work with the N bits to "redefine" or "translate" the expanded RISC instruction to "emulate" the instructions of the microprocessor of the target computer. We further conclude that the claimed "expanded instruction decoder" is a decoder that "redefines" or "translates" the native instruction identified as N bits of the expanded RISC instruction, using M bits of the expanded RISC instruction, thereby enabling the instruction set of the microprocessor of the computer to emulate the instructions of a target computer.

As noted, the '927 patent defines the LHS and RHS instructions recited in claim 1, as synonymous with the N bits and M bits of the expanded RISC instruction of claims 4 and 14. The '927 patent states, "[t]he native N bits are referred to as the LHS (left-hand side) of the instruction while the M bits are referred to as the RHS (right-hand side) of the instruction." '927 patent, col. 5, ll. 9-12. Consistent with the M+N bit expanded RISC instruction of claims 4 and 14, method claim 1 includes the step of "decoding said microcoded instruction into a LHS instruction having fields essentially compatible with a RISC architecture and a RHS instruction having fields to select a plurality of indirect registers pointing to emulated registers," and "processing said emulated registers with an arithmetic logic unit." For the reasons provided supra, we conclude that the claimed "decoding" step requires "redefining" or "translating" the native instruction, identified in claim 1 as LHS of the instruction, using the fields of the RHS of the instruction to emulate the instruction of a target computer.

II. Infringement

To support a summary judgment of noninfringement it must be shown that, on the correct claim construction, no reasonable jury could have found infringement on the undisputed facts or when all reasonable factual inferences are drawn in favor of the patentee. Network, LLC v. Centraal Corp., 242 F.3d 1347, 1351, 58 USPQ2d 1076, 1078 (Fed. Cir. 2001). Similarly, "[a]lthough equivalence is a factual matter normally reserved for a factfinder, the trial court should grant summary judgment in any case where no reasonable factfinder could find equivalence." Sage Prods. v. Devon Indus., Inc., 126 F.3d 1420, 1423, 44 USPQ2d 1103, 1106 (Fed. Cir. 1997).

An infringement analysis is "a two-step process in which we first determine the correct claim scope, and then compare the properly construed claim to the accused device to determine whether all of the claim limitations are present either literally or by a substantial equivalent." Renishaw PLC v. Marposs Societa' Per Azioni, 158 F.3d 1243, 1247-48, 48 USPQ2d 1117, 1120 (Fed. Cir. 1998). To establish literal infringement, all of the elements of the claim, as correctly construed, must be present in the accused system. See Cole v. Kimberly-Clark Corp., 102 F.3d at 524, 532, 41 USPQ2d 1001, 1007 (Fed. Cir. 1996).

"A party may not overcome a grant of summary judgment by merely offering conclusory statements." Moore U.S.A., Inc. v. Standard Register Co., 229 F.3d 1091, 1112, 56 USPQ2d 1225, 1240 (Fed. Cir. 2000). In Moore, the declarations offered by the patentee to carry its burden of proof of infringement were found insufficient. Moore's declarations alleged infringement with specific reference to the accused device. However, the Federal Circuit determined that the "allegations" contained therein were "entirely lacking in factual support." Id. This court similarly dismissed Moore's claim of infringement under the doctrine of equivalents,

finding "[t]he mere recital of the Graver Tank mantra that the accused device performs 'the same function, in the same way, to achieve the same result,' without more, does not create a genuine issue of material fact as to whether an accused device infringes by equivalents." Moore U.S.A., 229 F.3d at 113, 56 USPQ2d at 1240.

Accordingly, infringement must be shown literally or equivalently for each limitation; general assertions of facts, general denials, and conclusory statements are insufficient to shoulder the non-movant's burden. Johnston v. IVAC Corp., 885 F.2d 1574, 1578, 12 USPQ2d 1382, 1385 (Fed. Cir. 1989) (citing Chemical Eng'g v. Essef Indus., 795 F.2d 1565, 230 USPQ 385 (Fed. Cir. 1986)). Thus, the party opposing the motion for summary judgment of noninfringment must point to an evidentiary conflict created on the record, at least by a counter-statement of a fact set forth in detail in an affidavit by a knowledgeable affiant. Mere denials or conclusory statements are insufficient. Collins, Inc. v. N. Telecomm., Ltd., 216 F.3d 1042, 1046, 55 USPQ2d 1143, 1146 (Fed. Cir. 2000); Barmag Barmer Maschinenfabrik AG v. Murata Mach., Ltd., 731 F.2d 831, 836, 221 USPQ 561, 564 (Fed. Cir. 1984).

In Phillips Petroleum Co. v. Huntsman Polymers Corp., 157 F.3d 866, 48 USPQ2d 1161 (Fed. Cir. 1998), this court held that the patentee failed, through the conclusory statements of experts, to raise a genuine issue of material fact precluding summary judgment. 157 F.3d at 876, 48 USPQ2d at 1169-70. Rejecting Phillips' argument that the accused products contain block copolymers within the meaning of the claims, the court stated, "[w]e agree with the Special Master's conclusion that the expert declarations are wholly conclusory, devoid of facts upon which the affiant[s'] conclusions, as experts, were reached." Id. (quotation marks omitted). Thus, unsupported or conclusory averments are insufficient to avoid summary judgment where the moving party has met its initial burden. Celotex Corp. v. Catrett, 477 U.S.

317, 322-23 (1986); see also Schendel v. Curtis, 83 F.3d 1399, 1409, 38 USPQ2d 1743, 1752 (Fed. Cir. 1996).

In accordance with the limitations of claims 4 and 14, the claimed microprocessor executes N bit "native" instructions when not emulating, and also executes M+N bit expanded instructions in an emulating mode. M bits of the instruction "redefine" the N bits corresponding to the native instruction, to create an expanded instruction that emulates the instructions of a different microprocessor. The district court concluded that "it is beyond dispute that the P6 microprocessors are not configured to emulate in the manner claimed and do not, therefore, infringe any one of the asserted claims." The court further concluded that "it is beyond question" that the P6 microprocessors do not have both a "native mode" using microinstructions of N bits only, and an emulation mode in which the microprocessor executes M+N bit expanded instructions.

TechSearch acknowledges that the P6 microprocessor's instruction set is comprised of instructions of all "previous versions" of Intel's processors, and additional instructions newly added for the P6 microprocessor, that is, "current version" instructions. These previous version instructions are common to both the previous version processor and the P6 processor. Because the instruction set of the P6 processor is not complete without the previous version instructions, the P6 microprocessor cannot function without those instructions.

Nor does TechSearch dispute that the P6 microprocessor executes earlier version instructions in the same manner as those from the current version or that the earlier version instructions are part of the P6 microprocessor's instruction set. On that basis, we agree that the P6 microprocessor cannot infringe. The district court correctly concluded that the P6 microprocessor does not "emulate" or modify the instructions first introduced with earlier

version microprocessors when executing such previous version instructions. The P6 microprocessor cannot be said to "emulate" solely because it executes instructions that also belong to the instruction set of previous microprocessors. Those previous version instructions are part and parcel of the P6 microprocessor's instruction set.

Regardless of the version of instruction set in which an instruction was first introduced, the P6 microprocessor's instructions have the same length. Intel's processor does not operate using N bit native instructions at one time, and M+N bit expanded instructions when emulating. Nor are the M bits of the instruction ignored when the microprocessor is executing "current version" or "native" instructions.

Thus, the P6 microprocessor does not use M bits of an expanded RISC instruction, generated from an instruction which originated in a previous instruction set, to modify N bits corresponding to the current version instruction as required by the claims. Rather, the P6 microprocessor uses each bit of the previous instruction without modification, in the same manner regardless of whether the instruction originated with the P6 or an earlier version of Intel's processor. Therefore, even if we were to assume that the execution of instructions common to both the P6 and earlier version microprocessors could be deemed a form of "emulation," the instructions of the P6 microprocessor do not include M bits used to "redefine" the current version instruction to emulate an instruction of an earlier version microprocessor. Accordingly, we conclude that the district court correctly determined that no reasonable jury could find that the P6 microprocessor emulates in the manner provided in claims 4 and 14 of the '927 patent.

The district court properly rejected Dr. Hoevel's contentions on this point. Dr. Hoevel concludes that the '927 patent claims "[do] not require the additional presence of a 'native

mode' that independently executes instructions of N bits." However, claims 4 and 14 each expressly require "a native instruction width of N bits" that is "configured for emulating." This court has stated that "the motion of an accused infringer for judgment on the ground of non-infringement of a patent may be granted where the patentee's proof is deficient in meeting an essential part of the legal standard for infringement." Johnston v. IVAC Corp., 885 F.2d 1574, 1577, 12 USPQ2d 1382, 1384 (Fed. Cir. 1989). We have further recognized that specific claim limitations cannot be ignored as insignificant or immaterial in determining infringement. Perkin-Elmer Corp. v. Westinghouse Elec. Corp., 822 F.2d 1528, 1533, 3 USPQ2d 1321, 1325 (Fed. Cir. 1987). Because Hoevel fails to recognize the native mode claim requirement, a predicate to conducting a proper analysis of infringement, we conclude that TechSearch has failed to raise a genuine dispute of a material fact on this issue. We conclude, therefore, that Intel was entitled to a grant of summary judgment as to noninfringment of claims 4 and 14.

Notwithstanding that the P6 microprocessor executes the earlier version instructions without modification, TechSearch argues that it produced sufficient evidence to prevent a grant of summary judgment on the issue of infringement, arguing that the "Cuops" instruction of the P6 microprocessor emulates as claimed. Based on the testimony of its expert, Dr. Hoevel, TechSearch asserts that the "Cuops" found in the P6 microprocessors used for aliasing, or register renaming, are single M+N bit expanded RISC instructions. TechSearch further argues that twenty-four bits of the Cuops instruction, including an opcode, two sources and one destination operand, are redefined using the remaining forty-nine bits that "assist in executing the instructions" of the processors.

Even assuming this "assistance" is a type of emulation, the court correctly concluded that the P6 microprocessors do not emulate "in the same way." As Dr. Hoevel recognizes, the

"indirection" or register renaming performed by the P6 microprocessors "is attributable to out-of-order and superscalar complexities in the P6 that are not relevant to the '927 claims." The "emulation" identified by Dr. Hoevel is in fact aliasing for executing instructions out of order, and does not involve configuring the instruction set of a microprocessor to emulate the instruction set of another microprocessor as required by the claims. Furthermore, TechSearch does not challenge the court's conclusion that the format of the instructions that the P6 microprocessors uses when executing an instruction from an "earlier version" processor are absolutely indistinguishable from the format of the instructions exclusive to the P6 which operates in only one mode. Accordingly, we conclude that, even assuming TechSearch has shown that some aspect of the P6 processor may be characterized as performing a form of emulation, no reasonable jury could find that the P6 emulates in the manner claimed.

As an alternative basis for finding no infringement of claims 4 and 14, the district court held that the P6 microprocessor does not have an "expanded instruction decoder" using M bits from each expanded RISC instruction to "redefine" the RISC architecture computer in terms of the target computer during emulation. Because the issue of whether the P6 includes a decoder using M bits of the expanded RISC instruction to redefine the native instruction is so intertwined with those issues relating to the M+N bit instructions addressed supra, we shall address TechSearch's arguments regarding the court's conclusions on these issues.

First, we note that TechSearch does not dispute that the "alias multiplexer," identified by TechSearch as corresponding to the claimed decoder, simply routes the inputs selectively to the outputs. The decoder of the claimed invention, on the other hand, translates the instructions into a form for processing by the ALU in a manner involving considerable processing. We find no basis to disturb the district court's conclusion that one of ordinary skill

in the art would know that decoders and multiplexers perform substantially different functions and consist of substantially different structure. TechSearch has failed to dispute that fact.

Nor do we disagree with the district court's finding that Hoevel's testimony on this issue is insufficient to raise a material issue of fact. As the court noted, Hoevel did not contend that the multiplexer in the P6 microprocessor operates as a decoder, or that the multiplexer performs the decoding as claimed. Because the claimed decoder combines input signals to produce outputs that cause selection of the direct, indirect or emulation registers, the court correctly distinguished the operation of the alias multiplexer architecture found in the P6 on the basis that it simply steers each signal to the appropriate output field. Thus, the claimed decoding is quite different from the multiplexing found in the P6 microprocessor.

TechSearch's assertion that a multiplexer is capable of acting as a decoder does not suffice to raise a material issue of fact. Specifically, as the district court noted, TechSearch failed to provide evidence to explain how the multiplexer of the P6 performs the functions of the claimed decoder. Intel's evidence that the multiplexer does not produce outputs based on a combination of inputs stands uncontradicted. Similarly, Hoevel's wholly conclusory allegations failed to raise a genuine issue of material fact.

Nor does the multiplexer operate to "redefine" the microprocessor when "emulating." In fact, Intel's microprocessors in no way redefine instructions, much less in the manner required of the decoder recited in claims 4 and 14. The multiplexer of the P6 microprocessor does not use an additional M bits to redefine the computer when "emulating." Although Hoevel asserted that the microinstructions found in P6 microprocessors, known as "Cuops," contain fields for performing register indirection, those instructions are always the same size and always use all of their bits. Thus, no part of the Cuops microinstruction is redefined by the decoder as

claimed. Therefore, the district court correctly concluded that no reasonable jury could find that the Cuops are redefined "in any way."

With regard to claim 1, the district court concluded that to prove infringement TechSearch must show 1) that the accused products, the P6 microprocessors, have "a plurality of indirect registers pointing to emulated registers," and 2) that the accused products process the emulated registers with an arithmetic logic unit. The court determined that the macro alias register file ("MAR") of the P6 microprocessor, alleged by TechSearch to constitute indirect registers, does not point to "any registers or to anything processed by the ALU." Rather, the MAR points to "what are known as 'logical registers,'" which are merely references and not actual registers. Thus, the court determined that the MAR does not point to registers as required by the claims.

The district court further determined that TechSearch produced no evidence that "what it considers to be the 'emulated registers' in the accused products are themselves processed" by the ALU. Thus, the court concluded that Intel was entitled to summary judgment of noninfringement of claim 1.

TechSearch argues that Intel's own documents show that logical registers are registers. Specifically, TechSearch argues that because Intel identifies logical registers as registers, the district court's conclusion that the indirect registers do not point to emulated registers is incorrect.

TechSearch asserts that at most Intel established that the logical registers of the P6 microprocessor are mapped to physical registers before processing by the ALU, in accordance with the superscalar complexities in the P6, but TechSearch argues that this is an additional step that is not recited in the claim, and is therefore irrelevant. Similarly,

TechSearch argues that the claims cannot be read to require direct processing of the data in the emulated registers by the ALU because Figure 3 of the '927 patent illustrates an embodiment where the output of the emulated registers are not processed directly by the ALU but are placed into intermediate ALU registers prior to processing.

To infringe claim 1, emulation registers in the P6 must be pointed to by indirect registers and processed by the ALU. TechSearch does not dispute that there are at least two layers of registers between the alleged indirect registers and the alleged ALU. On that basis, we conclude that the P6 microprocessors cannot have registers both pointed to by the indirect registers and processed by the ALU, regardless of whether those registers are actually involved in emulation of a target instruction set. As TechSearch's own expert states, "Intel's indirect registers point to logical registers" and these logical registers are mapped to physical registers, which are processed by the ALU. Hoevel Declaration, ¶ 51. As noted, Hoevel acknowledges that due to the out-of-order and superscalar complexities of the P6 processor, the P6 processor does not have emulation registers pointing to the ALU, but that an additional step of indirection is involved. Hoevel Declaration, ¶ 51.

TechSearch counters that this additional step of indirection is irrelevant to whether the claim is infringed. We conclude, however, that where, as in this case, the claim recites steps of a method, each dependent upon the other, we cannot interpret the limitations so loosely. Rather, the claims expressly require that the indirect registers point to the emulated registers, and that the ALU processes the emulated registers.

Because TechSearch is unable to dispute that the components identified in Intel's processors as emulated registers are admittedly not both pointed to by the indirect registers and directly processed by the ALU, we cannot disturb the district court's conclusion that Intel is

entitled to summary judgment on the issue of infringement. On this basis alone, we conclude that no reasonable juror could find claim 1 infringed.

The method of claim 1 requires emulation of a target computer instruction set using the RHS bits of the instruction to enable the LHS bits to emulate the instruction set of a target computer. As noted, the '927 patent defines the terms LHS and RHS, used in claim 1 and corresponding to the left-hand bits and right-hand bits of the claimed microcoded instruction, as synonymous with the N and M bits of the expanded RISC instruction found in claims 4 and 14. '927 patent, col. 5, ll. 6-9. Claim 1 requires that a LHS of an instruction is used for executing instructions in a RISC architecture, and that the RHS is used for selecting emulated registers. Consistent with the limitations of claims 4 and 14, claim 1 further requires "[a] method for emulating the instruction set of a target computer," where that method involves the use of those "emulated registers." We conclude, therefore, in the alternative, that because no reasonable jury could find that the P6 microprocessor emulates in the manner claimed, there can be no infringement of the method recited in claim 1.

III. Appointment of a Technical Advisor

Procedural rulings are reviewed by this court under regional circuit law, the Ninth Circuit in this case, unless the procedural issues are unique to patent law. See Nat'l Presto v. W. Bend Co., 76 F.3d 1185, 1188 n.2, 37 USPQ2d 1685, 1686 n.2 (Fed. Cir. 1996). Further, "[w]e apply regional circuit law to procedural issues that are not themselves substantive patent law issues." Bose Corp. v. JBL, Inc., 274 F.3d 1354, 1360, 61 USPQ2d 1216, 1219 (Fed. Cir. 2001); Int'l Nutrition Co. v. Horphag Research Ltd., 257 F.3d 1324, 1328, 59 USPQ2d 1532, 1535 (Fed. Cir. 2001). The procedural issue, namely the use of a technical advisor to assist the district court in understanding complex scientific and technical factual issues, is not

limited to and unique to patent cases. Technical advisors may be useful for the understanding of scientific evidence generally as well as the science or technology involved in patent cases. Because understanding issues of complex science and technology is not so unique as to clearly implicate the jurisdictional responsibilities of this court in a field within its exclusive jurisdiction, Midwest Indus., Inc. v. Karavan Trailers, Inc., 175 F.3d 1356, 1359, 50 USPQ2d 1672, 1675 (Fed. Cir. 1999) (en banc in relevant part), we apply regional procedural law. The Ninth Circuit applies the abuse of discretion standard to a district court's appointment of a technical advisor. Ass'n of Mexican Am. Educators v. California, 231 F.3d 572, 591 (9th Cir. 2000) (en banc).

A technical advisor is helpful in assisting the court in understanding the scientific and technical evidence it must consider. See Id. at 590; see also Gen. Elec. Co. v. Joiner, 522 U.S. 136, 149 (1997) (Breyer, J., concurring) (endorsing the appointment of specialists to assist district courts in understanding scientific or technical evidence); Reilly v. United States, 863 F.2d 149, 156 (1st Cir. 1988). Such evidence in a patent case includes expert testimony, scientific articles and texts, and patents, upon which the court must rely in understanding the technology so that it can interpret the patent claims and determine whether to grant motions for summary judgment of validity, invalidity, infringement or noninfringement, and to assist the court in articulating appropriate jury instructions. In this case, the court specifically noted that evaluation of the prior art required it to consider and understand complex technical concepts beyond normal technical and scientific facts regularly addressed by the district court.

The district court is the gatekeeper of the trial in determining when scientific evidence is properly admissible. See Kumho Tire Co. v. Carmichael, 526 U.S. 137, 141 (1999); Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1308 n.2, 51 USPQ2d 1161, 1168 n.2

(Fed. Cir. 1999). Because this function is critical, the district court must have the authority to appoint a technical advisor in such instances so that the court can better understand scientific and technical evidence in order to properly discharge its gatekeeper role of determining the admissibility of such evidence. See Ass'n of Mexican Am. Educators, 231 F.3d at 591. However, the federal courts of appeals must determine, the extent, if any, to which a district court has established safeguards to prevent the technical advisor from introducing new evidence and to assure that the technical advisor does not influence the district court's review of the factual disputes.

The law has long recognized that it may effectively use the knowledge of experts to inform and support the judicial process to settle disputes. The Supreme Court noted that:

> Courts have (at least in the absence of legislation to the contrary) inherent power to provide themselves with appropriate instruments required for the performance of their duties. . . . This power includes authority to appoint persons unconnected with the court to aid judges in the performance of specific judicial duties, as they may arise in the progress of a cause.

Ex parte Peterson, 253 U.S. 300, 312 (1920).

The trial court's inherent search for truth is the basic building block by which the judicial process maintains its credibility within the fabric of our society. In this search, it cannot be expected that trial judges will have expertise in biotechnology, microprocessor technology, organic chemistry, or other complex scientific disciplines. Therefore, in those limited cases where the scientific complexity of the technology is such that the district court may require the assistance of a technical advisor to aid in understanding the complex technology underlying the patent, it has the inherent authority to appoint such an advisor.

A district court's appointment of a technical advisor, outside of the purview of Rule 706 of the Federal Rules of Evidence,1 falls within the district court's inherent authority, and the Ninth Circuit has held that district courts may use technical advisors when desirable and necessary. Ass'n of Mexican Am. Educators, 231 F.3d at 590. It also implicitly recognized that district courts should use this inherent authority sparingly and then only in exceptionally technically complicated cases. Id. at 590-91. Therefore, we apply the law of the Ninth Circuit and review the appointment of the technical advisor, and whether the district court properly followed appropriate procedural safeguards, for abuse of discretion. Id. at 591.

Although the Ninth Circuit has recognized the need for district courts to avoid impropriety, it has not held precisely what procedural safeguards district courts should employ. Thus, to establish a basis for our review, if the regional circuit court has not specifically spoken on the issue, we must reasonably predict how that court would decide the issue. Panduit Corp. v. All States Plastic Mfg. Co., 744 F.2d 1564, 1575, 223 USPQ 465, 472 (Fed. Cir. 1984).

In Association of Mexican American Educators, the majority noted that Judge Tashima suggested in his dissent a list of procedural safeguards. Id. at 591. The majority did not adopt the specific guidelines delineated by the dissent because such strict compliance would unnecessarily "undo [the] entire trial" in the case before it. Id. However, it recognized the need for some procedural safeguards and the need for a reviewing court to have a standard against

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1 Courts and commentators agree that the court's inherent authority to appoint a technical advisor has not been displaced by the federal rules. See Reilly v. United States, 863 F.2d 149, 158 (1st Cir. 1988); Note, Improving Judicial Gatekeeping: Technical Advisors and Scientific Evidence, 110 Harv. L. Rev. 941, 949-50 (1997).

which to judge abuse of discretion.2 This in the minimum implies the need to establish some definable safeguards for future cases. Conceptually, we can distill from the Association of Mexican American Educators opinion appropriate guidelines from which the Ninth Circuit would delineate desirable procedural mechanisms to safeguard the use of a technical advisor and generate a record for review on appeal.

These guidelines propose broad criteria for minimally safeguarding the judicial process and the district court from undue influence by the technical advisor and to ensure that the technical advisor's role is properly limited to a tutoring function and providing technical education and background information in the technology to the court. Id. at 611-14 (Tashima, J. dissenting). In essence, the guidelines propose that the district court in appointing a technical advisor must: use a "fair and open procedure for appointing a neutral technical advisor . . . addressing any allegations of bias, partiality or lack of qualifications" in the candidates;3 clearly define and limit the technical advisor's duties, presumably in a writing disclosed to all parties;4 guard against extra-record information;5 and make explicit, perhaps

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2 It is noted that through "these minimal safeguards, the parties can be assured that the technical advisor appointment process is fair and that the technical advisor does not exercise undue influence on the district court. These procedures will also enable meaningful appellate review." Ass'n of Mexican Am. Educators, 231 F.3d at 611 (Tashima, J. dissenting); see also id. at 614 n.9.

3 Typically the candidate list would be compiled through the respective parties' counsel, and through any recommendations the district court may make.

4 One option to ensure that the technical advisor adheres to these safeguards and does not bring evidence to bear on the case would be to require pre-appointment and post-completion affidavits by the technical advisor, in which the technical advisor declares that he or she has complied with these safeguards, operated within the scope of his or her assignment, and confined his or her information sources to the record.

through a report or record, the nature and content of the technical advisor's tutelage concerning the technology. Id. at 611. The fact that the use of a technical advisor is permissible under such guidelines does not mean that it is invariably desirable or that safeguards are not required. As a practical matter, there is a risk that some of the judicial decision-making function will be delegated to the technical advisor. District court judges need to be extremely sensitive to this risk and minimize the potential for its occurrence.6

In this case, we conclude, based on the record before us, that the district court did not abuse its discretion and established sufficient protective measures to ensure that Dr. Hearn did not unduly influence its decision. The court recognized that such appointments should be reserved for the exceptional case, but deemed it appropriate in this case because it concluded that this infringement determination was "a highly technical case far beyond the boundaries of the normal questions of fact and law with which judges routinely grapple." The court acknowledged that technical advisors "may not contribute evidence." As such, the court properly concluded that a technical advisor is not subject to the requirements set forth in Rule 706 of the Federal Rules of Evidence regulating the appointment of expert witnesses. The district court further recognized that the technical advisor's role is limited to explaining the

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5 Typically this would entail making clear to the technical advisor that any advice he or she gives to the court cannot be based on any extra-record information, except that the advisor may rely on his or her own technology-specific knowledge and background in educating the district court.

6 When a district court judge utilizes a technical advisor a reviewing court may want to take a hard look at the district court's decision, and to make certain that the decision does not in fact resolve factual disputes in the guise of determining that there is not a genuine issue of material fact. It has been noted that "a judge can filter out 'bad' legal advice or research from a law clerk; he or she is ill-equipped, however, to do the same with 'bad' technical advise." Ass'n of Mexican Am. Educators, 231 F.3d at 614. Moreover, reviewing courts may want to consider whether the procedural safeguards should be enhanced, or technical advisors should be allowed at all, when the district judge is acting as the trier of fact.

terminology and theory underlying the evidence offered by the parties. The court determined that its technical expert, Dr. Hearn, was a neutral third party, and explained its reasoning for that determination in its memorandum. The court assured the parties that Dr. Hearn had "agreed that he will not engage in any independent investigation of the underlying litigation, provide evidence to the Court, or contact any party or witness in this action." The court further agreed to identify any material relied upon by Dr. Hearn, other than that submitted by the parties or that "upon which a person versed in the relevant field of knowledge would be reasonably expected to rely." The court stated that Dr. Hearn would execute an affidavit indicating his understanding of that order before beginning his engagement, and would file an affidavit attesting to his compliance with its terms at the conclusion of his employment.

TechSearch complains that the district court abrogated its authority by allowing Dr. Hearn to resolve disputed issues of fact. It asserts that the district court could not have resolved the issues before it without improperly relying on the conclusions of Dr. Hearn, as evidenced by the fact that the district court had to seek the assistance of a technical advisor. TechSearch further alleges that Dr. Hearn undertook independent research and possible experiments. It asserts that the district court likely used such information and that this created reversible error, and that the district court should have allowed the parties to depose Dr. Hearn consistent with Fed. R. Evid. 706 to determine the extent this alleged evidence influenced the court. TechSearch's allegations of independent research and experimentations stem from, inter alia, the fact that Dr. Hearn purchased computer equipment and software while a technical advisor to the court. On that basis alone, TechSearch speculates that Dr. Hearn must have been conducting independent experiments on microprocessor architecture. That Dr. Hearn billed his time to "research" and charged the court for calls he had placed, is the

foundation upon which TechSearch bases its allegation of independent research. Finally, TechSearch alleges that Dr. Hearn's failure to certify his compliance with the order was reversible error.

TechSearch's arguments are without merit. As noted, the district court appointed Dr. Hearn as a technical advisor. Rule 706 applies to expert witnesses, but not to technical advisors. Unlike a technical advisor, an expert witness appointed by the court may be relied upon "as a source of evidence" and may be called upon to testify. Ass'n of Mexican Am. Educators, 231 F.3d at 591. Such was not the case here. Accordingly, we reject TechSearch's argument that the district court's failure to subject Dr. Hearn to cross-examination by the parties constitutes reversible error.

Upon review of the record before us, we are not convinced that the evidence suggests that Dr. Hearn conducted independent experiments or research. Nor are we persuaded that the evidence establishes that Dr. Hearn's failure to certify his compliance with the order was reversible error. As noted, the court exercised great care to insure that Dr. Hearn's assistance did not unduly influence the court's consideration of the evidence. To the extent the procedures followed by the district court fell somewhat short of those essential to avoiding such influence, we note that the district court appointed the technical advisor prior to the issuance of the Ninth Circuit's en banc opinion in Association of Mexican American Educators, and the district court at least followed the minimum requirements necessary at that time. Given the extent of the safeguards imposed by the district court as it exercised due care to avoid improper influence by its technical advisor, we conclude that the district court did not abuse its discretion in the appointment and use of the technical advisor.

CONCLUSION

We agree with the claim construction articulated by the district court. We further conclude that the district court properly granted Intel's motion for summary judgment of noninfringement. We also conclude that the district court did not abuse its discretion in the use of a technical advisor. Accordingly, the judgment of the district court is

AFFIRMED.

COSTS

No costs.

United States Court of Appeals for the Federal Circuit

00-1226, -1250

TECHSEARCH, L.L.C.,

Plaintiff-Appellant,

v.

INTEL CORPORATION,

Defendant-Cross Appellant

DYK, Circuit Judge, concurring.

I join parts I and III of the majority opinion and its excellent treatment of the technical advisor issue — with one qualification. My one qualification is that I am concerned that district court judges may have a tendency to rely on technical advisors in summary judgment situations to resolve disputed issues of fact. Since we review the grant of summary judgment without deference, it can be argued that such excessive reliance would be harmless error. But appellate review is not always perfect, and, as a practical matter, "common sense dictates that the trial judge's view will carry weight" even where our review is de novo. Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448, 1462, 46 USPQ2d 1169, 1180 (Fed. Cir. 1998) (en banc) (Plager, J., concurring). These risks with respect to the use of technical advisors make it all the more important that district judges confine technical advisors to the proper sphere — to provide advice without compromising the decision-making obligation of the district judge. As the majority recognizes, we must be particularly careful to take a "hard look" at the district court's conclusions. Ante at 33 n.6.

In this particular case I think that the district court's infringement analysis may have been too heavily influenced by the technical advisor, and that the district court may have resolved factual issues on summary judgment. However, the result the district court reached is correct, and as to each of the claims in dispute there is a ground for a finding of noninfringement that does not implicate my concerns about the use of the technical advisor. Accordingly, I join part II to the extent that it holds that (1) as to claim 1, Intel's P6 microprocessors lack emulated registers that are directly processed by an arithmetic logic unit ("ALU"); and (2) as to claims 4 and 14, Intel's P6 microprocessors lack an "expanded instruction decoder." This is sufficient to establish noninfringement as a matter of law. To establish noninfringement, Intel need only show that one limitation of each asserted claim is not met by Intel's P6 microprocessors. Rohm & Haas Co. v. Brotech Corp., 127 F.3d 1089, 1092, 44 USPQ2d 1459, 1462 (Fed. Cir. 1997); Laitram Corp. v. Rexnord, Inc., 939 F.2d 1533, 1535, 19 USPQ2d 1367, 1369 (Fed. Cir. 1991).