United States Court of Appeals for the Federal Circuit

01-1031, -1032, -1034

WINBOND ELECTRONICS CORPORATION
and WINBOND ELECTRONICS NORTH AMERICA CORPORATION,

Appellants,

and

SILICON STORAGE TECHNOLOGY, INC.,

Appellant,

and

SANYO ELECTRIC CO., LTD.,

Appellant,

and

MACRONIX INTERNATIONAL CO., LTD. and MACRONIX AMERICA, INC.,

Intervenors,

v.

INTERNATIONAL TRADE COMMISSION,

Appellee,

and

ATMEL CORPORATION,

Intervenor.

01-1128

ATMEL CORPORATION,

Appellant,

v.

INTERNATIONAL TRADE COMMISSION,

Appellee,

and

MACRONIX INTERNATIONAL CO., LTD. and MACRONIX AMERICA, INC.,

Intervenors,

and

WINBOND ELECTRONICS CORPORATION
and WINBOND ELECTRONICS NORTH AMERICA CORPORATION,

Intervenors,

and

SILICON STORAGE TECHNOLOGY, INC.,

Intervenor,

and

SANYO ELECTRIC CO., LTD.,

Intervenor.

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DECIDED: January 30, 2001

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Before CLEVENGER, RADER, and DYK, Circuit Judges.

RADER, Circuit Judge.

Pursuant to this court's order of January 30, 2001, this opinion constitutes the court's opinion with respect to claim construction and infringement of Atmel Corp.'s U.S. Patent No. 4,451,903 (the '903 patent).

The United States International Trade Commission determined that Macronix International Co., Ltd., and Macronix America, Inc., (collectively "Macronix") did not infringe claims 1 and 9 of the '903 patent. The Commission further found that Winbond Electronics Corp. and Winbond Electronics North America Corp. (collectively "Winbond") did infringe claims 1 and 9 of the '903 patent. Because the Commission erred in its construction of claims 1 and 9 of the '903 patent, this court vacates the Commission's judgment of non-infringement and remands for further proceedings to determine whether Macronix infringes the '903 patent under a correct claim construction. However, because this court's claim construction does not affect the Commission's determination that Winbond infringes the '903 patent, this court affirms that determination.

I.

The '903 patent discloses a semiconductor device and a method for encoding information onto and retrieving information from the device. In particular, the '903 patent discloses a semiconductor chip with circuitry that performs the primary function of the chip connected to memory cells containing the device's manufacturing and programming information. Thus, using the patented invention, a user can easily acquire information about the manufacture of the chip without disturbing the chip's primary functions.

According to the patent's written description, a chip's manufacturing and programming information is encoded onto specific memory cells called the "product information array." During regular operation of a semiconductor device, the information in the chip's main memory array is accessed by applying a signal at conventional voltage levels to a selected pin. This signal enables the chip's row decoder and column decoder to retrieve information from the chip's memory array. The retrieved information then appears at the output of the device through the chip's output buffer and pins.

During operation of the semiconductor device to access information in the product information array of the chip in accordance with the disclosed invention, a higher voltage signal is applied to the same selected pin. An "access logic" circuit detects the higher voltage signal and disables the row (or column) decoder of the chip, thereby addressing the product information array instead of the main memory array. The column decoder (or row decoder if it is the column decoder that is disabled) then retrieves the memory stored in the product information array and provides the information through the chip's output buffer and pins. In this manner, the chip's manufacturing and programming information is provided at the output of the semiconductor device. A conceptual schematic diagram of the '903 patent's disclosed invention is depicted below.

Apparatus claim 1 of the ‘903 patent recites:

> A device for providing semiconductor product information to a user through electrical interrogation comprising
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> a primary circuit disposed upon a semiconductor chip,
>
> a product information array disposed on the semiconductor chip adjacent said primary circuit, said product information array including information sufficient to identify at least the manufacturer of the chip,
>
> access means for receiving first and second signals and for selecting said primary circuit in response to said first signal, said access means including a logic circuit means responsive to said second signal for selecting said product information array while simultaneously preventing access to said primary circuit,
>
> output means for providing output signals representative of the information stored in said product information array.

(Emphasis added.) Method claim 9 of the ‘903 patent recites:

> A method of encoding product information on semiconductor devices including at least identification of the manufacture[r] of the semiconductor device comprising the steps of
>
> providing a nonvolatile storage means on the device adjacent a primary circuit,
>
> encoding in the storage means selected semiconductor product information including at least identification of the manufacturer, and

> providing access means to permit access to said primary circuit during a fir[s]t interval and to permit the encoded information to be retrieved from the storage means while simultaneously preventing access to said primary circuit during a second interval.

(Emphasis added.) The '903 patent issued on March 29, 1984, and will expire on September 18, 2001.

In March of 1997, based on Atmel's complaint, the Commission initiated an investigation of Macronix, Winbond and Sanyo (collectively "respondents") under section 337 of the Tariff Act of 1930, as amended by 19 U.S.C. § 1337. Atmel alleged that Macronix, Winbond and Sanyo violated section 337 by importing, selling for importation, and/or selling in the United States after importation, semiconductor chips that infringe the claims of three Atmel patents, including the '903 patent. Silicon Storage Technology, Inc., a company that imports Sanyo and Winbond chips, intervened in the investigation.

In his initial determination of March 19, 1998, the presiding administrative law judge concluded that none of the respondents violated section 337. Specifically, based on his claim construction, the administrative judge found, inter alia, claims 2 to 8 of the '903 patent invalid for indefiniteness and that none of the respondents infringed claim 1 or 9 of the '903 patent. Upon the parties' requests, the Commission held a hearing to review the administrative judge's decision.

In its July 9, 1998, opinion, the Commission held the '903 patent "unenforceable for failure to name an inventor" and thus determined that none of the respondents violated section 337. The Commission further held: "No remedy based on infringement of the '903 patent can be issued unless and until inventorship has been corrected." In the Matter of Certain EPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices and Products Containing Same, Investigation No. 337-TA-395, slip op. at 14 (July 9, 1998).

Chairman Bragg filed supplemental views to the Commission's opinion in which she determined the other issues under the Commission's review. See In the Matter of Certain EPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices and Products Containing Same, Investigation No. 337-TA-395 (July 9, 1998) (Supplemental Views of Chairman Bragg) ("Supplemental Views"). Chairman Bragg construed claims 1 and 9 of the '903 patent differently from the administrative judge. Based on her claim construction, Chairman Bragg found, inter alia, that claims 2 to 8 of the '903 patent were invalid for indefiniteness, that Macronix did not infringe the '903 patent and that Winbond did infringe claims 1 and 9 of the '903 patent. Id.

Following the Commission's opinion, in August of 1998, Atmel filed a petition for correction of inventorship with the United State Patent and Trademark Office (USPTO). After the USPTO granted Atmel a Certificate of Correction, Atmel petitioned the Commission for a rehearing on the issue of inventorship. The Commission remanded to the administrative judge to determine all issues relating to inventorship and the Certificate of Correction.

In his second initial decision, the administrative judge found the '903 patent unenforceable because the Certificate of Correction named incorrect inventors and because Atmel committed

inequitable conduct in obtaining the Certificate of Correction from the USPTO. Upon Atmel's request, the Commission held another hearing to review the administrative judge's second initial decision. In its October 16, 2000, opinion, the Commission held the '903 patent enforceable. In the Matter of Certain EPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices and Products Containing Same, Investigation No. 337-TA-395 (October 16, 2000). The Commission further adopted the July 9, 1998, supplemental views of Chairman Bragg. Id. at 63. Thus, the Commission found claims 1 and 9 of the '903 patent infringed by Winbond and not infringed by Macronix. To prevent the respondents from further violating section 337, the Commission issued a limited exclusion order covering the respondents' accused semiconductor devices and circuit boards containing those devices.

Atmel appeals, inter alia, the Commission's judgment that Macronix's accused devices do not infringe the '903 patent. Winbond appeals, inter alia, the Commission's judgment that its accused devices infringe. This court has jurisdiction to hear Atmel's and Winbond's appeals under 28 U.S.C. § 1295(a)(6) (1994).

II.

This court reviews claim construction without deference. Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448, 1454, 46 USPQ2d 1169, 1172 (Fed. Cir. 1998) (en banc). This court reviews the Commission's factual findings for substantial evidence on the record. Nutrition Specialties and Food Ingredients GmbH v. United States Int'l Trade Comm'n, 224 F.3d 1356, 1359, 55 USPQ2d 1951, 1953 (Fed. Cir. 2000).

To properly construe an asserted claim, this court considers the intrinsic evidence of record. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582, 39 USPQ2d 1573, 1576 (Fed. Cir. 1996). This intrinsic evidence includes the patent specification and, if in evidence, the prosecution history. Id. Within this intrinsic evidence, the emphasis remains at all times on the claim language itself. Bell Communications Research, Inc. v. Vitalink Communications Corp., 55 F.3d 615, 619-20, 34 USPQ2d 1816, 1819 (Fed. Cir. 1995) ("First, and most importantly, the language of the claim defines the scope of the protected invention.").

A claim term receives its ordinary meaning unless the specification or prosecution history provide a special meaning or definition. Kegel Co. v. AMF Bowling, Inc., 127 F.3d 1420, 1427, 44 USPQ2d 1123, 1127 (Fed. Cir. 1997). Furthermore, although a patent's written description may assist construction of a claim term, this court will decline to import into the claims limitations, examples, or embodiments appearing only in the written description. Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1186-87, 48 USPQ2d 1001, 1005 (Fed. Cir. 1998). Moreover, "where some claims are broad and others are narrow, the narrow claim limitations cannot be read into the broad" to escape infringement. D.M.I., Inc. v. Deere & Co., 755 F.2d 1570, 1574, 225 USPQ 236, 239 (Fed. Cir. 1985). Accordingly, by its terms, an independent claim is generally broader than its dependent claims.

A. "primary circuit"

By adopting Chairman Bragg's supplemental views, the Commission adopted her construction of claims 1 and 9 of the '903 patent. The Commission, therefore, determined that "primary circuit" "means the circuitry that performs the primary task for which the semiconductor chip is designed and excludes the auxiliary circuitry that is added to furnish the identification capability." Supplemental Views at 17. In other words, the primary circuit includes "everything

but the product information array and the access circuitry." Id. This court detects no error in that construction.

The term "primary circuit" has not been argued by the parties to be a term of art or to have any special meaning to those of skill in this art. The written description informs the meaning of "primary circuit." The written description first defines "primary circuit" as the "portion of the chip which performs the primary function of that circuit." Col.1, ll. 66-68. The written description further describes the primary circuit as being "the memory array and associated decoders, gates and buffers." Col. 3, ll. 36-37. Furthermore, the written description uses the terms "primary circuit" and "memory array" throughout but never limits the primary circuit to the memory array alone. Accordingly, the written description supports the Commission's construction of primary array as "any circuitry present in an integrated chip before the addition of the rest of the circuitry that implements the invention." Supplemental Views at 20.

The doctrine of claim differentiation also underscores that "primary circuit" does not refer to the memory array alone as alleged by respondents. Although claim 2 was found to be invalid for indefiniteness, a finding that Atmel has not contested on appeal, dependent claim 2 provides guidance for the interpretation of broader claim 1. Specifically, claim 2 recites "[a] device as set forth in claim 1, wherein said primary circuit is a semiconductor memory having a first portion arranged to provide a primary memory array . . . ." Dependent claim 2 narrows the meaning of the term "primary circuit" of claim 1 to a semiconductor memory providing a memory array. This claim thus suggests that "primary circuit" as used in claim 1 has a broader scope than a semiconductor memory with only a memory array.

As defined by the Commission, the decoders and buffers are part of the primary circuit. This definition, however, does not define an inoperable device. As explained above, decoders and buffers retrieve and read out information from the product information array. In addition, the "access means" functions to prevent access to the primary circuit when information is read from the product information array. Thus, it might appear that, with decoders and buffers as part of the primary circuit, the product information array could not be read. To the contrary, the Commission's reading of the claim accommodates a meaning of "access means" that includes decoders. The decoders, as already noted, are also part of the primary circuit. Likewise, the output buffer is a common structure to both the "primary circuit" and "output means" claim elements.

This court's predecessor, The United States Court of Customs and Patent Appeals, held that a single structural element may perform two functions and may also support two different claim terms. In re Kelley, 305 F.2d 909, 914, 134 USPQ 397, 401 (CCPA 1962) (the same cylinder is both the "means for reducing said actuating force" and the "power driven actuator"); cf. Reed v. Edwards, 101 F.2d 550, 554, 40 USPQ 620, 622 (CCPA 1939) (holding that different parts of a single element could support two means clauses); see also Landis, Mechanics of Patent Claim Drafting, § 21 (4th ed. 1999) ("If two differently named elements of a claim each contain some or much common structure, but not entirely common structure, it is not double inclusion to give those elements different names so long as at least some structure is different."). Thus, the Commission correctly discerned that a single structure, such as a decoder or a buffer, may support two different claim limitations when such a reading "is a reasonable construction of the language of the claims." In re Kelley at 1367.

According to the written description and claims of the '903 patent, when the access logic receives the first signal for selecting the primary circuit, it enables the row decoder. The access

logic and row decoder thus function as part of the access means. The row decoder and column decoder then "perform the primary function of the circuit," namely retrieving information from the memory array. In this scenario, the output buffer and pins also "perform the primary function of the circuit," presenting the retrieved memory array data. The row and column decoders and the output buffer and pins thus function as components of the primary circuit.

When the access logic receives the second signal for selecting the product information array, it disables the row decoder. This action prevents access to the row decoder and the rest of the primary circuit. In this capacity, the column decoder no longer functions as part of the primary circuit. Rather it retrieves information from the product information array. Similarly, the output buffer and pins perform a non-primary function of presenting the retrieved product information array data. Thus, the output buffer and pins form the structure of the "output buffer" when they are not functioning as part of the primary circuit. Therefore, under this court's construction of primary circuit, including, e.g., decoders and buffers, claims 1 and 9 of the '903 patent remain operable.

B. "adjacent"

The Commission determined that "adjacent," the term describing the location of the product information array, means "lying near or next to the primary circuit, but not overlapping with the primary circuit." Supplemental Views at 22. The Commission further used the language "not overlapping with the primary circuit" interchangeably with "not surrounded by the primary circuit". E.g., Supplemental Views at 31-32. This court, however, determines that the term "adjacent" simply means "close to, next to, lying near, or adjoining," rather than "not overlapping."

"Adjacent" is not a term of art and thus should receive its ordinary and accustomed meaning: close to; next to; adjoining. Webster's II New Riverside University Dictionary 79 (1988). This definition of "adjacent" does not render the claim unclear. Moreover, neither the specification nor prosecution history suggest any special definition for the term.

Claims 1 and 9 state that the product information array is "adjacent" the "primary circuit." Because "primary circuit" encompasses more than the memory array, the limitation "adjacent" does not restrict the product information array to a position immediately next to the memory array, or extending from the memory array, or physically contacting the memory array.

The prosecution history of the '903 patent does not contradict this reading of "adjacent." During prosecution of the '903 patent, Atmel's predecessor specified that the claimed invention "defines a semiconductor information array which is integrally formed with a primary circuit on a semiconductor chip" (emphasis added). This language does not mean that the product information array is integral to the memory array. Once again, the "primary circuit" encompasses more than the memory array alone. Because "primary circuit" includes more components than just the memory array, this statement in the prosecution history has not narrowed the meaning of "adjacent." The word "integral" means "[a] complete unit: whole." Webster's II New Riverside University Dictionary 634 (1988). Thus, the prosecution history simply affirms that the product information array is formed together with the primary circuit.

In sum, this court determines that "adjacent," according to its ordinary definition, can mean adjacent on all sides. The correct interpretation of the term "adjacent," therefore, is simply "close to, next to, or adjoining," without the additional limitation of "not overlapping." This

meaning includes embodiments where the primary circuit surrounds the product information array so that the product information array is close to, next to, or adjoining the primary circuit on all sides.

C. "access means"

Use of the word "means" in a claim element in combination with a function raises the presumption that the element is a means-plus-function element to which 35 U.S.C. § 112, ¶ 6 applies. Al-Site Corp. v. VSI Int'l, Inc., 174 F.3d 1308, 1318, 50 USPQ2d 1161, 1166 (Fed. Cir. 1998). This presumption can be overcome if the claim itself recites sufficient structure or material for performing the claimed function. Id.

Both claims 1 and 9 define the term "access means" with functions performed by the access means. This language raises the presumption that "access means" is a means-plus-function element. The term "access" in front of "means" does not provide structure to the means because "access" is itself a function. Claim 1 provides some structure for the claimed function, namely "a logic circuit means responsive to said second signal." However, this "logic circuit means" itself is in means-plus-function format and, therefore, does not provide sufficient structure to overcome the presumption that "access means" is a means-plus-function element.

As the Commission correctly found, the "access means" element recites "three functions: (1) receiving a first signal that causes the access means to select the primary circuit, (2) receiving a second signal by means of a logic [circuit] means that causes the access means to select the product information array, and (3) 'preventing access' to the primary circuit while the product information array is selected." Supplemental Views at 24. Because claim 1 recites that the "access means" includes a "logic circuit means" that performs the function of "preventing access to [the] primary circuit," this court turns to the written description of the '903 patent to determine the appropriate structure corresponding to the "logic circuit means." 35 U.S.C. § 112, ¶ 6; Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc., 145 F.3d 1303, 1308, 46 USPQ2d 1752, 1755-1756 (Fed. Cir. 1998) (explaining that a court must determine the structures disclosed

in the specification that correspond to the claimed function). According to the written description, the "logic circuit means" includes array access logic that acts as an interface between the chip's selected pin and decoder. E.g., Col. 3, ll. 53-57. The "array access logic" further includes a "high voltage detection circuit" that provides an enable/disable signal for the decoder. Fig. 2; Col. 4, ll. 5-13. The high voltage detection circuit sends either an enable or disable signal to the nor gates of the decoder which turn the decoder on to select the primary circuit, or turn the decoder off to select the product information array "while simultaneously preventing access to [the] primary array." Fig. 3, Col. 4, ll. 14-27. Thus, a "high voltage detection circuit" and a "decoder" are the corresponding structures for the "logic circuit means."

The "high voltage detection circuit" and "decoder" are also the corresponding structures for the "access means" because these two structures perform all three recited functions of the "access means." The doctrine of claim differentiation further supports this construction. Claim 3, which is dependent on claim 1, recites that the "access means further includes an address pin." The "access means" of broader claim 1, therefore, is not limited to structures including an address pin. Thus, this court identifies a high voltage detection circuit and a decoder as

structure for the "access means" of claims 1 and 9.

D. "output means"

Only claim 1 uses the term "output means." Claim 1 recites "output means" in terms of its function "for providing output signals representative of the information stored in said product information array." Because claim 1 does not recite any structure for the "output means," this term is in means-plus-function format and its corresponding structure resides in the written description.

The written description states that information from the product information array is provided through the same circuit components as information from the memory array -- the output buffer and pins. Col. 2, ll. 62-65; Col. 3, ll. 1-2; Col. 4, ll. 3-4. Thus, this court finds that the output buffer and pins are the corresponding structure of the "output means."

With this claim construction in place, this court turns to the issues of infringement. Winbond's argument that its circuits do not infringe claims 1 and 9 of the '903 patent relies solely on a claim construction where the "primary circuit" is the memory array and the term "adjacent" means next to the memory array. Winbond itself admits that its SID arrays (Winbond's version of product information arrays) lie next to decoder circuitry. Because the Commission correctly construed "primary circuit," this court affirms the Commission's finding that Winbond's devices infringe claims 1 and 9 of the '903 patent. This court's construction of "adjacent" is broader than, and inclusive of, the Commission's construction. This court, therefore, does not have to perform any fact finding to affirm the Commission's conclusion of infringement by Windbond.

Winbond correctly asserts that the Commission did not construe the corresponding structure to the "access means" or the "output means" terms of claim 1, and did not make an element-by-element or equivalents comparison between Winbond's devices and these two claim limitations. However, Winbond's sole claim construction and non-infringement arguments before this court regarded the meaning of "primary circuit" and "adjacent." Because Winbond did not argue the construction of "access means" or "output means" or the application of its suggested construction to its accused devices to this court, Winbond has waived those arguments.

Turning to Macronix, the Commission found that the primary circuit in the accused Macronix devices surrounds the product information array and thus found no infringement of claim 1 or claim 9. Supplemental Views, at 31-32. Under this court's construction of the term "adjacent," however, the location of the product information array in the Macronix devices does not preclude infringement.

Unlike Winbond, however, Macronix further argues that its devices do not infringe because they do not have the same structure as the access means recited in claims 1 and 9. Macronix agrees that its devices have circuitry that accesses specific memory cells while preventing access to others. However, according to Macronix, although this circuitry performs the same function and leads to the same result, the way in which Macronix's access means functions is different from that of the access means of the '903 patent. **[GB 17-18]** Macronix also argues that its accused devices do not contain an "output means" as recited in claim 1.

Because this court has supplied a new meaning of the claim elements "adjacent," "access means" and "output means," including structures corresponding to the claimed functions of the

"access means" and the "output means," this court vacates the Commission's judgment of non-infringement by Macronix and remands to the Commission. On remand, the Commission must make findings to determine whether the accused Macronix devices have the same or equivalent structures to: (1) a high voltage detection circuit and a decoder for the "access means"; and (2) an output buffer and output pins for the "output means." Kemco Sales, Inc. v. Control Papers Co., 208 F.3d 1352, 1364, 54 USPQ2d 1308, 1351 (stating that "[i]n order for an accused structure to literally meet a section 112, paragraph 6 means-plus-function limitation, the accused structure must either be the same as the disclosed structure or be a section 112, paragraph 6 "equivalent," i.e., (1) perform the identical function and (2) be otherwise insubstantially different with respect to structure.").

CONCLUSION

This court affirms the Commission's judgment that Winbond infringes claims 1 and 9 of the '903 patent. This court vacates the Commission's judgment that Macronix does not infringe claims 1 and 9 of the '903 patent and remands to the Commission to determine whether Macronix infringes under a proper claim construction.

FOOTNOTES:

[1] The Commission also determined that Sanyo Electric Co., Ltd., ("Sanyo") waived its right to contest infringement. Sanyo does not contest this determination on appeal.

[2] The Commission did not determine any structure for the "access means" in its opinion. During oral argument, the Commission asserted that pages 24 and 25 of Chairman Bragg's supplemental views define the "access means" as a high voltage detection circuit. This court does not detect that Chairman Bragg's opinion has identified any structure corresponding to the functions of the "access means."