

United States Court of Appeals for the Federal Circuit

02-1024, -1182

NORTHROP GRUMMAN CORPORATION,

Plaintiff-Appellant,

v.

INTEL CORPORATION and XIRCOM CORPORATION,

Defendants,

and

3COM CORPORATION,

Defendant-Cross Appellant,

and

D-LINK SYSTEMS, INC.,

Defendant,

and

THE LINKSYS GROUP, INC.,

Defendant-Appellee.

David G. Wille, Baker Botts L.L.P., of Dallas, Texas, argued for plaintiff-appellant, Northrop Grumman Corporation. With him on the brief were Samara L. Kline, Larry D. Carlson and Robert M. Chiaviello, Jr.

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Paul H. Berghoff, McDonnell Boehnen Hulbert & Berghoff, of Chicago, Illinois, argued for defendant-cross appellant 3COM Corporation. With him on the brief were Leif R. Sigmond, Jr., Matthew J. Sampson, George I. Lee, Marcus J. Thymian, and Alison J. Baldwin.

Appealed from: United States District Court for the Eastern District of Texas

Judge Thad Heartfield

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DECIDED: March 31, 2003

Before MAYER, Chief Judge, FRIEDMAN, Senior Circuit Judge, and BRYSON,
Circuit Judge.

BRYSON, Circuit Judge.

Northrop Grumman Corporation (“Northrop”) is the owner of U.S. Patent No. 4,453,229 (“the ’229 patent”), entitled “Bus Interface Unit.” The ’229 patent issued in 1982. In late 2000, shortly before the patent expired, Northrop filed suit in the United States District Court for the Eastern District of Texas against several defendants, including appellees 3Com Corporation and The Lynksys Group, Inc. (collectively, “3Com”). Northrop’s complaint alleged that the defendants had infringed several claims of the ’229 patent.

The district court appointed a special master to make a report and recommendations to the court regarding claim construction. After reviewing the patent and evidence submitted by the parties, the special master construed several critical limitations of the claims in suit. Northrop objected to the special master’s claim construction in several respects, but stipulated that if the district court adopted the special master’s recommendation with regard to three of the claim construction issues, Northrop would not be able to prove infringement.

The district court adopted the special master’s claim construction in large part, including the aspects of the special master’s claim construction relating to the three issues referred to in Northrop’s stipulation. Accordingly, the district court ruled in the defendants’ favor on the issue of infringement. The court subsequently entered a final judgment under Rule 54 (b) of the Federal Rules of Civil Procedure. Northrop took the present appeal from that judgment. 3Com initially filed a cross-appeal, but now advises us that the cross-appeal is moot in light of the district court’s entry of judgment under Rule 54 (b).

On appeal, Northrop argues that the district court construed claims 1 and 13 of the patent unduly restrictively. We agree, and we therefore reverse and remand for further proceedings.

I

A computer network consists of a set of computers that are interconnected for the purpose of data exchange. Computers within a network typically exchange data over a network serial bus, i.e., a wire over which data is transmitted through a network one bit at a time. In order for the data exchange process to function smoothly, it must be monitored and controlled in accordance with a particular data exchange protocol, which is a set of standard signals that can be interpreted by each device that is connected to the network serial bus.

In the early 1980s, when the ’229 patent was issued, communications between a host computer and a serial bus were usually handled by the host computer itself. Under that system, however, valuable host computer processing power was devoted to monitoring and controlling communications over the network serial bus. Ultimately, network designers discovered that they could free up the processing resources of the host computers by incorporating separate devices, known as “bus interface units,” between each host computer and the network serial bus.

Bus interface units supervise the exchange of data between a host computer and a network serial bus. The bus interface unit performs two basic tasks: It prepares data internal to a host computer for communication on the network serial bus, and it also receives data from

the network serial bus and prepares the received data for processing by an individual host computer. In order for the network to operate efficiently, all the bus interface units on the network must operate in accordance with a particular communications protocol, which governs the method by which the various computers on the network gain access to the network and transfer data over the network serial bus.

At the time the '229 patent was issued, a leading network communications protocol was military standard 1553 ("MIL-STD-1553"). The bus protocol specified by MIL-STD-1553 uses a technique called "time division command/response multiplexing" to share the serial bus. A system employing a "command/response" protocol designates one terminal on the network as the "bus controller" and the other terminals on the network as "remote terminals." The bus controller manages communications on the serial bus by initiating commands and controlling access to the bus, while the remote terminals respond in a predetermined manner to commands from the bus controller. The remote terminals use the bus only in response to commands from the bus controller.

One object of the '229 patent was to transfer the tasks of monitoring and controlling data transfer over the network serial bus to the bus interface unit, thereby freeing the associated processing unit from the need to perform those tasks. Another object of the invention was to enable the bus interface unit to handle a wide variety of flexible bus communication message formats and data algorithms. A third object was to provide a bus interface unit capable of being operated in either a bus controller or remote terminal mode, and thus allow the same bus interface unit to be used as either a bus controller or a remote terminal, depending on the needs of the network at the time.

The accused devices in this case do not use a command/response protocol such as MIL-STD-1553. 3Com contends that the '229 patent does not cover its devices because the patent's scope is limited to devices used in command/response protocol systems, i.e., systems featuring a bus controller and remote terminals. Northrop, on the other hand, argues that its patent is not limited to command/response protocols but is applicable to a wide range of protocols using bus interface units.

The dispute between the parties focuses on two claims of the '229 patent, claims 1 and 13. Those claims provide:

1. In a multiplex data bus interface unit having a Manchester encoder/decoder providing an interface for transmit and receive shift registers to a biphase serial bus, buffer registers providing an interface for the shift registers with an internal parallel bus communicating with a parallel direct memory access data port through a bidirectional buffer, and at least one additional register responsive to the internal bus, the improvement [sic] comprising:

means for defining a functional state of the bus interface unit;

means for monitoring a plurality of logical signals characterizing the operational status of the bus interface unit, the monitoring means generating a plurality of control signals regulating a data transfer process between the biphase serial bus and the parallel direct memory access data port.

* * * * *

13. A bus interface unit comprising:

a receive shift register for receiving an incoming data stream from a biphase serial bus;

a transmit shift register for transmitting an outgoing data stream to the biphase serial bus;

a Manchester encoder/decoder for providing an interface for the transmit and receive shift registers to the biphase serial bus;

an internal parallel bus;

a receive buffer for providing an interface for the receive shift register to the internal parallel bus;

a transmit buffer for providing an interface for the transmit shift register to the internal parallel bus;

means for defining a functional state of the bus interface unit; and

means for monitoring a plurality of logical signals characterizing the operational status of the bus interface unit, the monitoring means generating a plurality of control signals regulating a data transfer process between the biphase serial bus and the internal parallel bus.

For present purposes, the most important limitations in claims 1 and 13 are the “means for monitoring” limitation and the “means for defining” limitation, which are found, in essentially identical form, in each of the two claims. Northrop argues that the special master, and thus the district court, erroneously construed those two limitations, as well as the term “bus interface unit,” by interpreting each of them as limited to devices employing a command/response protocol. Because the district court adopted the special master’s report and recommendations as to all of the limitations pertinent to this appeal, we refer to the special master’s analysis and conclusions as the district court’s.

II

The “means for monitoring” limitation is written in means-plus-function form, as permitted by 35 U.S.C. § 112, paragraph 6. Section 112, paragraph 6, allows a patentee to express a claim limitation by reciting a function to be performed rather than by reciting structure or materials for performing that function. Such a limitation is construed “to cover the

corresponding structure, materials, or acts described in the specification and equivalents thereof.” 35 U.S.C. § 112, para. 6; Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc., 145 F.3d 1303, 1307-08, 46 USPQ2d 1752, 1755 (Fed. Cir. 1998).

In construing a means-plus-function limitation, a court must identify both the claimed function and the corresponding structure in the written description for performing that function. Micro Chem., Inc. v. Great Plains Chem. Co., 194 F.3d 1250, 1258, 52 USPQ2d 1258, 1263 (Fed. Cir. 1999). Determining the claimed function and the corresponding structure for a claim limitation written in means-plus-function format is a matter of claim construction as to which we exercise de novo review. WMS Gaming Inc. v. Int'l Game Tech., 184 F.3d 1339, 1347, 51 USPQ2d 1385, 1390 (Fed. Cir. 1999); Chiuminatta, 145 F.3d at 1308, 46 USPQ2d at 1755.

From the language of the claims, the district court correctly determined that the “means for monitoring” recited in claims 1 and 13 performs two functions: “monitoring a plurality of logical signals characterizing the operational status of the bus interface unit” and “generating a plurality of control signals regulating a data transfer process.” The court then undertook to determine what structure disclosed in the written description is necessary to carry out those two recited functions. In so doing, the court focused on a passage from the written description that, in the court’s view, most clearly described the structure that performs the “monitoring” and “generating” functions. That passage reads as follows:

With reference to FIG. 2, the control signals required for loading, enabling and clearing the various registers, setting error bits 180-182 and flag bits 207-209, and informing peripheral equipment of the current operating condition of the bus interface unit 10 are supplied by a sequence logic unit 220. Because these control signals in effect regulate the entire data transfer process between the serial bus and the direct memory access port 62, sequence logic 220 must receive a set of logical signals which, when continuously monitored, completely characterize the operational status of bus interface unit 10. That is, by appropriately considering the past history and present condition of such a set of logical signals, one may determine when each register should be loaded or enabled, when the various error and flag bits should be set or cleared, etc. In a preferred embodiment, nineteen signals are received by sequence logic 220 at logic inputs X0 through X18.

'229 patent, col. 7, ll. 44-61.

Sequence logic 220, which is featured in the passage quoted above, consists of two arrays of logic gates (AND array 234 and OR array 235), a state register (flip-flops FS0 through FS6), an asynchronous input buffer (231), an inverter array (233), and associated internal wiring. Figure 2 of the '229 patent, which depicts sequence logic 220, is set out below:

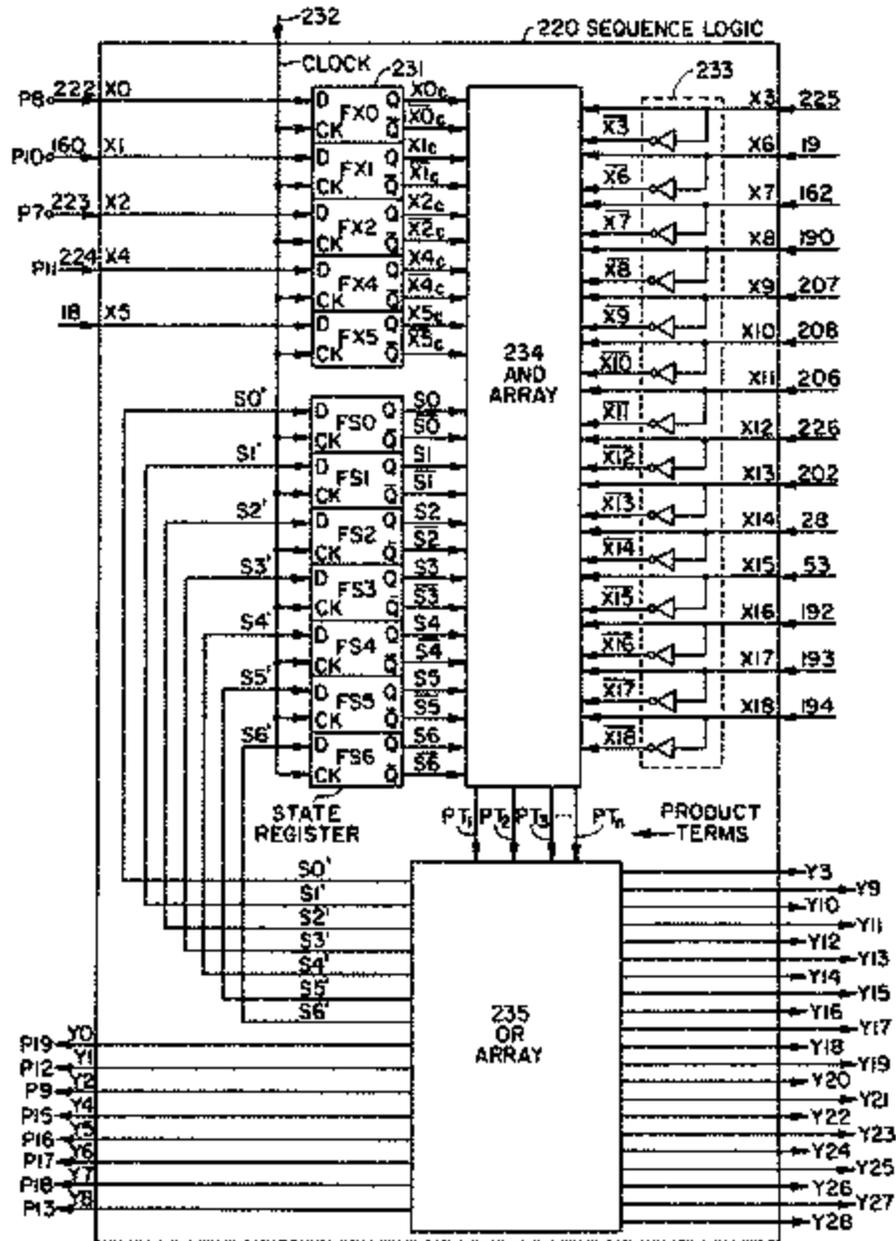


Fig.2

The district court identified the 19 signals received by sequence logic 220 at logic inputs X0 through X18 as the “plurality of logical signals characterizing the operational status of the bus interface unit” referred to in the passage quoted above. Those signals include signal 160, which is associated with pin 10 and logic input X1, and which the specification identifies as dictating whether the bus interface unit functions as a bus controller or a remote terminal in a command/response system. The court identified signals Y0 through Y28 as the “control signals regulating a data transfer process between the biphasic serial bus and the

parallel direct memory access data port” that are generated by the “means for monitoring.”

The district court correctly identified the structural components of sequence logic 220 as the structure that corresponds to the “monitoring” and “generating” functions of the “means for monitoring” in claims 1 and 13. The written description makes clear that sequence logic 220 performs the monitoring and generating functions, and that the structures within sequence logic 220 that perform those tasks include, at a minimum, the AND array 234, the OR array 235, and the flip-flops FS0 through FS6. The court, however, also included other elements as part of the “corresponding structure,” identifying those elements as “directly tied to the claimed functions.” The additional elements identified by the court were “the operating mode signal 160 from pin 10 and logical input signals [and] control signals” necessary “to define the bus interface unit as functioning in either a bus controller or a remote terminal mode, and any equivalents thereof.” By including those additional elements, the court erred.

Under section 112, paragraph 6, structure disclosed in the specification is “corresponding” structure “only if the specification or the prosecution history clearly links or associates that structure to the function recited in the claim.” B. Braun Med., Inc. v. Abbott Labs., 124 F.3d 1419, 1424, 43 USPQ2d 1896, 1900 (Fed. Cir. 1997). A court may not import into the claim features that are unnecessary to perform the claimed function. Acromed Corp. v. Sofamor Danek Group, Inc., 253 F.3d 1371, 1382, 59 USPQ2d 1130, 1138 (Fed. Cir. 2001). Features that do not perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations. See Cardiac Pacemakers, Inc. v. St. Jude Med., Inc., 296 F.3d 1106, 1116, 63 USPQ2d 1725, 1732 (Fed. Cir. 2002); Asyst Techs., Inc. v. Empak, Inc., 268 F.3d 1364, 1370, 60 USPQ2d 1567, 1571 (Fed. Cir. 2001); Wenger Mfg., Inc. v. Coating Mach. Sys., Inc., 239 F.3d 1225, 1233, 57 USPQ2d 1679, 1684 (Fed. Cir. 2001).

Those principles dictate that signal 160 and other input signals and control signals cannot be part of the structure corresponding to the functions of the “means for monitoring” limitation, because they are not part of the means for monitoring or generating signals. The specification makes clear that the signals associated with logical inputs X0 through X18, including signal 160 (which corresponds to logical input X1), are the signals that are monitored by the circuitry that constitutes the “means for monitoring.”^[1] The signals that are monitored by the “means for monitoring” cannot be part of the structure that does the monitoring. See

O.I. Corp. v. Tekmar Co., 115 F.3d 1576, 1581, 42 USPQ2d 1777, 1780 (Fed. Cir. 1997) (the passage through which a slug travels “is not the means that causes the passing”). For the same reason, control signals Y0 through Y28, which are generated by the “means for monitoring,” cannot be part of the structure that performs the recited function of “generating . . . control signals.”

The district court determined that operating mode signal 160, which enables the bus interface unit to operate in either a bus controller or remote terminal mode, plays a critical role in characterizing the “operational status of the bus interface unit.” Nothing in the written description of the ’229 patent, however, requires the term “operational status” to include the operating mode of the bus interface unit as either a bus controller or a remote terminal. In fact, other than the similarity of the terms “operating” and “operational,” there is nothing in the written description that suggests that the “operating mode” is a necessary element of the “operational status” of the bus interface unit, as that term is used in the claims of the ’229 patent.

The term “operational status” appears in the written description of the ’229 patent only once, in the statement that “sequence logic 220 must receive a set of logical signals which, when continuously monitored, completely characterize the operational status of bus interface unit 10.” ’229 patent, col. 7, ll. 52-55. The very next sentence emphasizes the breadth of the term “operational status”: “That is, by appropriately considering the past history and present condition of such a set of logical signals, one may determine when each register should be loaded or enabled, when the various error and flag bits should be set or cleared, etc.” Id., col. 7, ll. 55-59. “Considering” the past state and the present state of the device is the function normally performed by a finite state machine. Following that broad characterization of the term “operational status,” the written description goes on to describe particular embodiments, including a state machine that can be used in a bus controller/remote terminal environment. The treatment of the term “operational status” in the written description reinforces our conclusion that the portion of the patent that describes the structure corresponding to the functions recited in the “means for monitoring” limitation is quite general in nature and is not limited to a structure that monitors a signal such as signal 160. Nor must the “means for monitoring” structure necessarily include elements that define the bus interface unit as functioning in either a bus controller or remote terminal mode, as the district court concluded. We therefore disagree with the district court’s contrary construction of the “means for

monitoring” limitation. Under the construction we adopt, the structure corresponding to the “means for monitoring” includes only the structural features of sequence logic unit 220.

III

The second of the two means-plus-function limitations at issue in this case is the “means for defining a functional state of the bus interface unit.” The district court explained that the function of the “means for defining” limitation is to define the functional state of the bus interface unit, and that defining the functional state of the bus interface unit “requires, at a minimum, determining whether the bus interface unit is functioning in the bus controller or remote terminal mode.” Because the court determined that the functional state of the bus interface unit includes whether it is operating in bus controller or remote terminal mode, the court concluded that in order to define the functional state of the bus interface unit, “the operating mode signal 160 must be continuously monitored.” The district court therefore identified the structure corresponding to the function of defining the functional state of the bus interface unit as sequence logic 220, “including at a minimum the AND array 234, the OR array 235, the operating mode signal 160 at pin P10, and flip-flops of the state register necessary to define the bus interface unit as functioning in either a bus controller or remote terminal mode and any equivalents thereof.”

As in the case of the “means for monitoring” limitation, the district court defined the structure corresponding to the recited function too broadly. The written description of the ’229 patent describes the structure corresponding to the function of defining a functional state of the bus interface unit much more narrowly. The specification states:

A present functional state of logic 220 is defined by the bit pattern stored in flip-flops FS0 through FS6, allowing the implementation of up to 128 (2^7) different sequencing states. Each defined state, in turn, has one or more product lines connected by appropriate series gates to the state flip-flop outputs representing that state.

’229 patent, col. 15, ll. 6-12. That passage makes it clear that the structure corresponding to the “defining” function is the set of flip-flops, FS0 through FS6.

Other portions of the written description reinforce this interpretation of the “means for defining” limitation. The flip-flops are referred to as comprising a “state register” that outputs state variable signals, which are input to AND array 234 along with sequence logic inputs X0 through X18. ’229 patent, col. 8, ll. 62-65. Moreover, the patent explains that in each of the

128 states that are defined by the flip-flops, the bus interface unit can be arranged to monitor any selected combination of sequence logic inputs, X0 through X18. *Id.*, col. 15, ll. 17-19. Through those passages, the written description makes clear that the term “functional state” of the bus interface unit is defined by the flip-flops FS0 through FS6, and that no other features that are “necessary to define the bus interface unit as functioning in either a bus controller or remote terminal mode” (including logic inputs X0 through X18 and signal 160) are necessary parts of the structure that performs the function of “defining a functional state of the bus interface unit.” We therefore reverse the district court with respect to the “means for defining” limitation in claims 1 and 13. We construe the structural component of the “means for defining” limitation to include only the flip-flops FS0 through FS6.

IV

The third claim construction issue raised on appeal is the district court’s construction of the term “bus interface unit” in claims 1 and 13 to mean “a bus interface unit capable of functioning as a bus controller or a remote terminal when connected to a biphase serial bus in a command/response system.” The district court’s claim construction was dictated by the court’s overall view of the patent as limited to use in a command/response system. Based on that view, the court refused to construe the term “bus interface unit” according to its plain meaning, but instead gave it a more restrictive interpretation, consistent with the court’s understanding of the objectives of the patent and the preferred embodiment.

This is not a case in which the specification disavows any embodiment other than one operating in a bus controller/remote terminal environment. Nor does the patent in any other way indicate that the invention was intended solely for use in such an environment. Accordingly, we decline to read the bus controller/remote terminal limitation into claims 1 or 13. Instead, we accord the term “bus interface unit” its ordinary meaning: a unit for interfacing with a serial data bus. *See Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325-26, 63 USPQ2d 1374, 1380-81 (Fed. Cir. 2002) (“In the absence of an express intent to impart a novel meaning to claim terms, an inventor’s claim terms take on their ordinary meaning.”); *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366, 62 USPQ2d 1658, 1662 (Fed. Cir. 2002) (“Generally speaking, we indulge a ‘heavy presumption’ that a claim term carries its ordinary and customary meaning.”).

It is no doubt true that the inventor conceived that the invention of the ’229 patent would be used principally, if not exclusively, in a “command/response” environment. The patent refers repeatedly to the advantages of the invention in that context, and the description of the preferred embodiment clearly envisages a protocol in which the subsystems serve either as bus controllers or remote terminals. The “Background of the Invention” states, for example, that one of the objects of the invention “is the provision of a bus interface unit capable of being operated in either a bus controller or a remote terminal mode.” ’229 patent, col. 2, ll. 1-4. The “Detailed Description of Preferred Embodiment” describes the bus interface unit as operating in “either of two modes,” bus controller or remote terminal mode, *id.*, col. 11, ll. 35-40, and explains that the operating mode signal 160 “dictates which of two operating modes—remote terminal or bus controller—that unit 10 will operate in,” *id.*, col. 6, ll. 29-32. None of those statements, however, constitutes a limitation on the scope of the invention. The first merely

states one of several objectives that can be achieved through use of the invention; it does not suggest that the invention must always be used in a manner that achieves that objective. The statements from the description of the preferred embodiment, moreover, are just that—descriptions of a preferred embodiment that operates in a command/response system. Those statements do not indicate that the invention can be used only with a “command/response” protocol. Absent a clear disclaimer of particular subject matter, the fact that the inventor may have anticipated that the invention would be used in a particular way does not mean that the scope of the patent is limited to that context. See, e.g., Teleflex, 299 F.3d at 1328, 63 USPQ2d at 1382-83; Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 809, 62 USPQ2d 1781, 1785 (Fed. Cir. 2002). And here, notwithstanding the repeated references in the patent to the operation of the bus interface unit in either the bus controller or remote terminal mode, there is no clear disclaimer of using the invention in a protocol other than a command/response protocol.

The patent teaches that a “major object” of the invention is “handling the protocols of a wide variety of flexible bus communication message formats and data transfer algorithms.” While the patent discusses at length an embodiment that implements the MIL-STD-1553 protocol, it goes on to teach that other embodiments of the invention need not utilize that protocol. See ’229 patent, col. 17, ll. 35-42. The disclosure even teaches how to eliminate certain input signals and contemplates an embodiment in which mode codes—codes intimately associated with the MIL-STD-1553 protocol—“are not to be used.” Id., col. 17, ll. 43-50.

The nomenclature used in describing the embodiment depicted in Figure 2 of the patent suggests that the claims are to an invention of broader application than that urged by 3Com. The labeling of the logical connections between AND array 234 and OR array 235 uses generalized, not specific, algebraic nomenclature. Moreover, the patent teaches one skilled in the art that “the present invention may be made to conform to any one of a variety of data transfer algorithms.” ’229 patent, col. 17, ll. 55-57. Contrary to the finding of the district court and the assertions of 3Com, the patent does not rest upon a mere “boilerplate” suggestion of broad application. It goes on to provide substantive, albeit general, support for that declared intention:

[I]mplementation of a desired algorithm is readily accomplished in the present invention by defining functional states around the desired sequences, assigning bit patterns for each defined state, and making the appropriate connections for each assigned bit pattern in sequence logic 220.

Id., col. 17, ll. 57-63.

The quoted passage describes the process of state machine design that is familiar to

those skilled in the relevant art. Both parties agree that a person of ordinary skill in the art at the time the invention was made would have had knowledge of protocols or data transfer algorithms that did not operate in a bus controller/remote terminal environment or require an operating mode signal such as signal 160. The '229 patent teaches how to implement those other protocols in its inventive system: by defining the states associated with the protocol, assigning bit patterns for each state, and connecting AND array 234 and OR array 235 appropriately. We therefore define the term “bus interface unit” according to its ordinary meaning and reject the district court’s construction of the term as limited to a bus controller/remote terminal environment.

We recognize that our construction of claims 1 and 13 results in according those claims substantial breadth, and that the breadth of the claims may raise questions as to their validity. Any question as to validity, however, is for the district court to address on remand, inasmuch as the only issue before us on this appeal is claim construction. Accordingly, we reverse the district court’s claim construction on the three issues raised on appeal and remand the case to the district court to address the issues of infringement consistent with the claim construction adopted herein and to address any remaining defenses or counterclaims raised by the defendants.

REVERSED and REMANDED.

[1] Although the patent consistently refers to X0 through X18 as “logic inputs,” the special master’s report refers to X0 through X18 as “logical input signals.” By contrast, the patent refers to Y0 through Y28 interchangeably as “output signals” and “sequence logic outputs.” The parties do not attach significance to the distinction between logical inputs and logical input signals; indeed, 3Com, like the special master, refers to logical inputs X0 through X18 as both “signals” and “logical inputs.” The distinction, if any, is not critical to our decision.